Backplane Path Checkout List: Card_____ and Slot Number _____

First Steps: If you are testing a BP, put the EIC in the slot you intend to test. Log in to the **cmslab** account. Zero all the memories. Start **vmedia** and execute the script **eiso_backplane_slotN.txt (N=slot #)**. That will program things in the order given by the grey numbers. Place a check mark over the grey number. You will be prompted to change cables.

Direct data: check at U125 (pin 8,11,14,17) and U126 (pins 8,11,14). First hex pattern should completely show up, second should have no bits firing at all. All paths checked.

Data type: # of paths (RC slot)	First Pattern	Okay?	Second Pattern	Okay?
DIRECT A: 8 paths $440000	7F	1	00	2
DIRECT B: 8 paths $4c0000	7F	3	00	4
DIRECT C: 8 paths $540000	7F	5	00	6
DIRECT D: 8 paths $5c0000	7F	7	00	8
DIRECT E: 8 paths $640000	7F	9	00	10
DIRECT F: 8 paths $6c0000	7F	11	00	12
DIRECT G: 8 paths $740000	7F	13	00	14
DIRECT H: 8 paths $7c0000	7F	15	00	16

Shared data: The first pattern is for the adjacent card (via cable or backplane), and the second is should be in the adjacent tower for the card you are checking. First column should result in a 7F and 0 seen at the outputs for U125 and U126 and the second should result in double 7F output pulses at these chips.

Backplane R0: 8 paths	7F	17	7F and 7F	19
	00	18		
Cable R0: 8 paths	7F	21	7F and 7F	20
	00	22		
Backplane R1: 8 paths	7F	23	7F and 7F	25
	00	24		
Cable R1: 8 paths	7F	27	7F and 7F	26
	00	28		
WEST(Backplane): 8 paths	7F	29	7F and 7F	31
	00	30		
EAST(Backplane): 8 paths	7F	32	7F and 7F	34
	00	33		

Corner Data: These are probably best checked at the PLCC's leading into the EISO ASIC for R0: U66: 24, 28, 4, 6 and 23, 27, 3, 5 R1: U128: 24, 28, 4, 6 and 23, 27, 3, 5. This is the order for an even slot. The pin sets are reversed for an odd slot.

SW(Backplane): 4 paths	FF	35
NW(Cable): 4 paths	FF	36
Move the West Cable to the East Side		
SE(Backplane): 4 paths	FF	37
NE(Cable): 4 paths	FF	38