EI Card Backplane Path Checkout List: Card Number _____

First Steps: Zero all the memories. Execute scripts aa3.txt, eiso_setup.txt in vmedia, and script run_all.txt. Set EI Card command register $00 to 0x84 for an odd card and 0x04 for an even card. Set EI Card command register $02 to 0x09 for cards 0-5 and 0x89 for card 6.

Direct data: check at U125 and U126. First hex pattern should completely show up, second should have no bits firing at all. All paths checked.

Path: # of Bits	First Pattern	Okay?	Second Pattern	Okay?
DIRECT A: 8 bits $440000	7F		FF	
DIRECT B: 8 bits $4c0000	7F		FF	
DIRECT C: 8 bits $540000	7F		FF	
DIRECT D: 8 bits $5c0000	7F		FF	
DIRECT E: 8 bits $640000	7F		FF	
DIRECT F: 8 bits $6c0000	7F		FF	
DIRECT G: 8 bits $740000	7F		FF	
DIRECT H: 8 bits $7c0000	7F		FF	

Shared data: The first pattern is for the adjacent card (via cable or backplane), and the second is should be in the adjacent tower for the card you are checking. First column should result in a 7F and 0 energy seen at the outputs for U125 and U126 and the second should result in double output pulses at these chips. Place the 7F's at opposite sides to be sure.

TOP R0: 8 bits	3F & 40 Adj.		80 & 7F Adj. & 7F Opp.	
	40 & 3F Adj.			
BOT R0: 8 bits	3F & 40 Adj.		80 & 7F Adj. & 7F Opp.	
	40 & 3F Adj.			
TOP R1: 8 bits	3F & 40 Adj.		80 & 7F Adj. & 7F Opp.	
	40 & 3F Adj.			
BOT R1: 8 bits	3F & 40 Adj.		80 & 7F Adj. & 7F Opp.	
	40 & 3F Adj.			
WEST: 8 bits	3F & 40 Adj.		80 & 7F Adj. & 7F Opp.	
	40 & 3F Adj.			
EAST: 8 bits	3F & 40 Adj.		80 & 7F Adj. & 7F Opp.	
	40 & 3F Adj.			

Corner Data: These are probably best checked at the PLCC's leading into the EISO ASIC for R0: U66: 3,4,5,6,27,28,23,24 R1: U128: 3,4,5,6,27,28,23,24

NW: 4 bits	FF	
SW: 4 bits	FF	
Move the West Cable to the East Side		
NE: 4 bits	FF	
SE: 4 bits	FF	