Clock and Control Clock Checkout List: Card Number_____

Compare phases on Receiver Cards' 160 MHz Clock, Reset, 120 MHz Clock, & BC0

RC Slot 1 and RC Slot 4

Signal	Difference in ps	Slot 1 or Slot 4 earlier?
160 MHz Clock (R473 pin 2)		
Reset (R473 pin 1)		
120 MHz Clock (R204 pin 8)		
BC0 (R229 pin 2)		

RC Slot 1 and RC Slot 6

Signal	Difference in ps	Slot 1 or Slot 6 earlier?
160 MHz Clock (R473 pin 2)		
Reset (R473 pin 1)		
120 MHz Clock (R204 pin 8)		
BC0 (R229 pin 2)		

RC Slot 2 and RC Slot 6

Signal	Difference in ps	Slot 2 or Slot 6 earlier?
160 MHz Clock (R473 pin 2)		
Reset (R473 pin 1)		
120 MHz Clock (R204 pin 8)		
BC0 (R229 pin 2)		

Compare phases on EI Cards' 160 MHz Clock and Reset

EIC Slot 1 and EIC Slot 4

Signal	Difference in ps	Slot 1 or Slot 4 earlier?
160 MHz Clock (R309 pin 3)		
Reset (R309 pin 1)		

EIC Slot 1 and EIC Slot 6

Signal	Difference in ps	Slot 1 or Slot 6 earlier?
160 MHz Clock (R309 pin 3)		
Reset (R309 pin 1)		

EIC Slot 2 and EIC Slot 6

Signal	Difference in ps	Slot 2 or Slot 6 earlier?
160 MHz Clock (R309 pin 3)		
Reset (R309 pin 1)		

Compare phases on RC's and JSC's 160 MHz Clock, Reset, and 120 MHz Clock

JSC Slot and RC Slot 3 (locations of signals are for JSC rev B, RC is given above)

Signal	Difference in ps	JSC or RC earlier?
160 MHz Clock (R381 pin 2)		
Reset (R381 pin 1)		
120 MHz Clock (R405 pin 8)		
BC0 (R251 pin 2)	JSC should be ~1.5 ns later	

Check that all RC's, EIC's, and the JSC are receiving their signals:

Card	160 MHz	Reset	120 MHz	BC0
RC0	R473 pin 2	R473 pin 1	R204 pin 8	R229 pin 2
RC1	R473 pin 2	R473 pin 1	R204 pin 8	R229 pin 2
RC2	R473 pin 2	R473 pin 1	R204 pin 8	R229 pin 2
RC3	R473 pin 2	R473 pin 1	R204 pin 8	R229 pin 2
RC4	R473 pin 2	R473 pin 1	R204 pin 8	R229 pin 2
RC5	R473 pin 2	R473 pin 1	R204 pin 8	R229 pin 2
RC6	R473 pin 2	R473 pin 1	R204 pin 8	R229 pin 2
EIC0	R309 pin 3	R309 pin 1	N/A	N/A
EIC1	R309 pin 3	R309 pin 1	N/A	N/A
EIC2	R309 pin 3	R309 pin 1	N/A	N/A
EIC3	R309 pin 3	R309 pin 1	N/A	N/A
EIC4	R309 pin 3	R309 pin 1	N/A	N/A
EIC5	R309 pin 3	R309 pin 1	N/A	N/A
EIC6	R309 pin 3	R309 pin 1	N/A	N/A
JSC	R381 pin 2	R381 pin 1	R405 pin 8	R251 pin 2

Validate the cable outputs with the new CCC card and the inputs using CCC 500 in the EIC slot 3, all probing is on the new CCC, card 500 needs all of SW3 off!

1. Output Clocks:
    a. Attach the testing cable on new CCC from connector J7 to J9
    b. Probe on U115 pin 3 and 4 for 120 MHz Clock. Okay? ☐
    c. Probe on U115 pin 23 and 24 for 160 MHz Clock. Okay? ☐
2. Output L1 Accept, Reset, BX0:
    a. Attach the testing cable on new CCC from connector J6 to J8
    b. In vmedia type: `aa3.txt`
    c. For L1 Accept probe on U114 pins 9 and 10
    d. In vmedia type: `l1a` twice to see the signal edge on each pin. Okay? ☐
    e. For Reset probe on U114 pins 3 and 4
    f. In vmedia type: `resys` twice to see the signal edge on each pin. Okay? ☐
    g. For L1 Accept probe on U114 pins 20 and 21
    h. In vmedia type: `bx0` twice to see the signal edge on each pin. Okay? ☐
3. Input Clocks:
    a. Attach the testing cable from CCC #500 J7 to new CCC J9
    b. Turn off Switch SW32 (front panel)
    c. Probe U115 pin 14 and 15 for 120 MHz Clock. Okay? ☐
    d. Probe U115 pin 17 and 18 for 160 MHz Clock. Okay? ☐
4. Input L1 Accept, Reset, BX0:
    a. Turn on Switch SW32 (front panel)
    b. In vmedia type: `poke 1 10000002 00`
    (to make signals come from a remote source)
    c. Attach the testing cable from new CCC #500 J6 to new CCC J8
    d. In vmedia type: `ccc_test_cables.txt`
    e. For L1 Accept probe on U114 pins 13 and 12
    f. In vmedia type: `l1a` twice to see the signal edge on each pin. Okay? ☐
    g. For Reset probe on U114 pins 14 and 15
    h. In vmedia type: `resys` twice to see the signal edge on each pin. Okay? ☐
    i. For L1 Accept probe on U114 pins 17 and 18
    j. In vmedia type: `bx0` twice to see the signal edge on each pin. Okay? ☐