CMS

Compact Muon Solenoid

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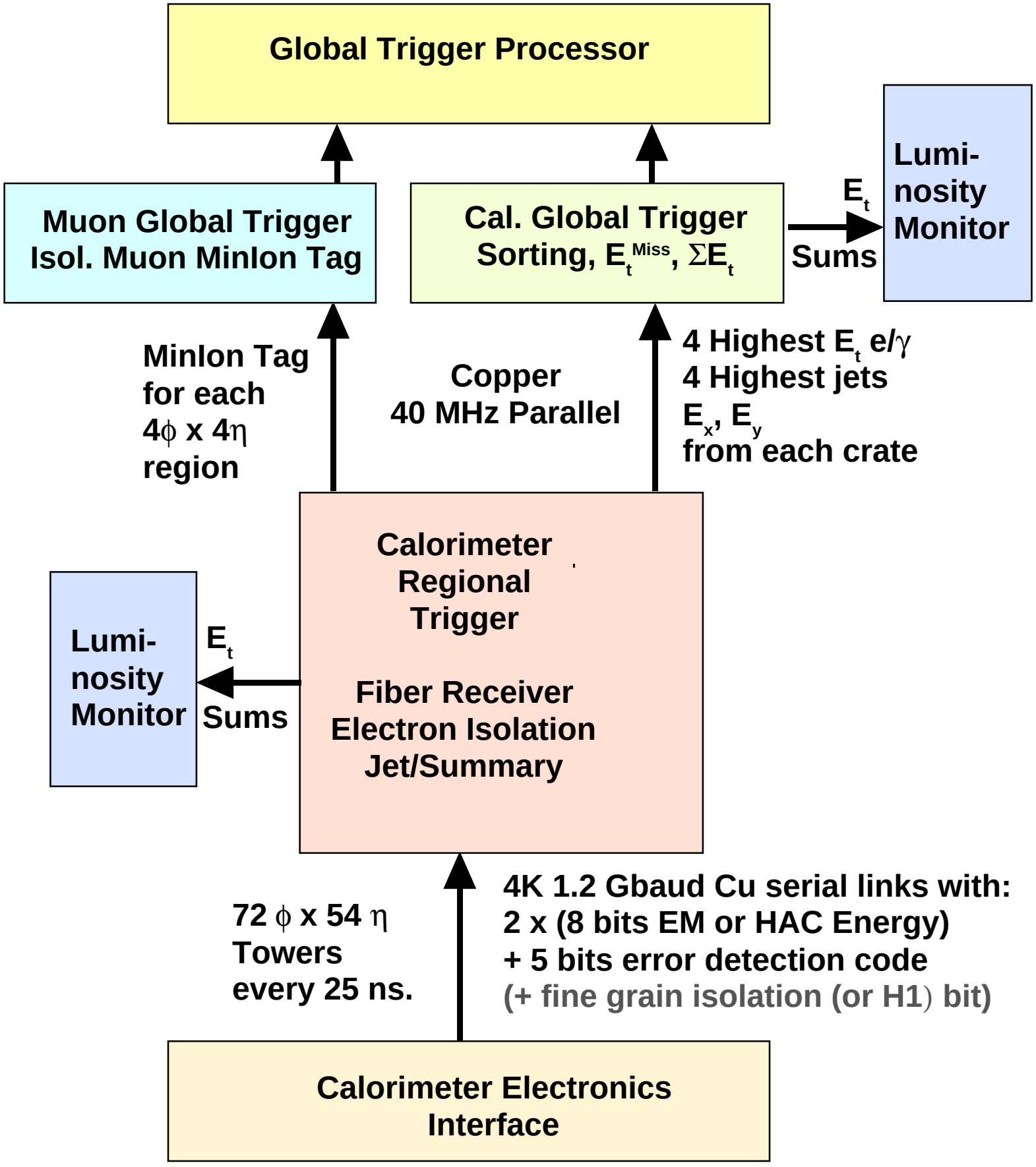
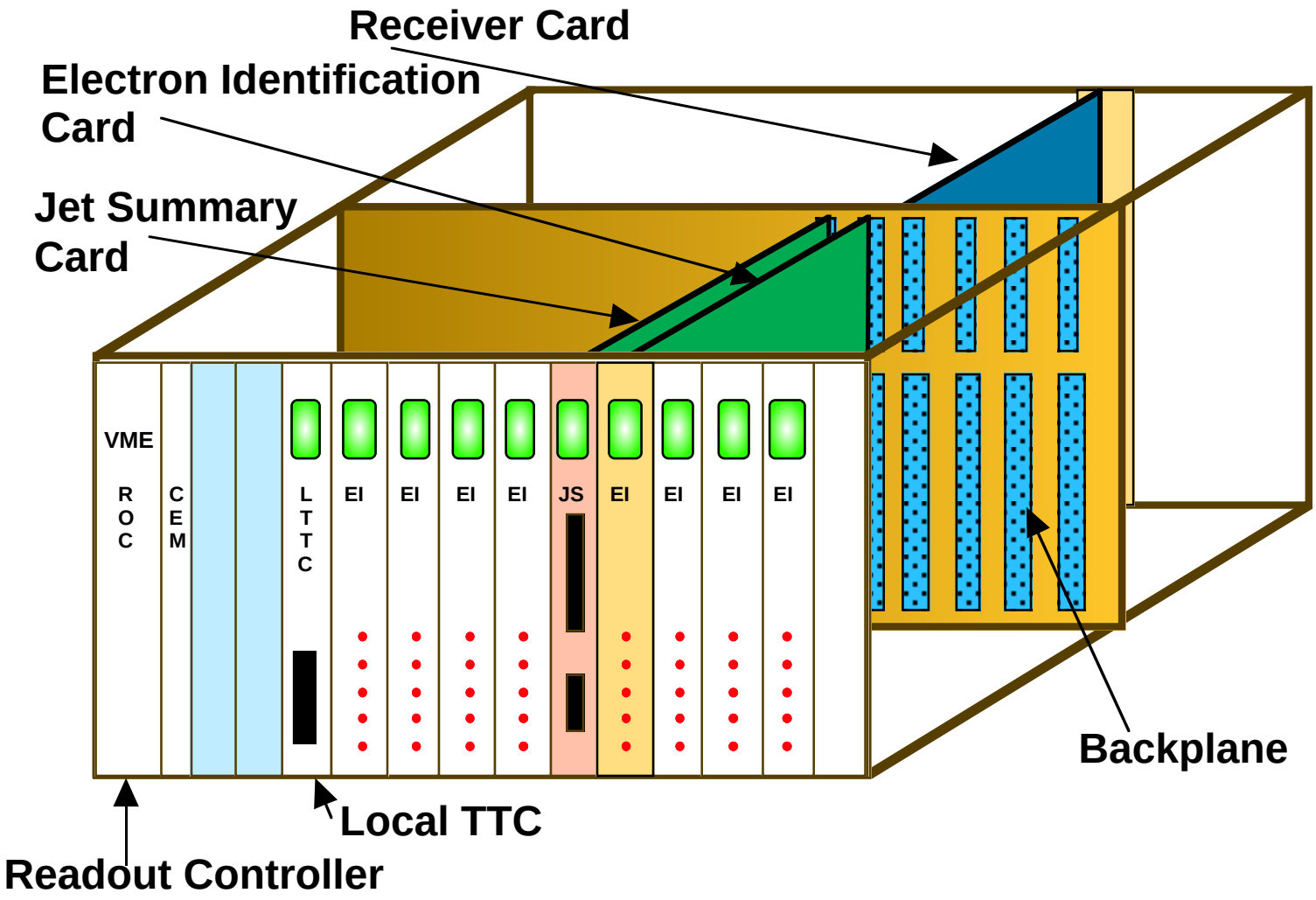
Calorimeter Regional Trigger:

- Hardware Progress
- R&D Plans
- Cost & Schedule

Calorimeter Trigger Overview



Regional Calorimeter Crate



Data from calorimeter FE on Cu links @ 1.2 Gbaud

- Into rear-mounted Receiver Cards

160 MHz point to point backplane

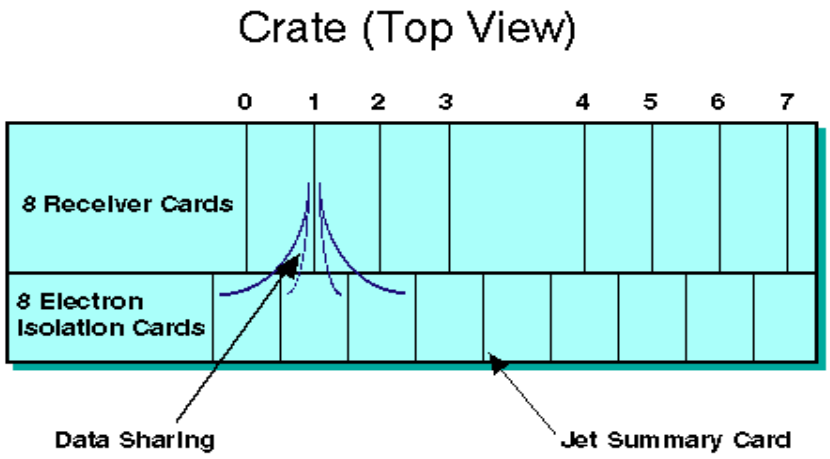
- Receiver, Electron Identification, Jet Summary Cards Operate @ 160 MHz

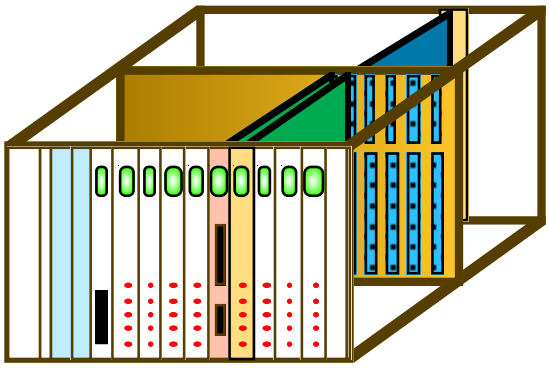
Output to calorimeter global trigger

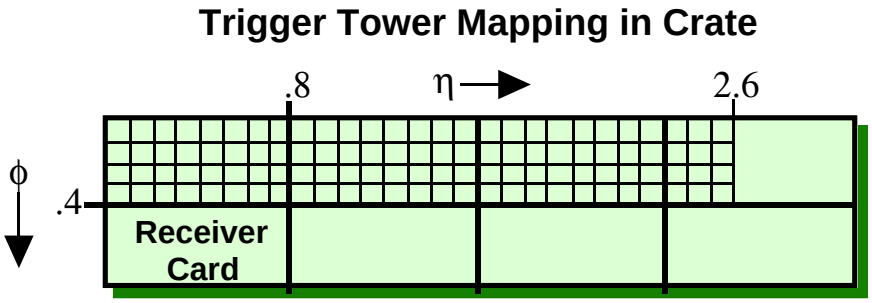
- From Jet Summary Card

Min Ion and Quiet bits to muon trigger

Receiver Card Function





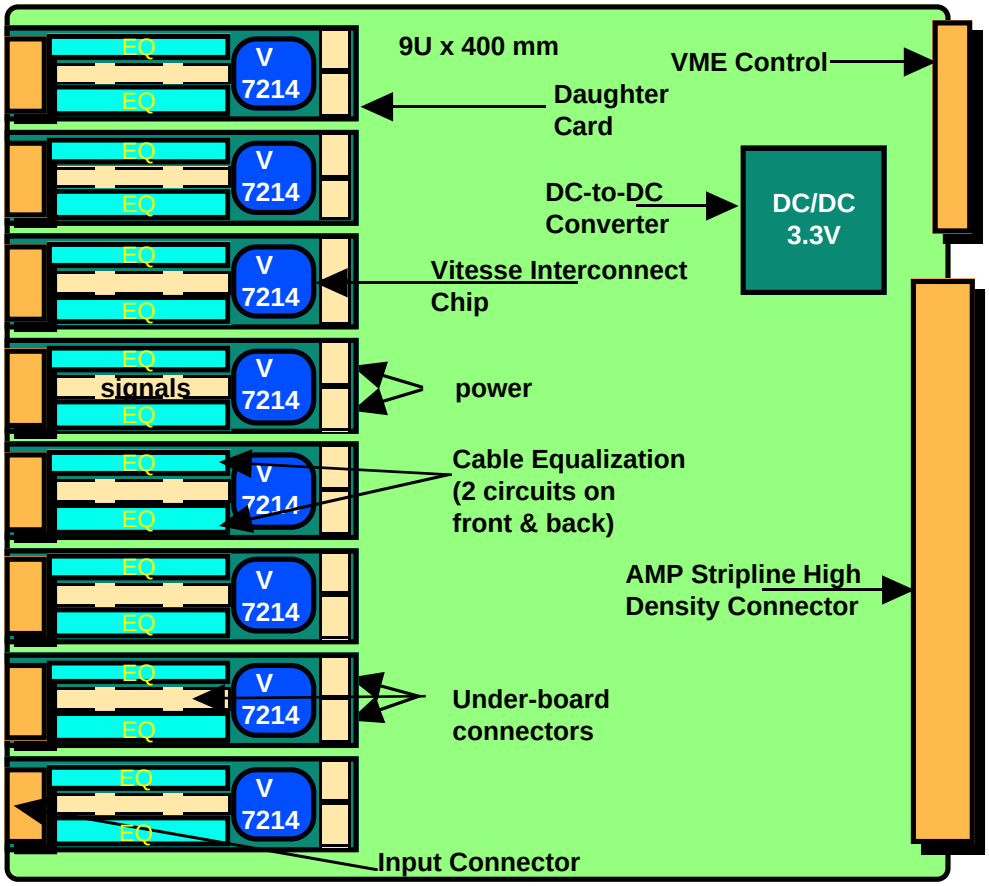


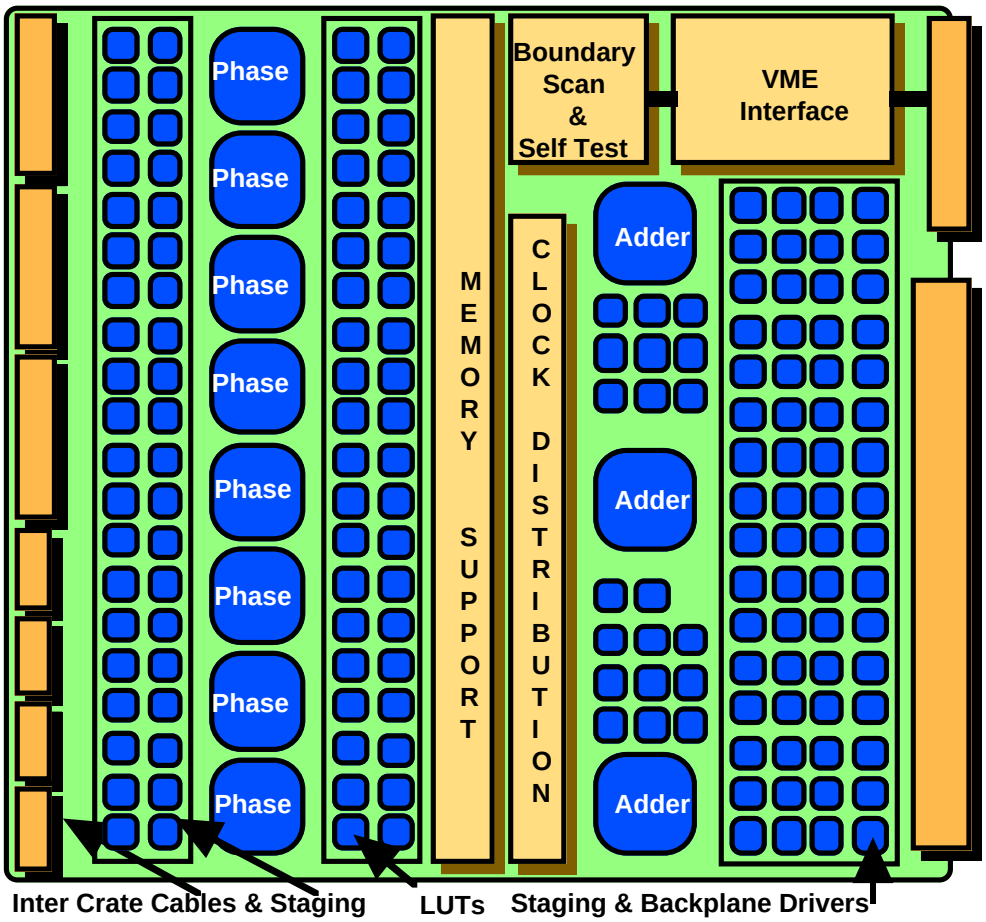
Design optimized to forward data for further processing only at appropriate resolution and only on need-to-know basis.

Receiver card

- Receives 8-bit non-linear E_t + 1-bit ID data from 32 ECAL & corresponding HCAL trigger towers.
- Linearizes ECAL & HCAL E_t & prepares data for subsequent processing by Electron ID Card.
- Stages this & neighbor tower data to Elec. ID card.
- Linearizes ECAL and HCAL E_t on 8-bit scale and uses Adder ASIC to make 4x4 sums for jet and missing E_t triggers.
- ORs ECAL fine-grain EM ID and HCAL Muon ID bits separately for each 4x4 region.
- Stages 4x4 region data to Jet/Summary cards.

Receiver Card





Rear:

32 Channels = 4 Ch. x 8 daughter cards

1.2 GBaud copper rcvrs

18 bit (2x9) data + 5 bit error det. codes

Vitesse Chip Converts Serial to Parallel

Front:

Data from Rear @ 120 MHz TTL

Phase ASIC: Deskew, EDC, Mux @ 160MHz ECL, Test vectors

Error bit for each 4x4

Memory LUT @ 160 MHz

Adder ASIC: 8 inputs @ 160 MHz in 25 ns. (built!)

Differential Out@160 MHz

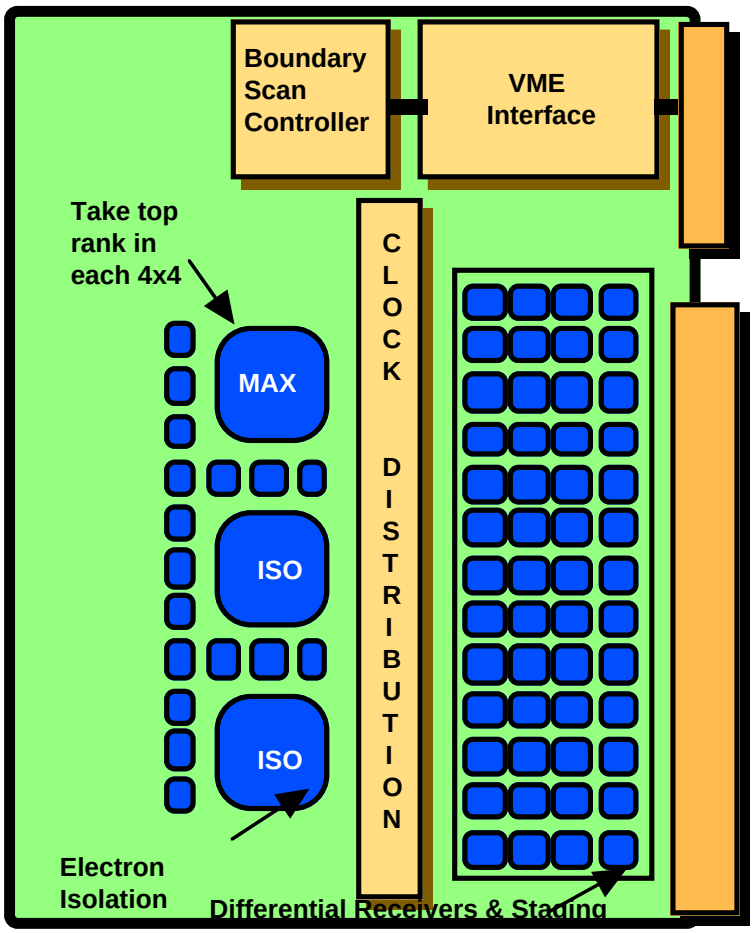
Cu Data Link Specification

Support for 64 E/HCAL ch. per Receiver card.
Same technology for both E/HCAL (32 ch. each)
2 channels per copper link:

- **Use 24-bit frame to get better trigger energy resolution than 21-bit G-Link frame**
  - 18-bit data + 5-bit error detection code
  - 8-bit energy + 1-bit fine-grain ID per channel
- **Error detection bits are necessary for error logging and to zero problem channels that can cause high spurious trigger rate.**
- **24-bit word with 8/10-bit encoding implies 1.2 GHz serial link.**
- **Non-halogenated candidate cables are available. (Cable development being pushed by 1000BaseT ethernet).**
- **Agreement w/HCAL to limit link length at 20m.**

4 links per connector: one per daughter card
4 links per Vitesse VSC7214 per daughter card
Channel grouping must match between E/HCAL.
Data across all channels (ECAL & HCAL) should be synchronized for both trigger primitive extraction and DAQ readout.
Data transmitted on equal length cables.
Limited phase adjust allowed on Receiver card.

Electron ID & Jet/Summary Cards



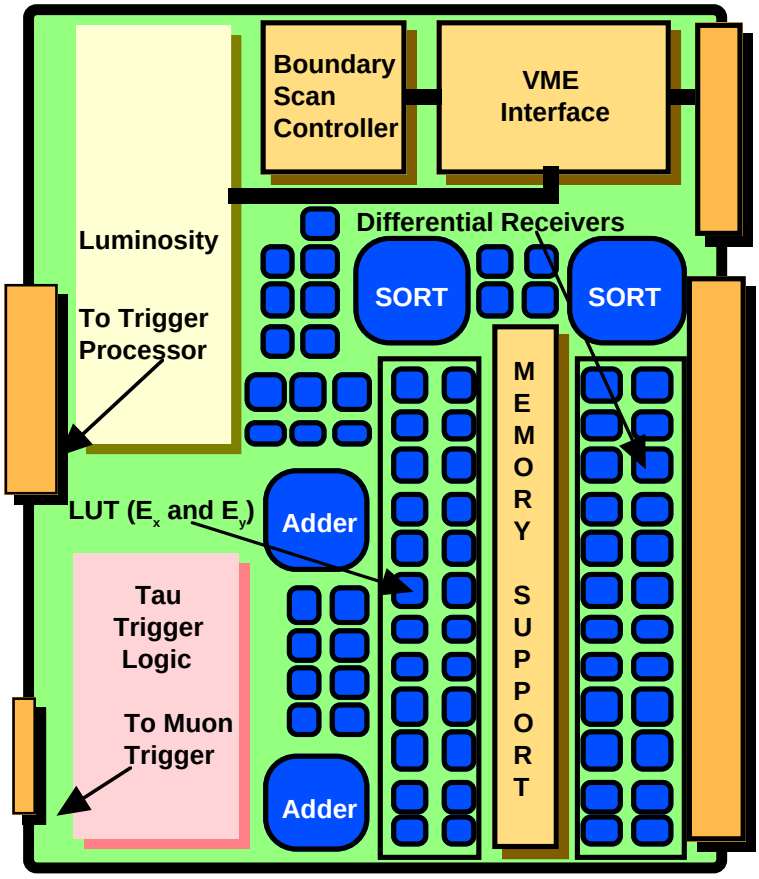
Electron Identification:

Processes 4x8 region @ 160 MHz

Electron isolation on ASIC

Lookup tables for ranking

Select top rank candidate in each 4x4 region



Jet/Summary:

Summarizes full crate:

Sorts 32 electrons for top 4

Sorts 32 4x4 E_t sums for top 4 jets

LUTs generate E_x & E_y from E_t for 4x4 region

Adder tree for crate E_t, E_x and E_y sums

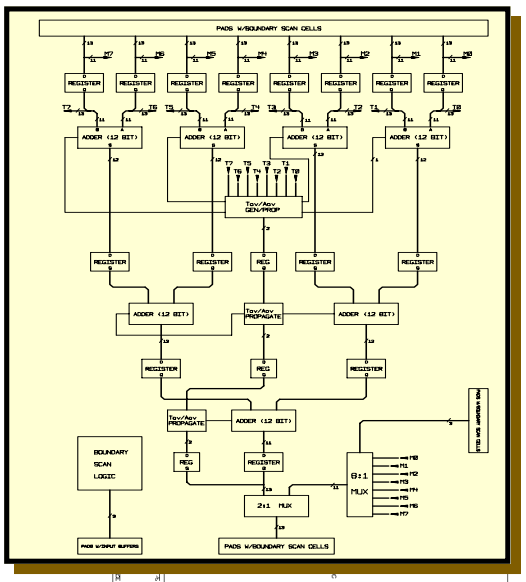
Quiet/MinI bits for each 4x4 region

Reserved space for Tau & Lumi

40 MHz output to global and muon systems

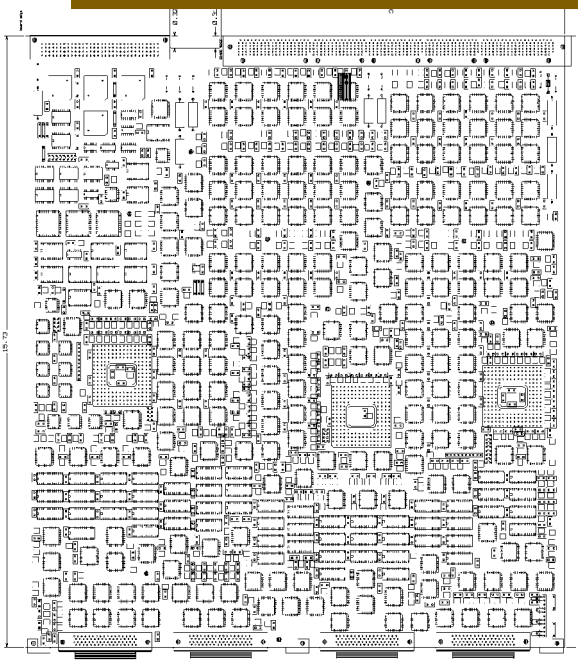
Calorimeter Trigger Status

13 x 8 bit Adder ASIC tested > 160 MHz



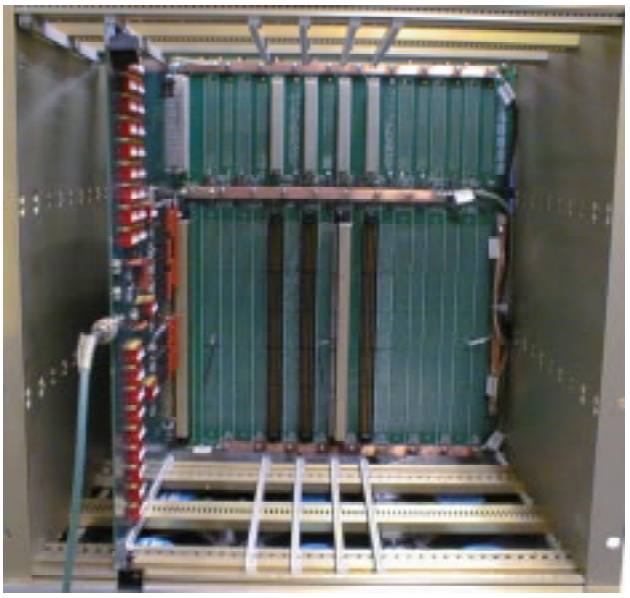
Receiver Card

- Designed for 160 MHz
- Being built



Backplane for VME & trigger data

- Prototype constructed
- Prototype Clock & Control Card built
- Signal performance excellent @ 160 MHz
- Confirmation of design feasibility



Receiver Card Prototype

Front side: Includes almost all features listed in the conceptual design.

Rear side: Serial input handling

- Change in calorimeter electronics location enabled consideration of copper links for transmission btw. calorimeter electronics & level-1 trigger crates in control room.
- Change in receiver card prototype to include feasibility study of Vitesse 7214 communication chips & associated copper cable plant.
- To retain flexibility with testing and to separate data link revisions from the rest of the receiver card, the data link circuitry placed on daughter cards.
- Since special test circuitry has been removed from the final Receiver Card, it is placed on a separate Test Card which the daughter cards also plug into.

Receiver card status

Front (Bkpl. I/O & Adder ASIC tests)

- **Submitted for Manufacture**

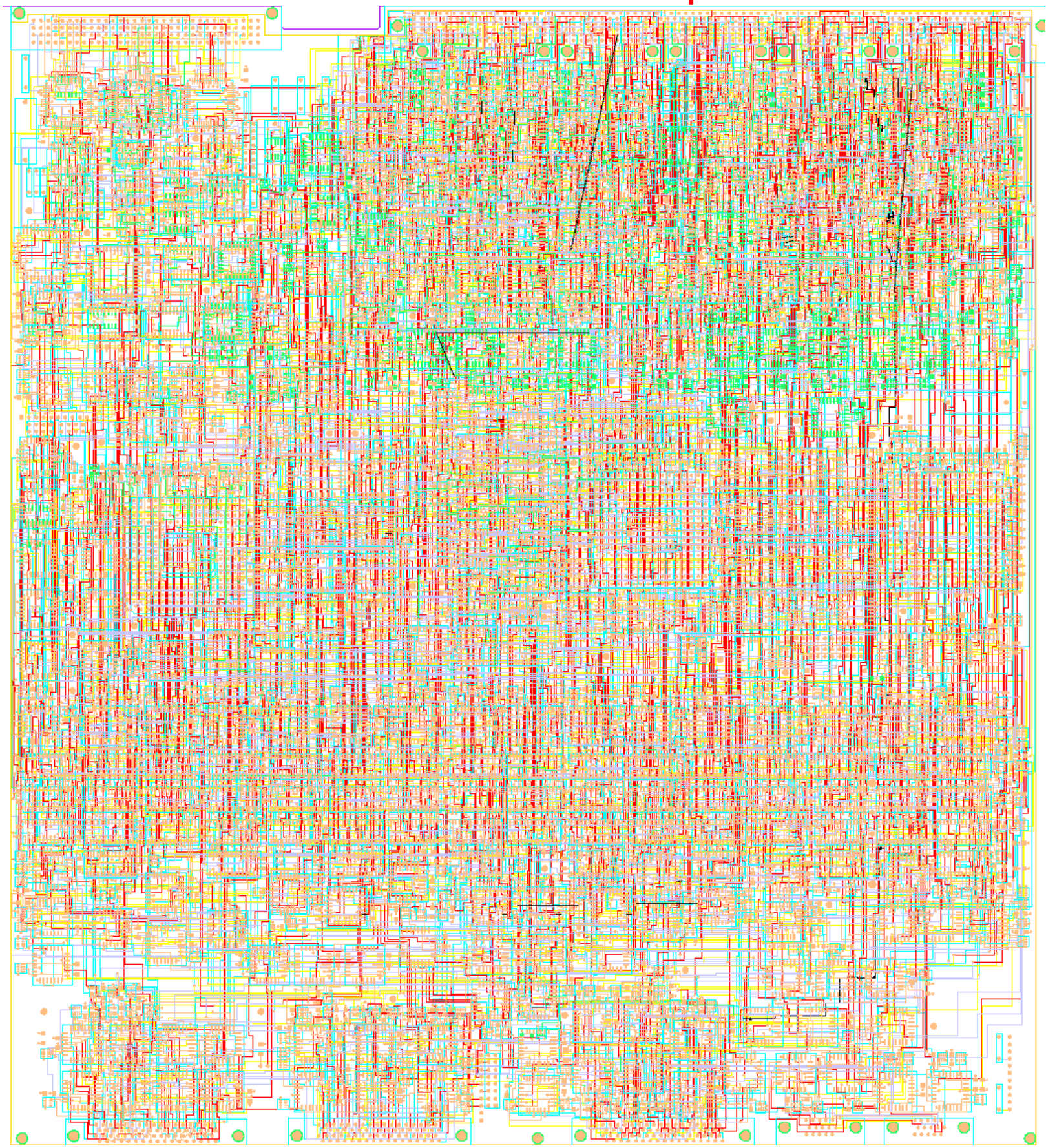
Rear (Serial copper connection test)

- **Equalization network designed & simulated for 20m cable**
  - Circuit is placed on a daughter card
- **Evaluation circuit for the Vitesse 7214 chip is designed and laid out**
  - Testing circuit is moved to a "Test Card"
  - Initiates synchronization & data streams from the transmitter & recognizes them at receiver.
  - Test memories at 120 MHz: 8-bit x 3 @ 40MHz.
  - Captures the data at 120 MHz and compares, on the fly, w/data in a buffer on board.
  - Stores received data & interrupts on error.
- **Input Circuitry on Daughter Card**
  - Layout finished...ready for manufacture
    - (see transp.)
- **Test Circuitry on separate test card**
  - Daughter Cards also plug into this card
  - Test Card is in layout

Receiver Card Layout

VME Connector

AMP Stripline Connector

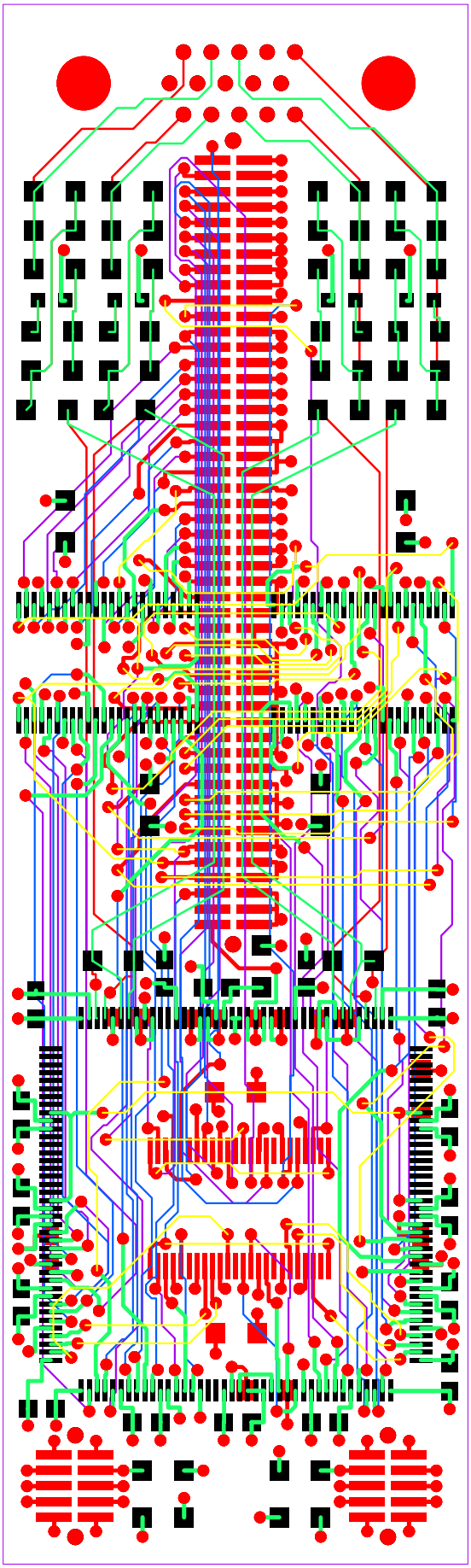


Inter-Crate Communication Connectors

Receiver Daughter Card

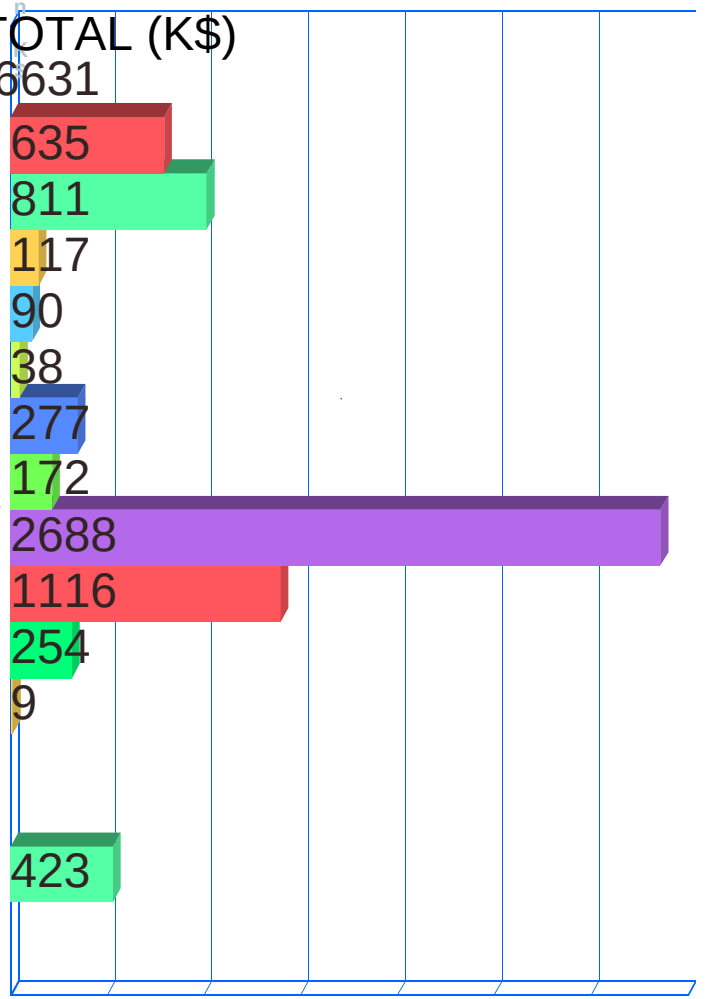
Layout Complete

Will hold for test card design and then submit both



Calorimeter Trig. Costs at L4

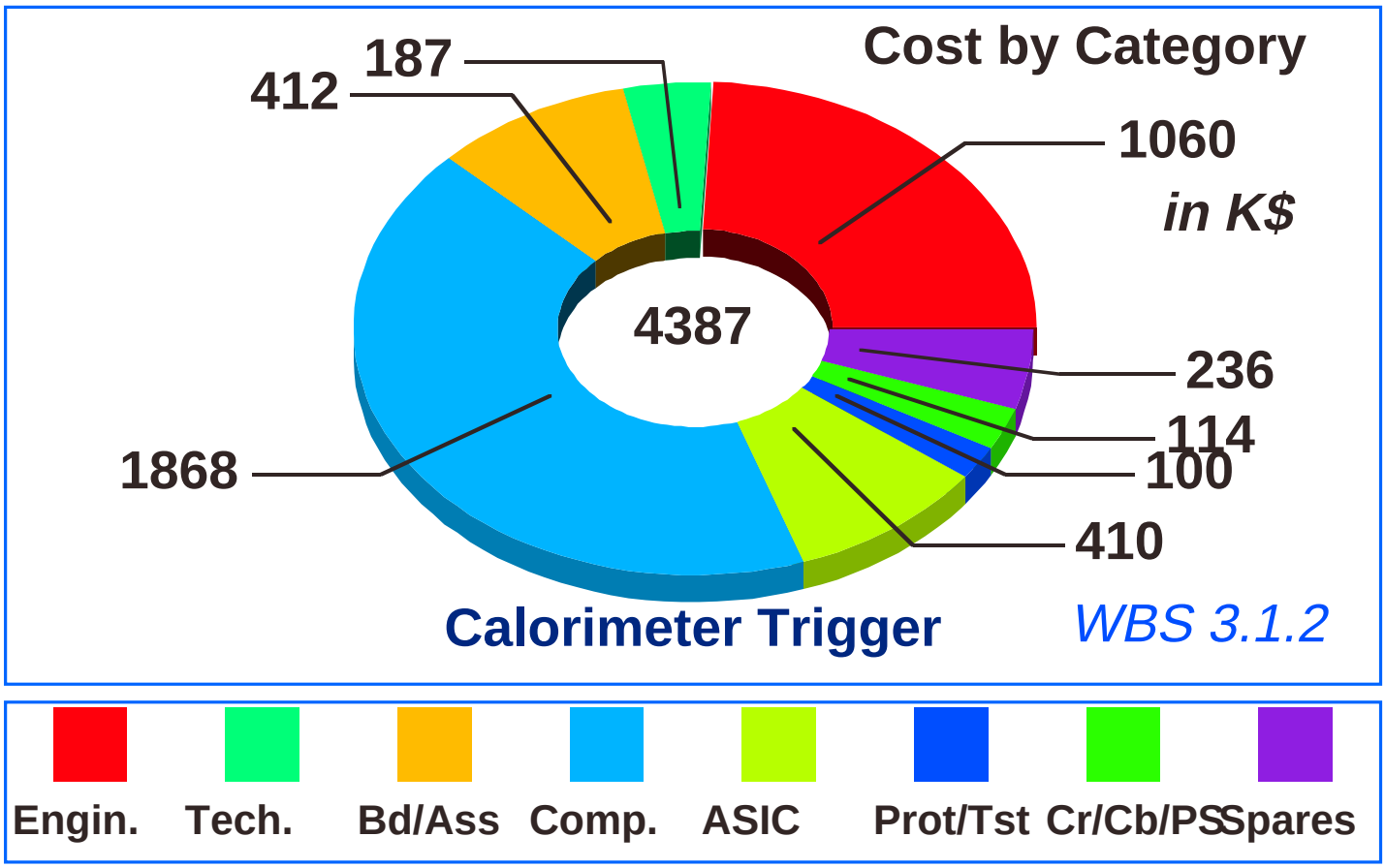
WBS	ITEM	BASE(K$)	Cont(%)	TOTAL (K$)
3.1.2	Cal.Regional Trigger	4,388	51	6631
3.1.2.1	Prototypes	441	44	635
3.1.2.2	Preproduction ASICs	553	47	811
3.1.2.3	Test Facilities	78	50	117
3.1.2.4	Power Supplies	82	10	90
3.1.2.5	Crates	35	10	38
3.1.2.6	Backplane	194	43	277
3.1.2.7	Clock & Control Card	132	30	172
3.1.2.8	Receiver Card	1,670	61	2688
3.1.2.9	Electron ID Card	744	50	1116
3.1.2.10	Jet Summary Card	170	50	254
3.1.2.11	Cables	7	30	9
3.1.2.12	DAQ Processor			
3.1.2.13	Crate Monitor Card			
3.1.2.14	Trigger Tests	282	50	423
3.1.2.15	Project Management			

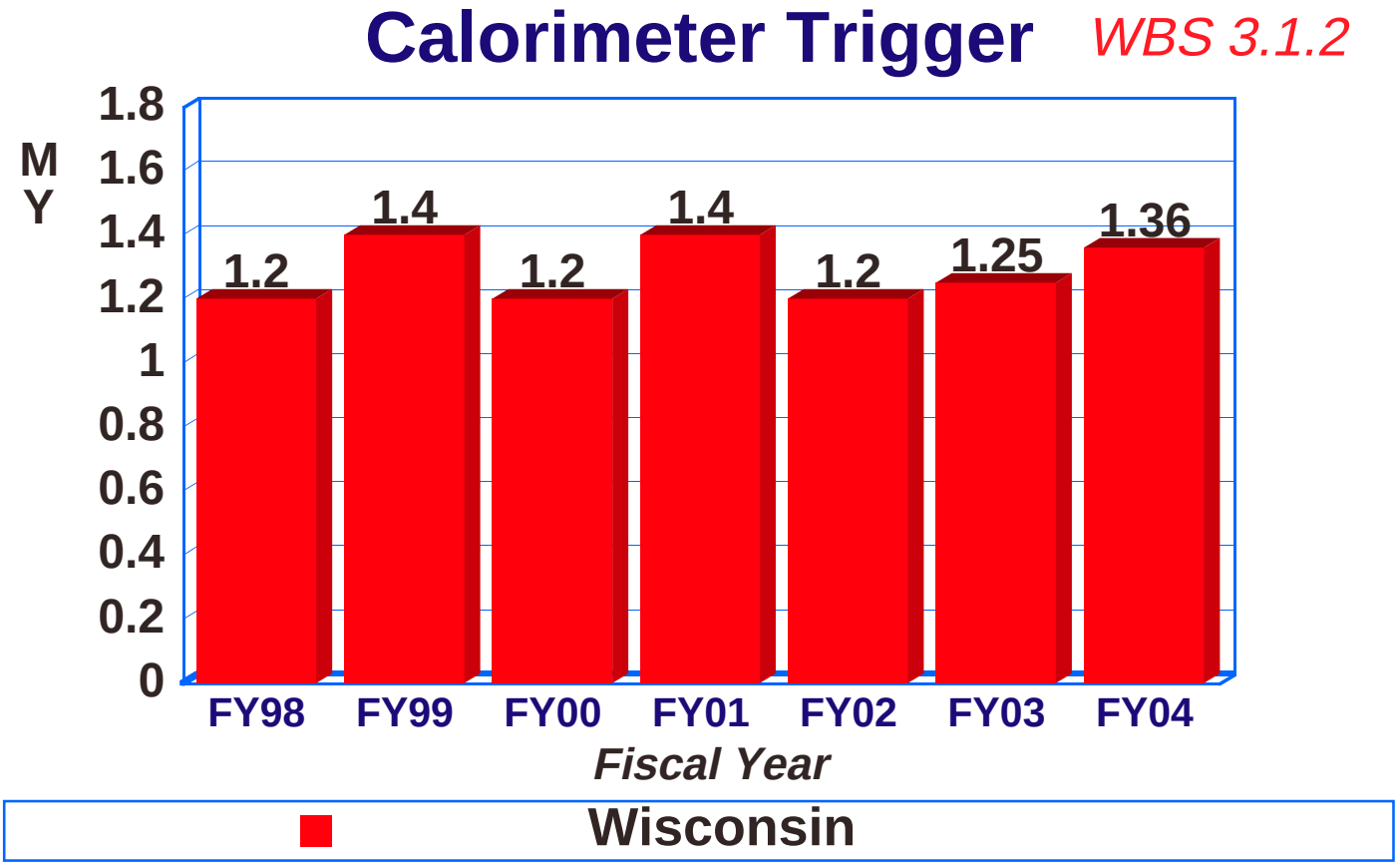


Changes since last May 1997 Review:

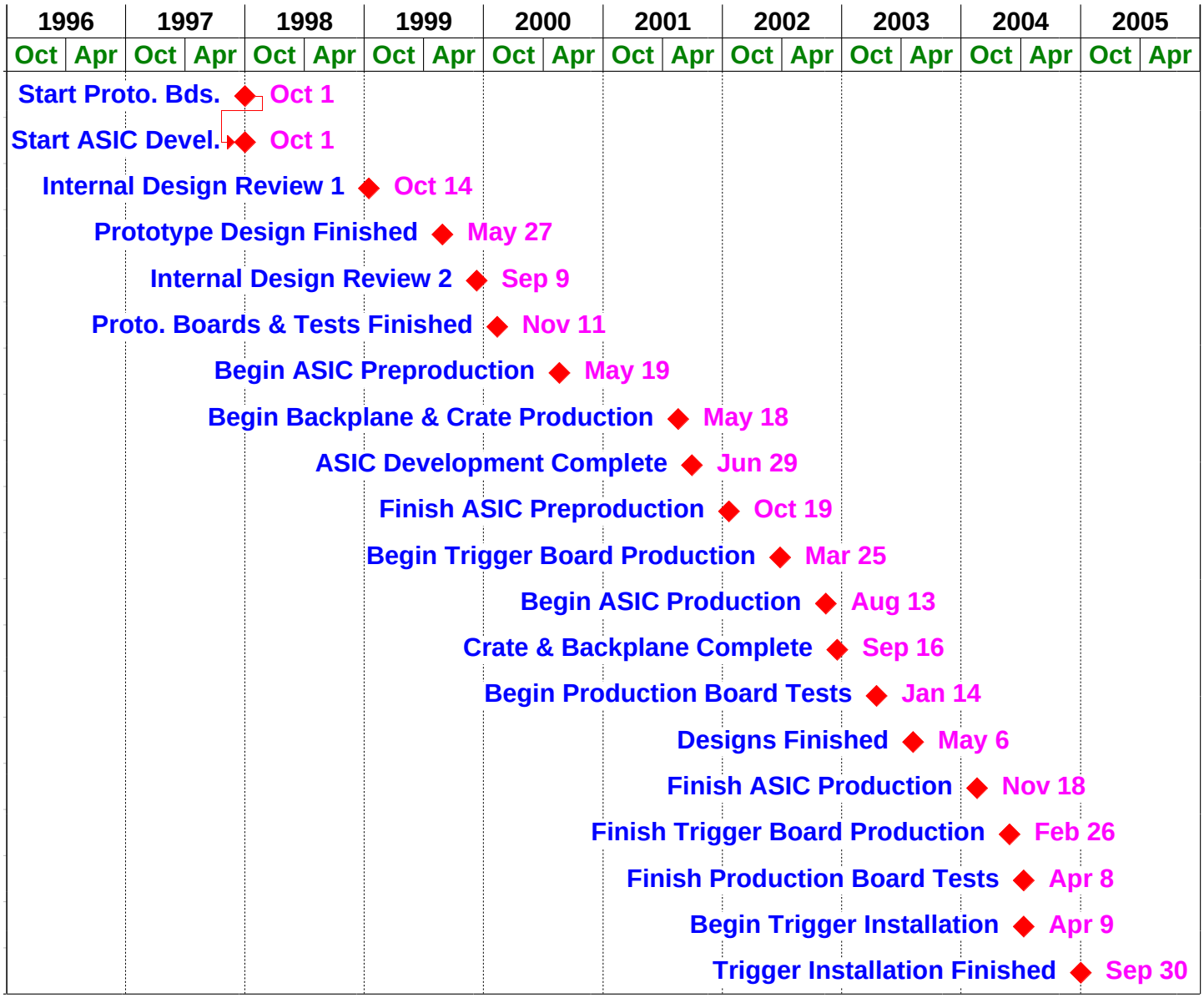
- Contingency analysis performed at lowest level (increased from 39->50%)
- Bottoms-up recosting & new WBS (no substantial *net* cost change)

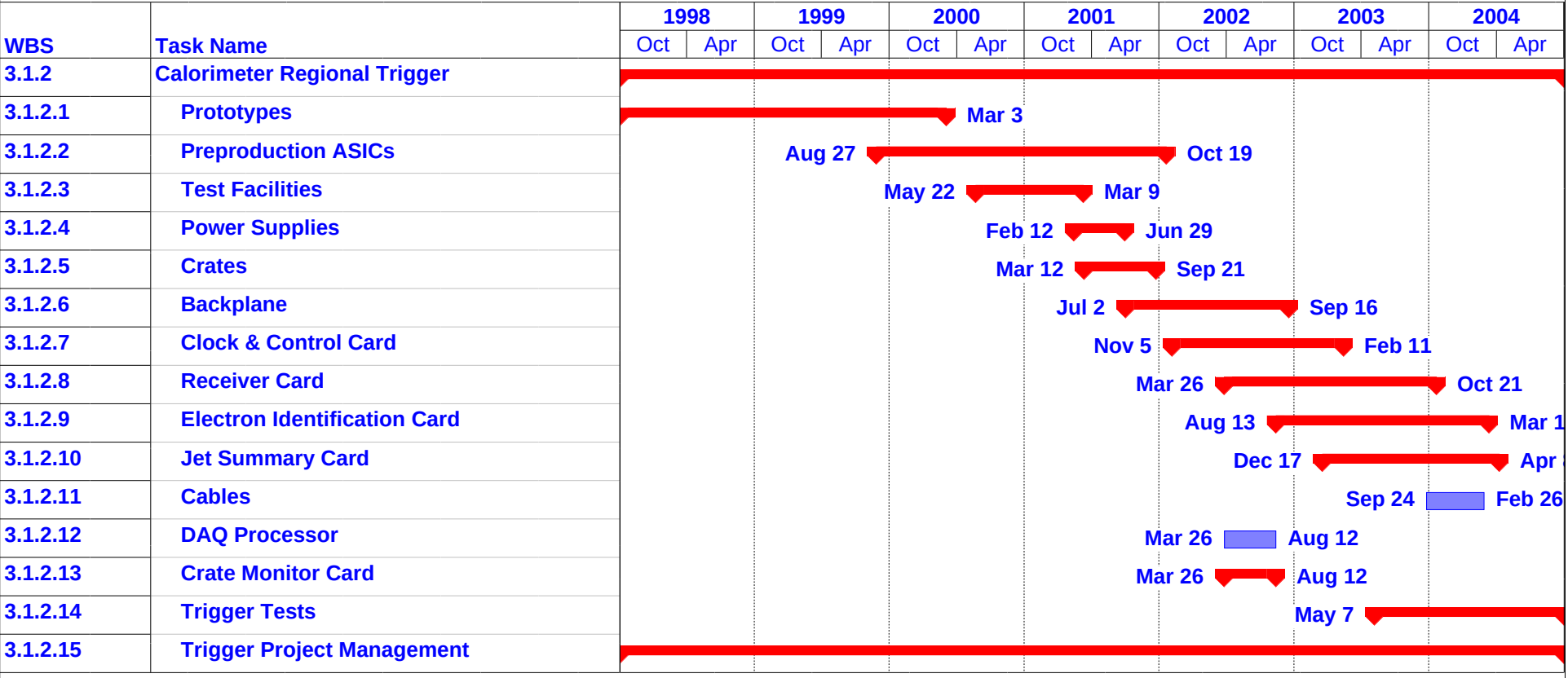
Cost Drivers & Peak Engineering

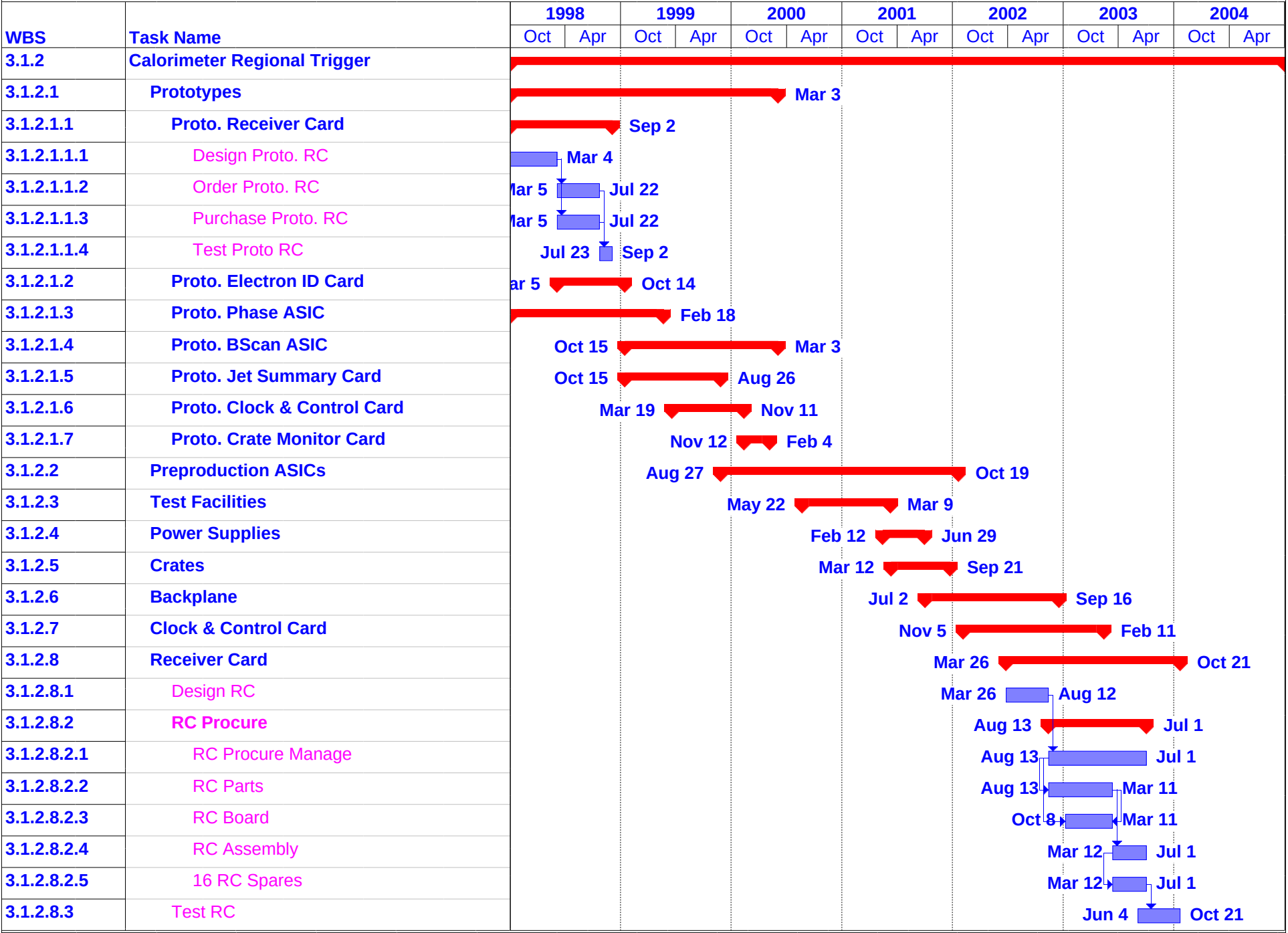




Cal. Trig. Schedule & Milestones




WBS
Task Name
1998
1999
2000
2001
2002
2003
2004
Oct
Apr
3.1.2
Calorimeter Regional Trigger
3.1.2.1
Prototypes
Mar 3
3.1.2.2
Preproduction ASICs
Aug 27
Oct 19
3.1.2.3
Test Facilities
May 22
Mar 9
3.1.2.4
Power Supplies
Feb 12
Jun 29
3.1.2.5
Crates
Mar 12
Sep 21
3.1.2.6
Backplane
Jul 2
Sep 16
3.1.2.7
Clock & Control Card
Nov 5
Feb 11
3.1.2.8
Receiver Card
Mar 26
Oct 21
3.1.2.9
Electron Identification Card
Aug 13
Mar 1
3.1.2.10
Jet Summary Card
Dec 17
Apr
3.1.2.11
Cables
Sep 24
Feb 26
3.1.2.12
DAQ Processor
Mar 26
Aug 12
3.1.2.13
Crate Monitor Card
Mar 26
Aug 12
3.1.2.14
Trigger Tests
May 7
3.1.2.15
Trigger Project Management


1998
1999
2000
2001
2002
2003
2004
Oct
Apr
WBS
Task Name
3.1.2 Calorimeter Regional Trigger
3.1.2.1 Prototypes
Mar 3
3.1.2.1.1 Proto. Receiver Card
Sep 2
3.1.2.1.1.1 Design Proto. RC
Mar 4
3.1.2.1.1.2 Order Proto. RC
Jul 22
3.1.2.1.1.3 Purchase Proto. RC
Jul 22
3.1.2.1.1.4 Test Proto RC
Jul 23
Sep 2
3.1.2.1.2 Proto. Electron ID Card
Oct 14
3.1.2.1.3 Proto. Phase ASIC
Feb 18
3.1.2.1.4 Proto. BScan ASIC
Oct 15
Mar 3
3.1.2.1.5 Proto. Jet Summary Card
Oct 15
Aug 26
3.1.2.1.6 Proto. Clock & Control Card
Mar 19
Nov 11
3.1.2.1.7 Proto. Crate Monitor Card
Nov 12
Feb 4
3.1.2.2 Preproduction ASICs
Aug 27
Oct 19
3.1.2.3 Test Facilities
May 22
Mar 9
3.1.2.4 Power Supplies
Feb 12
Jun 29
3.1.2.5 Crates
Mar 12
Sep 21
3.1.2.6 Backplane
Jul 2
Sep 16
3.1.2.7 Clock & Control Card
Nov 5
Feb 11
3.1.2.8 Receiver Card
Mar 26
Oct 21
3.1.2.8.1 Design RC
Mar 26
Aug 12
3.1.2.8.2 RC Procure
Aug 13
Jul 1
3.1.2.8.2.1 RC Procure Manage
Aug 13
Jul 1
3.1.2.8.2.2 RC Parts
Aug 13
Mar 11
3.1.2.8.2.3 RC Board
Oct 8
Mar 11
3.1.2.8.2.4 RC Assembly
Mar 12
Jul 1
3.1.2.8.2.5 16 RC Spares
Mar 12
Jul 1
3.1.2.8.3 Test RC
Jun 4
Oct 21

Cal. Trig. Milest. & Integration

Prototype Design Finished	May '99
Proto. test w/ECAL Proto. Elect.	Jun '99
Proto. Boards & Tests Finished	Nov '99
Begin ASIC Preproduction	May '00
Proto. test w/HCAL Proto. Elect.	Jun '00
Begin Backplane & Crate Production	May '01
ASIC Development Complete	Jun '01
Finish ASIC Preproduction	Oct '01
Begin Trigger Board Production	Mar '02
Begin Tests w/Final ECAL Elect.	Jul '02
Begin ASIC Production	Aug '02
Begin Tests w/Final HCAL Elect.	Sep '02
Crate & Backplane Complete	Sep '02
Begin Production Board Tests	Jan '03
Designs Finished	May '03
Finish ASIC Production	Nov '03
Finish Trigger Board Production	Feb '04
Finish Production Board Tests	Apr '04
Begin Trigger Installation	Apr '04
Begin Final System tests w/E,HCAL	May '04
Trigger Installation Finished	Sep '04

New Cal. Trig. Milestones

Regional Trigger:

- **D220 - Nov '98**
  - Review of Prototype Tests
- **D250 - Nov '98**
  - Review of Prototype Integration
- **New - Feb '99**
  - Test of Prototype Clock Board
- **New - Aug '99**
- Delivery of Elec ID Pre-production ASIC

  New - Nov '99
  - Delivery of Adder Pre-production ASIC

Global Trigger:

- **New - Jul '98**
  - Prototype Sort ASIC Test Results
  - Begin Fast Link tests
- **New - Nov '98**
  - Design Final Sort ASIC
  - Choose Link Technology
  - Finalize Processing Requirements
- **New - Nov '99**
  - Test Pre-production Sort ASIC
  - Link Tests using final technology/pkg.
  - Complete GCT Design

1998/9 Cal. Trigger Plans

Full dataflow tests

- Receiver Card
- Backplane Prototype
- Pseudo Electron Isolation Card

Electron Isolation ASIC

- Design in Vitesse GaAs
- Produce Prototype

Prototype Jet Summary Board

- Trigger data summary generation
- Data transmission to global cal. trig.

Intercrate data transfer

- Second crate & backplane
- Test transmit/align techniques

1st Test w/Trigger Primitive Logic

Detailed Simulation

- Use full GEANT
- Check new calorimeter geometries

Conclusions

CMS Regional Calorimeter Trigger

- **Receiver Card**
  - Cu copper serial receiver on daughter cards
  - Use of Vitesse 7214 Receiver Chip
  - Being Manufactured
- **Receiver Daughter Card**
  - Layout finished
- **New Test Card**
  - Will use daughter cards with dedicated test circuit
  - In Layout
- **Plans**
  - Dataflow test with Receiver Card
  - Data transmission test with daughter & test cards
- **Cost & schedule**
  - Well developed