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CMS Trigger Project Manager

*Presentation to PMG*

July 19, 1999
Cal. Trigger Dataflow Test

Prototype Crate with

- 160 MHz Backplane
- Proto. Receiver Card (rear)
- Proto. Clock Card (front)
- Proto. Electron ID Card (front)
Status as of January

• Vitesse investigating outsourcing ASIC development
  • Vitesse declined to bid on the Electron ID ASIC
• We were holding other ASIC designs (alt. vendors):
  • Phase ASIC, BSCAN ASIC, Sort ASIC

Status as of July

• Adder ASIC prototype fully tested
  • No revision required
• Purchase order for production of Adder ASICs awarded to Vitesse
• Designs of all ASICs submitted to Vitesse
• Vitesse has bid and been awarded PO's for all ASICs:
  • Electron ID, Phase, BSCAN, Sort ASICs
• Engineering work with Vitesse starts
Calorimeter Trigger Plans

Ongoing Dataflow Tests - Jul '99
- 160 MHz Backplane
- Proto. Receiver Card
- Proto. Clock Card
- Proto. Electron ID Card

Serial Data Tests - Oct '99
- Serial Link Test Card

ASIC Prototypes - Mar '00
- Electron ID ASIC
- Phase ASIC
- Boundary Scan ASIC
- Sort ASIC

Crate Test - Jun '00
- 160 MHz Backplane
- Proto. Receiver Card
- Proto. Clock Card
- Proto. Electron ID Card
- Proto. Jet Summary Card
Muon Trigger Detector Status

← Trigger Motherboard. Prototype is built and at FNAL for test

Clock Board. Prototype is built & at FNAL

Optical part of Muon Port Card

RICE
Sector Receiver Prototype

Status:

- Prelim. card layout done
- Backplane layout finalized
- Approval of preliminary design at March 25, 26 Review
- Need definition of readout, SP interface

UCLA
Sector Processor Design

**Status:**
- Mar 25 Review: Conceptual design accepted
- Track Assembler RAM designed
- Recently: Merge SP-CSC & SP-OVR
- Next Review July 27,28 @ FNAL

-- U. Florida
Simplifications to Sector Processor Logic

Don’t select best extrapolations, remove 12 LUTs

• Reduces chip count
• Shortens latency
• Merges overlap and endcap processors
• Reduces output to Muon Sorter from 72 to 36 muons

26*9 = 234
EU1
ME1*-ME2
ME1*-ME3
ME2-ME3
9*2+9*2+9 = 45

26*9 = 234
EU2
ME1**-ME2
ME1**-ME3
ME2-ME3
9*2+9*2+9 = 45

26*9 = 234
EU3
ME2-ME3
ME2-ME4
ME3-ME4
9+9+9 = 27

TAU1

Link 21
6*2+3+3 = 18
15

Link 22
6*2+3+3 = 18
15

Link 23
6*2+3+3 = 18
15

TAU2

Link 31
6*2+3+3 = 18
15

Link 32
6*2+3+3 = 18
15

Link 33
6*2+3+3 = 18
15

256K x 16 LUTs

9*15 = 135

Final Selection Unit

Only 1 bit quality for 2-3, 2-4, 3-4

Don’t select best extrapolations, remove 12 LUTs

Allow only one track per Link hit, remove Selection Unit and MUX

TFU must sort all 9 tracks to 3 from Endcap region logic and overlap logic

University of Florida
Muon Trigger Plans

Muon Port Card - Rice
- Construct Prototype - Sep '99
- Test with Sector Receiver - Dec '99
- Test with Trigger Motherboard - Mar '00

Sector Receiver - UCLA
- Construct Prototype - Oct '99
- Test with Muon Port Card - Dec '99

Sector Processor - Florida
- Prototype Design Review - Jul 27,28 '99 ❯
- Construct CSC Prototype - Oct '99
- Construct OVR Prototype - Dec '99

Crate Test - Jun '00
- Sector Receiver Prototype - UCLA
- Sector Process. CSC & OVR Proto - Florida
- Backplane - UCLA
- Clock & Control Card - Rice