

HF All Bits Timing Test: JSC Number _____

Setup: A RCT crate with a Jet/Summary Card (JSC) and a Receiver Card (RC) in Slot 0 with a Receiver Mezzanine Card (RMC) in the first HCAL position (second from the top) and third HCAL position (sixth from the top). A VME crate with one STC card and a 20 m cable from the transmit mezzanine card to the first RMC on the RC. Initialize the RCT crate.

1. Zero the memories: **rctCrateTest -t 1**
2. To setup the JSC and RC enter vmedia for the RCT and type:
 - a. RCT: vmedia> poke 1 19000000 84 (04 for JSC REVB)
 - b. RCT: vmedia> read jsc_hf_allbits.txt
3. To do the first cycle checks run the STC as follows:
 - a. STC: vmedia> read aa.txt
 - b. STC: vmedia> resett
 - c. STC: vmedia> read stc_jsc_hf_allbits.txt
 - d. STC: vmedia> idlet
 - e. STC: vmedia> ready
4. Send a reset to the RCT system:
 - a. RCT: vmedia> resys
5. Start sending data:
 - a. STC: vmedia> datat
6. Trigger on connector J4 pin 37, there should be a pulse 12.5 ns wide. This pin is expected to be a “1” followed by a “0”. The next pin for HF 0 h 0,2 should be a “0” followed by a “1” in time, like the grey numbers in the table below. Check each bit, and its complement, on the pin below (e.g. for pin 37 that would be pin 38) and place a check mark over the grey numbers.

Bit	HF 0 η 0,2	Pattern Expected	HF 0 η 1,3	Pattern Expected	HF 1 η 0,2	Pattern Expected	HF 1 η 1,3	Pattern Expected
0	J4 pin 37	10	J4 pin 35	10	J3 pin 29	10	J3 pin 63	10
1	J3 pin 1	01	J3 pin 3	01	J3 pin 61	10	J3 pin 59	10
2	J3 pin 5	10	J3 pin 7	10	J3 pin 57	10	J3 pin 55	10
3	J3 pin 9	01	J3 pin 11	01	J3 pin 53	10	J3 pin 51	10
4	J3 pin 13	10	J3 pin 15	10	J3 pin 49	01	J3 pin 47	01
5	J3 pin 17	01	J3 pin 19	01	J3 pin 45	01	J3 pin 43	01
6	J3 pin 21	10	J3 pin 23	10	J3 pin 41	01	J3 pin 38	01
7	J3 pin 25	01	J3 pin 27	01	J3 pin 37	01	J3 pin 35	01
QB	J4 pin 45	10	J4 pin 43	10	J4 pin 41	10	J4 pin 39	10

Pattern out of the phase ASIC: (See the card document for STC channels)

