

## JSC HF Quality Bit Timing Test: JSC Number \_\_\_\_\_

**Setup:** A RCT crate with a Jet/Summary Card (JSC) with a Receiver Mezzanine Card (RMC) on board. A VME crate with one STC card and a 20 m cable from the transmit mezzanine card to the RMC on the JSC. Initialize the RCT Crate and zero the memories:  
**rctCrateTest -t 1**

1. To setup the JSC enter vmedia for the RCT and type:
  - a. RCT: vmedia> read jsc\_hf\_test\_qb.txt
1. To do the first cycle checks run the STC as follows:
  - a. STC: vmedia> read aa.txt
  - b. STC: vmedia> resett
  - c. STC: vmedia> read channelaabbccdd\_x0\_fg10.txt
  - d. STC: vmedia> idlet
  - e. STC: vmedia> ready
2. Send a reset to the RCT system:
  - a. RCT: vmedia> resys
3. Start sending data:
  - a. STC: vmedia> datat
4. Trigger on connector J4 pin 37, there should be a pulse 25ns wide. The quality bit (QB) should arrive with the leading edge this pulse (first 12.5 ns cycle):

QB	Connector:Pin	Okay?
HF 0 $\eta_0, \eta_2$	J4:45	
HF 0 $\eta_1, \eta_3$	J4:43	
HF 1 $\eta_0, \eta_2$	J4:41	
HF 1 $\eta_1, \eta_3$	J4:39	

5. Idle the STC:
  - a. STC: vmedia> idlet
6. Then redo the above sequence, replacing 2c with:
  - a. STC: vmedia> read channelaabbccdd\_x0\_fg01.txt
7. Then trigger on the same connector and pin: J4 pin 37. The quality bit (QB) should arrive with the falling edge of the pulse (second 12.5 ns cycle):

QB	Connector:Pin	Okay?
HF 0 $\eta_0, \eta_2$	J4:45	
HF 0 $\eta_1, \eta_3$	J4:43	
HF 1 $\eta_0, \eta_2$	J4:41	
HF 1 $\eta_1, \eta_3$	J4:39	

## JSC HCAL MIP Bit Timing Test: JSC Number \_\_\_\_\_

**Setup:** A RCT crate with a Jet/Summary Card (JSC) and a Receiver Card (RC) in Slot 0 with a Receiver Mezzanine Card (RMC) in the first HCAL position (second from the top) and third HCAL position (sixth from the top). A VME crate with one STC card and a 20 m cable from the transmit mezzanine card to the first RMC on the RC. Initialize the RCT crate.

1. Zero the memories: **rctCrateTest -t 1**
2. To setup the JSC and RC enter vmedia for the RCT and type:
  - a. RCT: vmedia> poke 1 19000000 84 (04 for JSC REVB)
  - b. RCT: vmedia> read jsc\_threshold\_1ff.txt
  - c. RCT: vmedia> read rc\_hcal\_qb\_test\_rc0\_r0.txt
3. To do the first cycle checks run the STC as follows:
  - a. STC: vmedia> read aa.txt
  - b. STC: vmedia> resett
  - c. STC: vmedia> read qb\_data\_long\_c1.txt
  - d. STC: vmedia> idlet
  - e. STC: vmedia> ready
4. Send a reset to the RCT system:
  - a. RCT: vmedia> resys
5. Start sending data:
  - a. STC: vmedia> datat
6. Trigger on the **Trigger** connector and pin, there should be a pulse 12.5 ns wide. The quality bit should arrive after the falling edge this pulse (12.5 ns long) on the JSC Mezzanine card connector and pin given in the table.
7. Repeat step 2d and move the cable to the lower RMC. Load a new file for the RC:
  - a. RCT: vmedia> read rc\_hcal\_qb\_test\_rc0\_r1.txt
8. Then repeat steps 2e to 4a.
9. Trigger on the **Trigger** connector and pin, there should be a pulse 12.5 ns wide. The quality bit should arrive in time with this pulse on the JSC Mezzanine card connector and pin given in the table.
10. Shutdown the RCT crate and move the RC to the next slot. Repeat from Step 1, replacing the `_rc0_` in the name of the vmedia files to `_rc1_`, `_rc2_`, etc.

RC	Trigger	QB R0 pin	Okay?	QB R1 pin	Okay?
0	J5 pin 1	ISO-E pin 45		ISO-E pin 47	
1	J5 pin 25	ISO-E pin 49		ISO-E pin 51	
2	J5 pin 45	ISO-E pin 53		ISO-E pin 55	
3	J6 pin 13	ISO-E pin 57		ISO-E pin 59	
4	J6 pin 57	NISO-E pin 45		NISO-E pin 47	
5	J4 pin 1	NISO-E pin 49		NISO-E pin 51	
6	J4 pin 25	NISO-E pin 53		NISO-E pin 45	