

STC to JSC Link Tests: Card Number _____

Setup: A RCT crate with a Jet/Summary Card (JSC) with a Receiver Mezzanine Card (RMC) on board. A VME crate with one STC card and a 20 m cable from the transmit mezzanine card to the RMC on the JSC.

Initialization: Power up both crates. Open two terminal windows on the PC, logging in remotely to another host if necessary to operate the SBS or RCT. Use one window for running vmedia in the subdirectory vmediaSTC for the STC, and one window should be in the subdirectory RCTvmedia for the JSC. Before starting the RCT vmedia session, type rctBoot and then “b” and then type exit to return to the shell prompt. In the following “STC” is vmedia for the STC crate, and “RCT” is vmedia for the RCT crate.

1. To setup the JSC enter vmedia and type:
 - a. RCT: vmedia> read linktest_jsc.txt
 - b. Which is equivalent to:
 - i. RCT: vmedia> poke 1 19000000 84
 - ii. RCT: vmedia> poke 1 19000002 00
 - iii. RCT: vmedia> poke 1 19000002 ff
 - iv. RCT: vmedia> poke 1 19000002 00
 - v. RCT: vmedia> poke 1 19000006 e00
2. To do the first checks run the STC (base address c10000) with incremental data:
 - a. STC: vmedia> read aa.txt
 - b. STC: vmedia> resett
 - c. STC: vmedia> read inc_long_error_c1.txt
 - d. STC: vmedia> idlet
 - e. STC: vmedia> ready
3. Send a reset to the RCT system:
 - a. RCT: vmedia> resys
4. Start sending data:
 - a. STC: vmedia> datat
5. To check the Compare Phase
 - a. RCT: vmedia> dump 1 19000002 (several times)
 - b. The bit (hex) 0010 shows the CMP_PHS bit for the Phase ASIC on the board. This only works if a link is attached and running. Please repeat the dump several times to be certain it stays at zero, because it may change! If this bit stays zero, put a check in the Compare Phase box for that ASIC below. If it doesn't stay zero, CMP_PHS was probably not set up correctly for this configuration. This will have to be done before link can be checked. Please report this and stop testing.
4. Probe on the JSC to check the patterns for all bits

- a. Trigger on the error to see the patterns. Component U250, pin 26 (Schematic D0852 – SELCT_ERR) will have the error bit for the Phase ASIC. You should only see one error bit. If you see more, stop the STC and repeat steps 2d to 4a again. If you cannot seem to clear errors after several repetitions of these steps, start from step 2b. The patterns are easily seen in ECL on the translators at the data output of the Phase ASIC (D0824 – HF_RCVR). The quality bits can be seen on U240 pin 3 and pin 7 (D0827 – MEM). If the data checks out okay for the Phase ASIC. Check BX0 at U249 pin 24 (D0852 – SELCT_ERR).
5. Double-check the EDC and Check the Zero Data
 - a. There is no switch on the JSC to change the EDC interpretation (it is jumpered instead). To test this, go through steps 2b to 4a again and load the vmedia script **random_long_odd.txt** into the memory of the STC instead of the increment pattern. This should send the error bits to “high” levels and zero all the data instantly. Probe at the U250 pin 26 to find the error bit and check a few of the data bits.

Checklist:

Phase ASIC	Compare Phase	Data: 16 bits	QB: 2 bits	BX0	EDC	Zero Data
JSC						