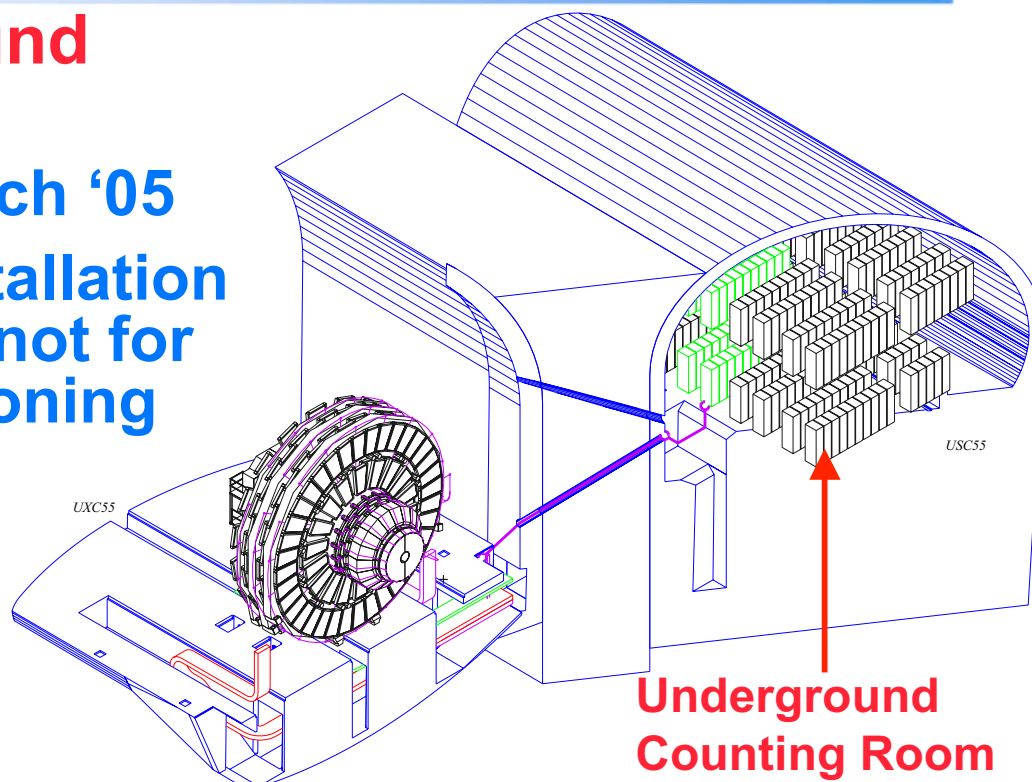


Slice Test & Trigger Completion

Installation in Underground Counting Room

- Expect access by March '05
- Sufficient time for installation and some testing but not for completing commissioning with detectors



Slice Test (on surface)

With both HCAL and EMU

Verify trigger functions and interfaces by testing with detectors on surface at CERN.

Suggest as substitute for commissioning completion step.

Will check as much on surface before gaining access to underground facilities.

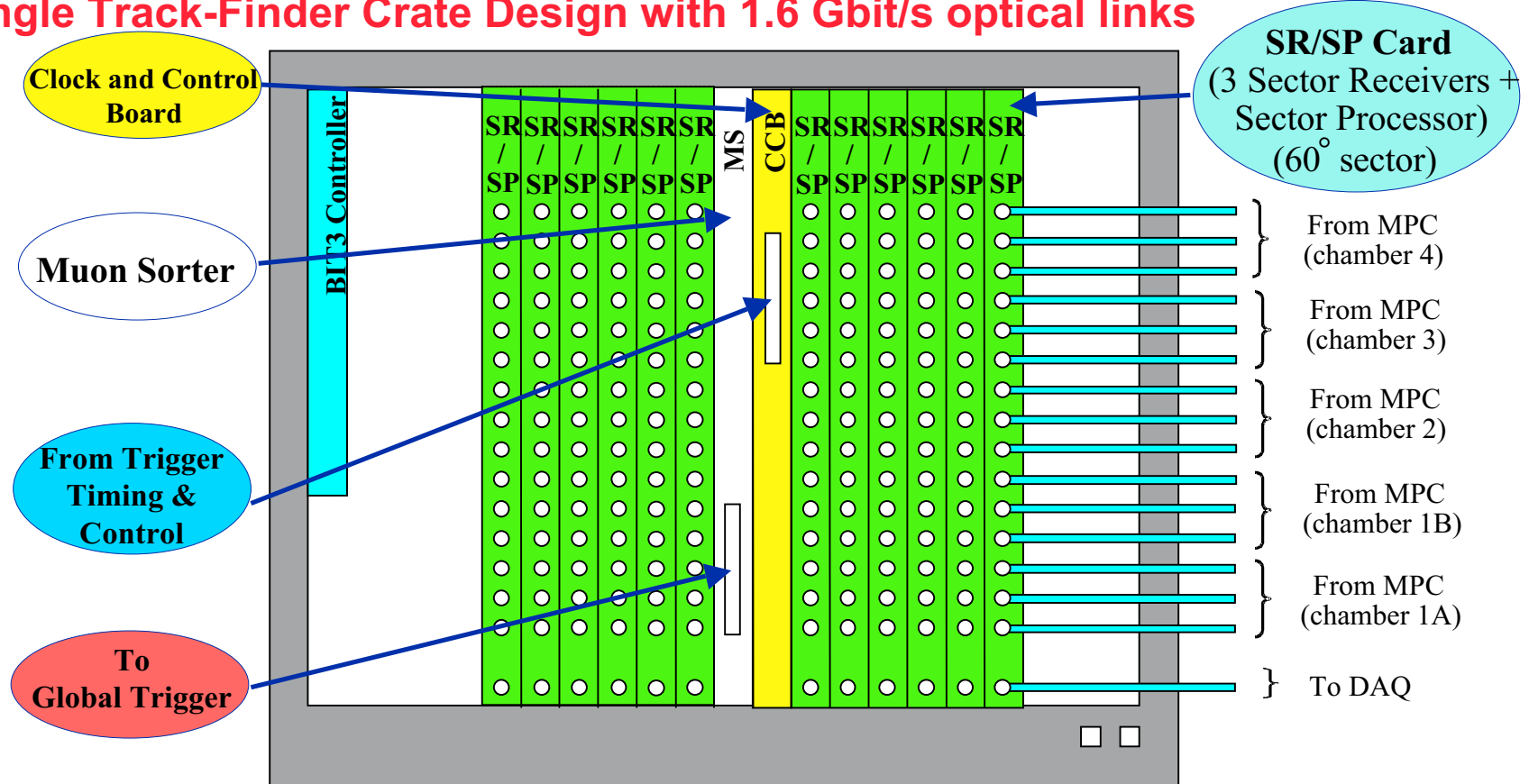
Planned for October '04 - March '05



Ingredients for Slice Test

(whole system is one crate)

Single Track-Finder Crate Design with 1.6 Gbit/s optical links



- Reduces processing time from 525 ns (old design) to 175 ns
 - Total Latency ~ 20 Bx (from input of SR/SP card to output of MS card)
- Crate Power Consumption ~ 500 W • 15 Optical connections per SR/SP card
- Custom Backplane for SR/SP ↔ CCB and MS connection



CSC Trigger Slice Test

Requirements for 3-station 20 degree slice test of 12 CSCs (w/2 ME1/1):

- Need: 3 MPC, 1 SP/SR, 1 CCB module, 1 backplane
- Integrate w/3 partially populated peripheral crates + 1 DDU

Schedule:

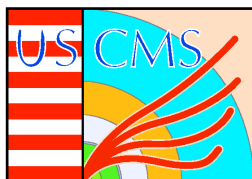
- Apr-02 Prototype 2 designs done
- Nov-02 Prototype 2 construction done
- Apr-03 Prototype 2 testing done
- Sep-03 Final designs done
- CSC Sorter module: only 1, design by Jan-04
 - Not needed for Slice Test I: use trigger output from CCB
- Oct-04 Production done
- Mar-05 Installation begins in USC55

Slice Test Phase I

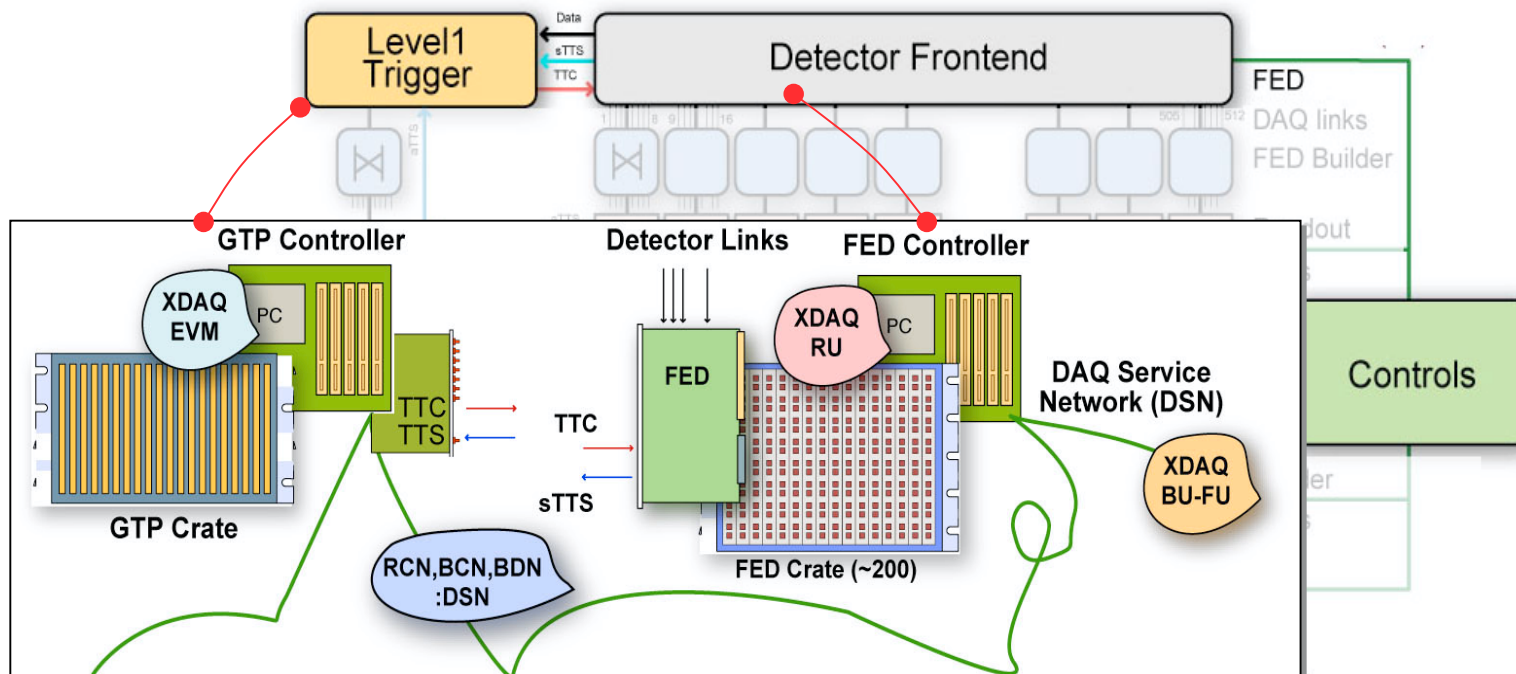
- Oct-03 to Oct-04
- Use Prototype 2 modules

Slice Test Phase II:

- Oct-04 to Mar-05
- Use Production Modules (& Proto. Sorter)



Slice Test DAQ (10-100 Hz)



Trigger system
 Detector readout
 Readout Units
 Data to Surface
 RCN, BCN, BDN networks
 Event manager
 Builder/Filter Units
 Performances

GTP, TTC and sTTS

Complete **FED crate systems** (FED-TTC-TTS, Controller CPU+DSN)
 XDAQ **RU-VME-tasks** running in all the **FED controllers**
 None just the **FED-VME bus** of FED crates
 DAQ Service Network (**DSN** e.g. GEthernet)
 XDAQ **EVM-task** running in the **GTP controller**
 XDAQ BU-task running in **any DSN(WAN) CPU**
Few 10 Hz (up to 100s when using GE switches in DSN as EVB)