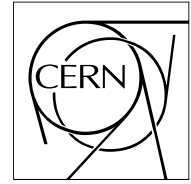


The Compact Muon Solenoid Experiment

CMS Note

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CMS Calorimeter Level 1 Regional Trigger Conceptual Design

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Abstract

The CMS level-1 calorimeter trigger electronics is designed to identify signatures for high-energy electrons, photons, neutrinos and jets. The calorimeter regional trigger system receives and processes digital serial data transmitted from the nearby calorimeter readout electronics on copper cables. This system consists of 19 calorimeter processor crates covering the full calorimeter. Eighteen crates are dedicated to the barrel and two endcaps. The remaining crate covers both forward calorimeters. Each calorimeter regional crate transmits to the calorimeter global trigger processor its sum E_t , E_x and E_y . It also sends its 4 highest-ranked isolated and non-isolated electrons and 4 highest energy jets along with information about their location. The global calorimeter trigger then sums the energies and sorts the electrons and jets and forwards the top four calorimeter-wide isolated and non-isolated electrons and jets, as well as the total calorimeter missing and sum E_t to the CMS global trigger.

Preliminary version

1 Introduction

1.1 CMS Trigger Overview

The CMS trigger and data acquisition system is designed to operate at the nominal LHC design luminosity of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, where an average of 20 inelastic events occur at the beam crossing frequency of 40 MHz. This input rate of 10^9 interactions every second must be reduced by a factor of at least 10^7 to 100 Hz, the maximum rate that can be archived by the on-line computer farm. The CMS trigger system must carefully sift the 40 MHz data to retain only interesting physics signals at a 75 Hz level while discarding the well-known QCD background. The CMS trigger is implemented in two physical levels, one based on custom electronics and the other relying upon commercial processors. The level-1 system uses only coarsely segmented data from calorimeter and muon detectors, while holding all the high-resolution data in pipeline memories in the front-end electronics, to produce a trigger decision in 3 μs . Level-1 triggered events at a 75 kHz rate are sifted further in higher levels of triggers implemented as software filters.

1.2 Level 1 Calorimeter Trigger System Function

The CMS level 1 trigger decision is based in part upon local information from the level 1 calorimeter trigger about the presence of physics objects such as photons, electrons, and jets, as well as global sums of E_T and missing E_T (to find neutrinos) [1]. The calorimeter trigger system provides triggers based upon the energy profiles left in the CMS calorimeter by these electrons, photons, jets and non-interacting particles in the interesting events. It also provides additional information for the muon trigger system for isolation and minimum ionization signal identification. Each of the objects, such as electrons, muons and jets, are required to pass a series of p_t or E_t thresholds, which are used in making the Level 1 Trigger Decision.

1.3 Input Data

The calorimeter level 1 trigger system baseline design receives digital trigger sums via copper links from the front-end electronics system in the electronics counting house. The data includes energy on an eight bit compressed non-linear scale and a fine grain ID bit determined from the data used to make the energy sums. The compressed scale of the trigger tower data will be derived from memory lookup tables within the front-end system. Programmable tables will enable full flexibility to modify the compression algorithm as required. The Trigger system will use memory lookup tables to decode the 8-bit compressed scale data into a linear scale with a 10 bit dynamic range in the adder tree. The data for two HCAL or ECAL trigger towers for the same crossing will be sent on a single copper serial link in eighteen total bits accompanied by five bits of error detection. One additional bit is used to set the link into either control or data modes.

For most of the CMS ECAL, a 5 x 5 array of PbWO4 crystals is mapped into trigger towers. In the rest of the ECAL there is somewhat lower granularity of crystals within a trigger tower. There is a 1:1 correspondence between the HCAL and ECAL trigger towers. The trigger tower size is equivalent to the HCAL physical towers, .087 x .087 in η x ϕ . The ϕ size remains constant in $\Delta\phi$ and the η size remains constant in $\Delta\eta$ out to an η of 2.262, beyond which the η size increases. Where the HCAL is no longer able to maintain the $\Delta\phi$ granularity, the output sums will be doubled, carrying the same information, so that the pattern logic can be preserved. Figure 1 shows the η x ϕ mapping of the calorimeter trigger towers onto a single regional trigger crate with 8 receiver cards. Figure 2 shows the mapping of the Calorimeter η towers into calorimeter trigger towers. Table 1 shows the input data to the calorimeter level 1 regional trigger system.

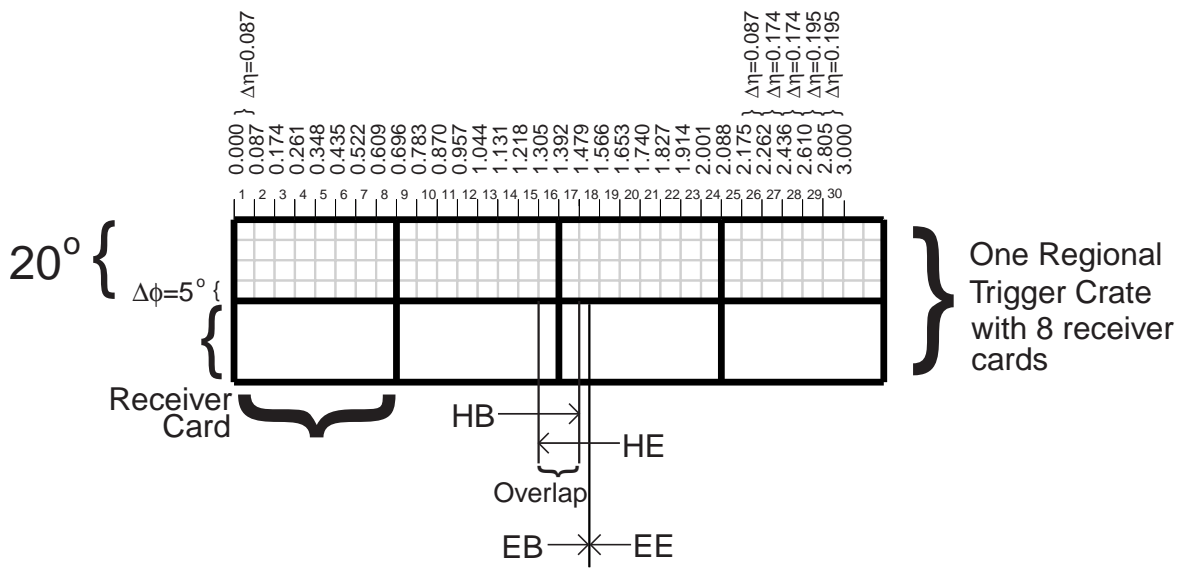


Figure 1. Mapping of calorimeter trigger towers onto the Receiver Cards in one of the 18 Regional Trigger Crates.

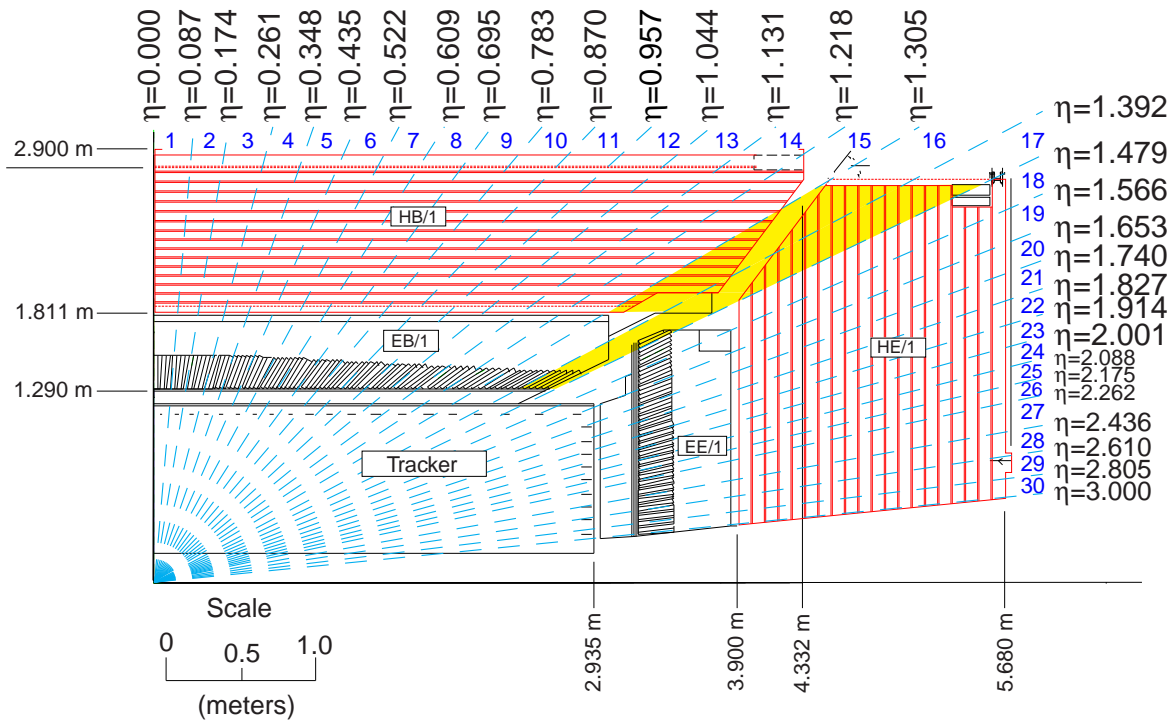


Figure 2. Mapping of Calorimeter η towers into calorimeter trigger towers.

Calorimeter	Input Segmentation/half	$\Delta\eta \times \Delta\phi$	Input Level 1 Data
ECAL ($0 < \eta < 2.262$)	$72 \phi \times 26 \eta$	$.087 \times .087$	8 bits energy 1 bit fine grain
HCAL ($0 < \eta < 2.262$)	$72 \phi \times 26 \eta$	$.087 \times .087$	8 bits energy 1 bit HCAL feature
ECAL ($2.262 < \eta < 2.610$)	$72 \phi \times 2 \eta$	$.174 \times .087$	8 bits energy 1 bit fine grain
HCAL ($2.262 < \eta < 2.610$)	$36 \phi \times 2 \eta$ (ϕ data doubled)	$.174 \times .087$	8 bits energy 1 bit HCAL feature
ECAL ($2.61 < \eta < 3.0$)	$72 \phi \times 2 \eta$	$.195 \times .087$	8 bits energy
HCAL ($2.61 < \eta < 3.0$)	$36 \phi \times 2 \eta$ (ϕ data doubled)	$.195 \times .087$	8 bits energy 1 bit HCAL feature
VFCAL ($3.0 < \eta < 5.0$)	$12 \phi \times 12 \eta$	$.167 \times .523$	8 bits energy 1 bit jet tag

Table 1. Input Data to the Level 1 Regional Calorimeter Trigger.

1.4 Calorimeter Trigger Algorithms

The calorimeter trigger system provides electron/photon, jet, missing and total transverse energy triggers. The electron/photon algorithm is illustrated in the Figure 3. The data for this algorithm is composed of the trigger primitives generated by the ECAL and the HCAL front end electronics comprise of the 8-bit trigger tower transverse energy and a single bit characterizing the fine grain profile of the energy deposit within the trigger tower. The ECAL and HCAL trigger towers are expected to correspond to the same $\Delta\eta \times$ segments and to fully span the calorimeter coverage. The electron/photon algorithm is performed on the center of every trigger tower in the system. The candidate energy is determined by summing in leakage energy in the highest of its four nearest neighbors. The candidate is then characterized based on four distinct sub-algorithms which implement the cuts detailed below.

- *Fine Grain:* In the barrel region where there are up to 25 ECAL crystals per trigger tower arranged in a square configuration, the sum of E_T in η strips of towers are made because the energy spreads in the ϕ direction. The sum of energy in the neighboring η strips is compared to the total E_T in the trigger tower to set a fine grain profile bit.
- *HAC Veto:* The central HCAL and ECAL trigger tower E_T 's are compared to set a bit to veto non-EM deposits. Care is taken to set this HAC Veto bit only when the energies in the trigger towers are significantly above the noise floor.
- *Neighbor HAC Veto:* The HAC Veto bit, as defined above, is required to be set in all eight trigger towers surrounding the center tower being considered.
- *EM E_T Isolation:* The isolation of the electron in the ECAL itself is determined by requiring that at least one of the four corners surrounding the center tower have all five towers quiet. The isolation region is defined to be only a corner because we need to prevent self-veto of the electrons due to a possible leakage of energy to the nearest neighbor. We chose to simplify the algorithm by requiring only one of the four corners to be quiet, because there is no need to identify which of the corners is quiet.

The cut values in all four of these sub-algorithms are programmable in lookup tables. The fine grain portion of the algorithm illustrated in Figure 3 is implemented in the front-end electronics itself. The HAC veto, the neighbor HAC veto and the E_T isolation portions of the algorithm are implemented in the regional calorimeter trigger discussed here. The highest E_T candidate for each 4×4 region is selected. The fine grain feature ID bits for each trigger tower in this 4×4 region are OR'ed and tagged to the highest E_T candidate. These selected

candidates are then ranked using a look-up-table and sorted to find the top four isolated and non-isolated electron/photon candidates.

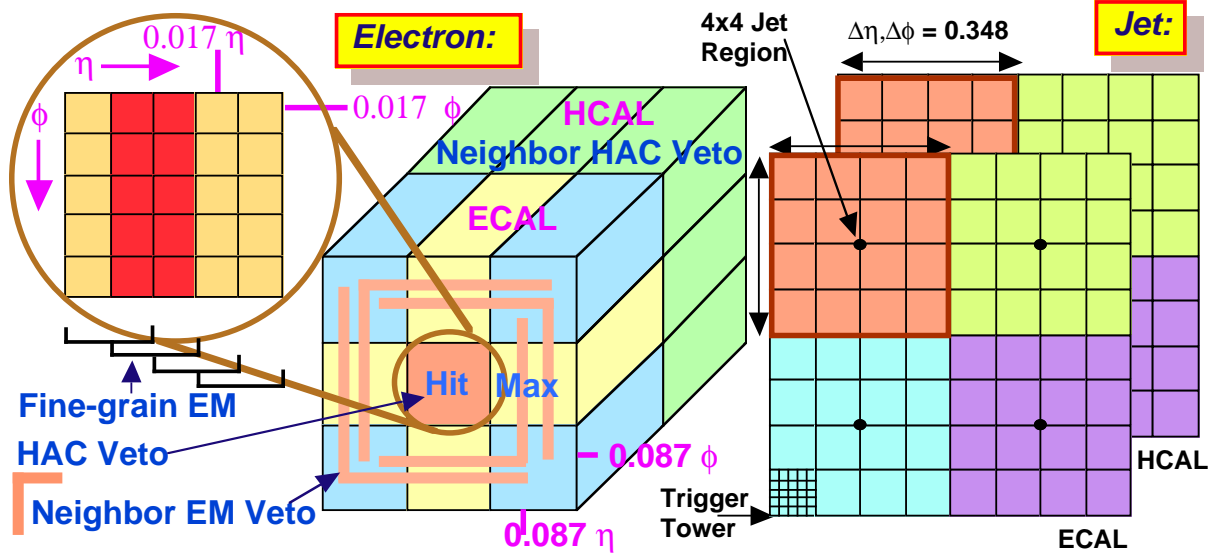


Figure 3. Calorimeter Trigger Algorithms.

The jet algorithm is also illustrated in Figure 3. The 8-bit trigger tower transverse energy data from the calorimeter front-end electronics is used again to sum the ECAL and HCAL energies in the non-overlapping 4 x 4 regions to form the jets, and to look up the E_x and E_y components for computing the missing transverse energy. The jet candidates are sorted based on their E_T and the top four candidates are saved for global trigger decision.

Additional trigger cuts are imposed to permit lower E_t thresholds. An ECAL transverse isolation cut considers all four 5-tower corners of the 3x3 window and requires that at least one of them be below a programmable cutoff. The act of checking all four 5-tower corners ensures that the candidates depositing energy in any corner of the central tower do not self-veto due to leakage energy. Another cut is based on a summary of the energy found in the ECAL crystals before summation in trigger towers. A “fine-grain” electromagnetic isolation bit is set and transmitted with the trigger tower energy if the maximum energy found in a pair of strips of five crystals represents a large fraction of the total energy found in the 25 crystals summed in a single ECAL trigger tower. An electron found in a region where this bit is set can be triggered with a lower threshold.

As shown in Figure 3, jet triggers are based on sums of ECAL and HCAL transverse energy in non-overlapping 4x4 trigger tower ($0.35 \eta \times 0.35 \phi$) regions. Results of detailed simulation of both electron and jet algorithms have shown good performance on the CMS physics signals [2].

Neutrino identification consists of calculating the event missing E_T vector and testing it against a threshold. The calorimeter trigger calculates both sums of E_T and missing E_T . The transverse energy vector components are calculated from the 8-bit compressed-scale digitized HCAL and ECAL pulse heights converted to a linear scale with a 10-bit dynamic range, and multiplied by entries in lookup tables containing the tower angular coordinates. The HCAL and ECAL sums are then combined into single tower sums. The tower sums over threshold are routed through the digital summing networks. The E_T trigger is not used as a standalone trigger, but only in combination with other triggers. When pre-scaled by factors of 1000 or more for E_T above 100 GeV, it is also used to check trigger efficiency and measure the E_T spectrum.

1.5 Calorimeter Trigger Hardware

This document outlines the conceptual design for the level 1 calorimeter regional trigger. It is an update of a previous document³. A block diagram of the CMS Level 1 Calorimeter trigger system is shown in Figure 2. General considerations that have been emphasized in this conceptual design include access to components, power, space and cooling requirements, diagnostics, efficiency and performance information, backplane traffic and timing, DAQ and timing interface, and I/O connections. The design is implemented using off-the-shelf

technology wherever feasible, e.g., 10KH and ECLiPS ECL, TTL, and CMOS components. ASICs are used only where fully justified. The logic design maximizes flexibility and programmability by using memory lookup tables.

The calorimeter level 1 trigger system, shown in Figure 4, receives digital trigger sums from the front end electronics system, which transmits energy on an eight bit compressed scale. The data for two HCAL or ECAL trigger towers for the same crossing will be sent on a single link in eight bits apiece, accompanied by five bits of error detection code and a “fine-grain” bit characterizing the energies summed into the trigger towers. For ECAL, this is the “fine-grain” electromagnetic isolation bit. In HCAL, this bit is set based on the ratio and amount of energy in the first and second longitudinal HCAL sections. For the forward calorimeter, this bit will be set by a tower over threshold, thereby providing a jet tag bit.

The calorimeter regional crate system uses 19 calorimeter processor crates covering the full detector. Eighteen crates are dedicated to the barrel and two endcaps. The remaining crate covers both forward calorimeters. Each calorimeter regional crate transmits to the calorimeter global trigger processor its sum E_T , E_X and E_Y . It also sends its 4 highest-ranked isolated and non-isolated electrons and 4 highest energy jets along with information about their location. The global calorimeter trigger then sums the energies and sorts the electrons and jets and forwards the top four calorimeter-wide electrons and jets, as well as the total calorimeter missing and sum E_t to the CMS global trigger.

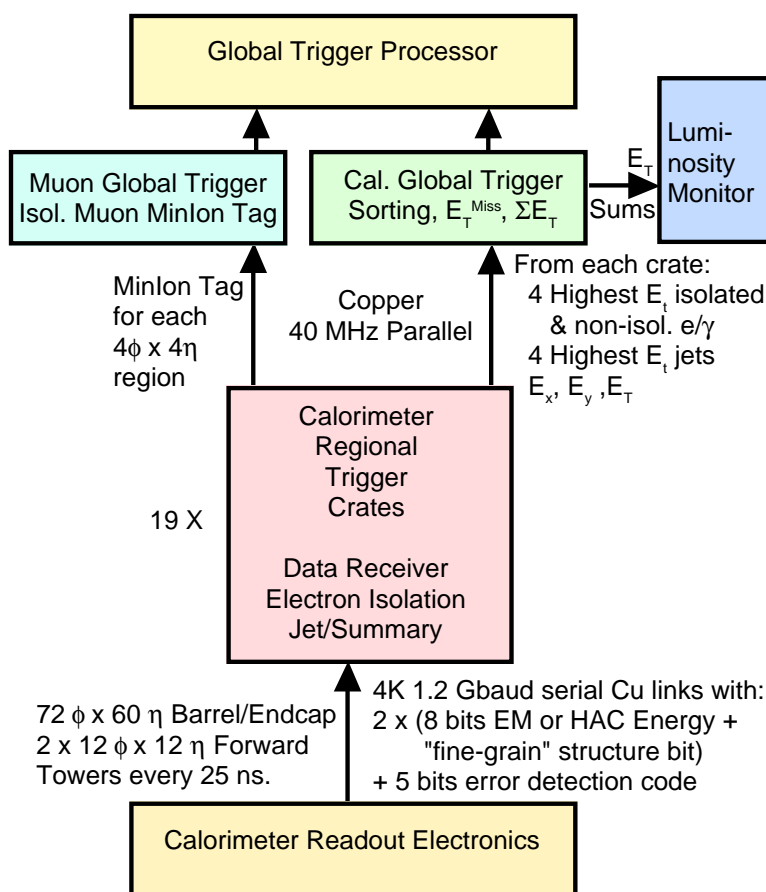


Figure 4. Overview of Level 1 Calorimeter Trigger

Each crate in the Calorimeter Regional Trigger contains eight Receiver Cards, which accept data, described in Section 0, from the Calorimeter Readout Electronics on 32 1.2 Gbaud links. The Receiver Card synchronizes the input data and passes it through look-up tables to separately linearize the energies into the number of bits needed for electron identification and energy triggers. Data in parallel form is shared with the neighboring crates at 80 MHz. The entire system operates in lock step after this stage at 160 MHz. The energies are then summed in 4 x 4 trigger tower regions. The crate is built on a central “backplane” which provides data sharing at

160 MHz. Data for electron identification logic, which includes both the data, received on the serial cables and that received on inter-crate cables, are transferred to the eight Electron Identification Cards. The 4 x 4 sums are transferred to the single Jet/Summary Card.

The two highest E_t candidates from each of the Electron Identification Cards are passed to the Jet/Summary card. The Jet/Summary card sorts the electron and jet candidates in the crate to output the top four ranking isolated and non-isolated electron candidates, and the top four E_t jets on a cable at 40 MHz to the Global Calorimeter Trigger. The candidate electrons are ranked and top candidates are passed to the Jet/Summary card. The Jet/Summary Card also calculates sums of E_x , E_y and E_t for transmission at 40 MHz to the global calorimeter trigger. The global calorimeter trigger cards sort objects and sum energies from their inputs to obtain the final output of the calorimeter trigger which is used together with the muon trigger data to provide the final trigger decision. The output from the calorimeter level 1 regional trigger is described in Table 2.

Calorimeter	Output Segmentation per half	Output Level 1 Data
ECAL & HCAL	$18 \phi \times 6 \eta$	4 highest E_T isolated & non-isolated electrons, jets 10 bits energy
ECAL & HCAL	9ϕ	E_T, E_x, E_y in 10 bits
VFCAL ($3.0 < \eta < 5.0$)	One Region for both halves	E_T, E_x, E_y in 10 bits, jet tag

Table 2. Output Data from the Level 1 Regional Calorimeter Trigger.

2 Calorimeter Regional Trigger Crates

There will be 19 calorimeter processor crates covering the full detector. Eighteen crates are dedicated to the barrel and two endcaps. These crates contain 8 Receiver cards, 8 Electron Isolation Cards, 1 Jet Summary card, and additional support modules. All channels in the Receiver cards are occupied out to an eta of 2.6 with some channels unused from 2.6 to 3.0. The 19th crate covers both Very Forward Calorimeters. Our intention at present is to locate two crates each in Aleph-style racks. The remaining rack front panel space will be occupied by fans, heat exchangers, and crate power supplies. Front panels will be used at all card locations to provide an enclosed environment for the chilled air.

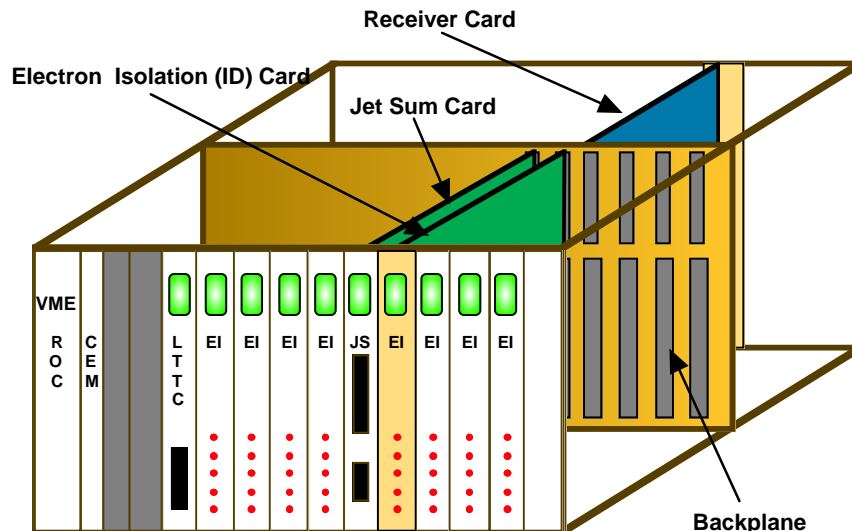


Figure 3. Schematic view of a typical Calorimeter Level 1 Regional crate.

The crate, shown schematically in Figure 3, is based on standard Eurocard hardware. The height is 9U and the depth approximately 700mm, as determined by the front and rear card insertion. The Aleph rack dimension (900mm deep) can handle the crate depth with some reserve for cabling, plumbing, and other services. The backplane is completely custom with a full 9U height. The top 3U is reserved for a 32 bit VME interface. The remaining 6U is used for the high speed data paths between individual cards. The front section of the crate is designed to accommodate 280mm deep cards, leaving the major portion of the volume for 400mm deep rear mounted cards.

Power supplies will be mounted in a separate chassis above each crate. They will be located in the forward 280mm of the volume in consideration of the lower heat load (per unit area) of the forward cards. It is desirable to put the supplies above the crates to place the cards closer to the heat exchangers. Testing is required to determine whether this up and down arrangement will be successful. On board DC - DC converters are also being considered as possible solution to power distribution.

2.1 Enumeration of Card Types

The majority of cards in the Calorimeter Level 1 Regional Processor Crates, encompassing three custom board designs, are dedicated to receiving and processing data from the calorimeter. There are eight rear mounted Receiver cards, eight front mounted Electron Isolation cards, and one front mounted Jet Summary card for a total of 17 cards per crate dedicated to processing data from the calorimeter.

In addition, there are several support cards. The first of these is a readout crate controller and communication module (ROC) selected by the DAQ group. The second is a crate environment monitor (CEM). Both the ROC and CEM will be provided by the Lisbon group. The decision to purchase or create a custom design for the CEM will depend on the final requirements of the environmental monitoring system. Finally, there will be a card dedicated entirely to clock distribution and logging status for the cards in the data processing path. This card, the Local Timing, Trigger and Control card (LTTC), provided by UW, will interface to a TTCrx ASIC located on a card in a separate crate. The TTCrx is the timing receiver ASIC produced by RD12 [4].

2.2 Crate Backplane

As mentioned above, the backplane is a monolithic, custom, 9U high printed circuit board with front and back card connectors. The top 3U of the backplane utilizes 4 row (128 pin) DIN connectors, capable of full 32 bit VME. The first front slot of the backplane will, however, use three row (96 pin) DIN connectors in the P1 and P2 positions with the standard VME pinout. Thus, a standard VME system module can be inserted in the first front station with a form factor conversion between the first slot and remaining slots performed on the custom backplane. The second front card position may also be designed with standard 96 pin DIN connectors if the crate monitor requires them. VME terminations will reside on the backplane.

The bottom 6U of the backplane, in the data processing section of the crate, utilizes a single high speed, controlled impedance, connector for both front and rear insertion at alternating card positions. The design is based around a 340 pin connector, by AMP Inc, to handle the high volume of data transmitted from the Receiver cards to the Electron Isolation and Jet Summary Cards.

The AMP 340 pin stripline connectors have a powerplane between every four signal pins, producing a impedance of 50 Ω . Separate high current contacts, provided for the powerplane connections, will be used to transmit power to the boards. The connectors are housed in a cast aluminum shell that doubles as a board stiffener. The electrical characteristics of the connectors are excellent, allowing rise times in the sub-nanosecond region with very low crosstalk. Press fit contacts are available for use on the backplane. The mating force required for the 340 pin AMP connector is approximately 190N. The four row DIN connector requires an additional 109N. For comparison, a standard 9U, three connector system requires a total of 244N. Therefore, the mating force should be manageable.

2.2.1 Number of Slots

The front and rear insertion of cards in the data processing section of the crate was chosen to allow greater separation between cards and to provide a more protected environment for the cables connected to the rear mounted Receiver cards. The increased separation promotes better cooling of the cards, and will enable a wider selection of front panel components. The staggering of the slots between front and rear cards, shown in Figure 4, is as much a result of the style of connector selected as the fact that piggybacking of connectors is inappropriate in this situation. Almost half of the signals entering the Electron Isolation board come from neighboring Receiver cards.

The spacing between cards, in the data processing area, is 3.56cm front or rear, with a 1.78cm stagger front to rear. Therefore, the eight Receiver cards, eight Electron Isolation cards, Jet Summary card, and Clock distribution card occupy 18 slots with a span of only 32.04cm across the front of the crate. The remaining 8.61cm will be allocated to a DAQ Readout card (ROC) (4.06cm), Crate Environment Monitor (CEM) (2.03cm), and a transition region for the change in form factor between the standard and non-standard VME. This is a total of 20 slots.

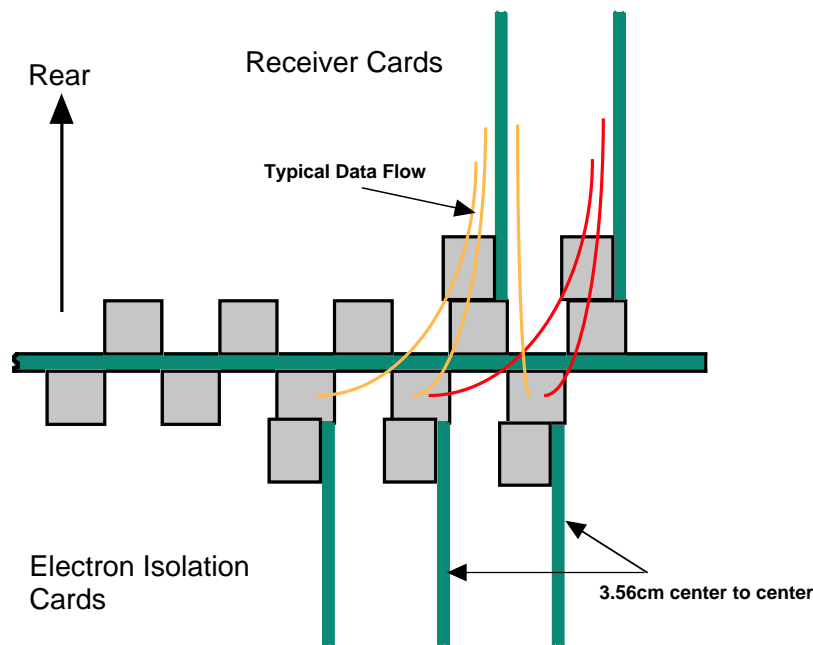


Figure 4. Top view of region crate backplane.

2.2.2 Card Order

As shown in Figure 3, the first two or three slots in the crate will house the Crate Readout Card (ROC) and Crate Environment Monitor (CEM). The remaining crate volume is used for the data processing cards. The first card after the transition region will be the Local Timing Trigger and Control card (LTTC). This is followed by the first four Electron Isolation cards (EI) with their corresponding Receiver cards (RC) staggered 1.78cm to the right in the rear of the crate. The next card is the Jet Summary card (JS), with no matching Receiver Card. Finally the four remaining Electron Isolation cards fill out the crate. The corresponding Receiver cards are plugged in at the rear, staggered 1.78cm to the right. The figure is not to scale in that it implies substantially more free space at the right hand end of the crate than actually exists.

2.2.3 Backplane construction

The prototype backplane is a 42.52cm x 39.70cm multilayer printed circuit board .34cm thick. The thickness of the final version will likely change based on our experience with the prototype with regards to impedance, mechanical strength, and final choice of connectors. The other dimensions are fixed by the physical size of the crate. There are on board VME terminations, multiple studs for power supply connections, bypass capacitors, and mounting holes.

The design impedance is 50Ω for the lower 2/3 of the backplane which contains all the trigger data paths. This impedance matches the AMP connector impedance and the impedance of the individual boards. The wiring in this section is all point to point, making for a fairly straightforward transmission line. Terminations for these lines are on the receiving cards. The multi-drop transmission line of the VME backplane in the upper 1/3 of the backplane has an impedance of 100Ω – before holes and connectors are added. The effective impedance of this section will drop to a little less than 50Ω after connectors and trace stubs on the individual boards are taken into account.

The VME specification is written for crates containing no more than 21 cards. In addition, the specification requires that VME signal stubs on individual boards be no greater than 5.08cm in length. The present design for

the trigger processor crates contains 20 cards with a VME interface. Reducing the VME interface from two connectors to one has increased the difficulty of staying within the 5.08cm requirement. Special care has been taken throughout the design process to stay within the VME standards.

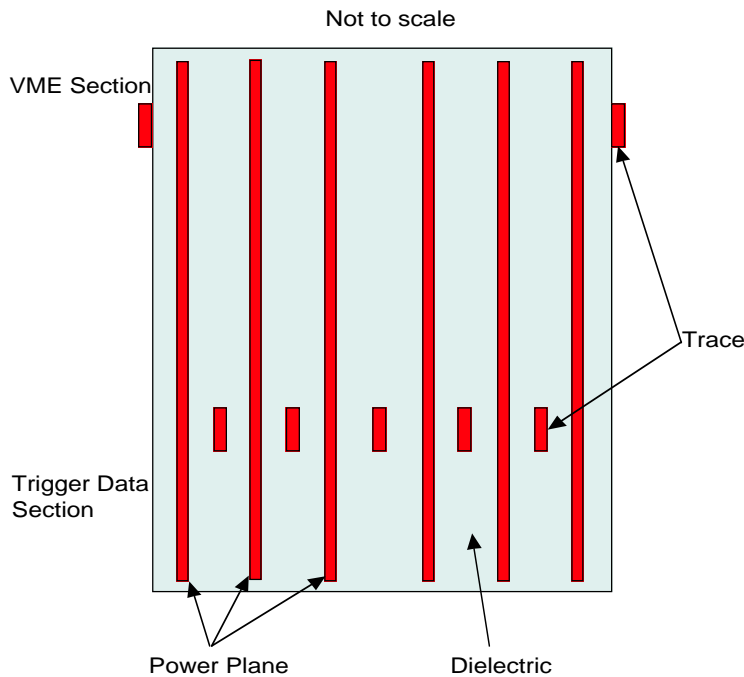


Figure 5. Schematic representation of backplane showing stack-up for VME and Trigger Data sections.

In order to ensure there are sufficient wiring channels and to maintain symmetry, five buried layers are used in the trigger data section. A picture of the board stack-up is given in Figure 5. An alternating power plane/signal plane structure produces a buried stripline design and surface micro-strip traces. The stripline structure provides good control over crosstalk and general noise immunity. The outside signal layers will be used mostly in the VME section of the backplane. Signals in the trigger data portion are constrained, but not strictly limited to, the buried stripline layers.

2.2.4 Data Rates

All signals in the trigger data portion of the backplane are transmitted at 160 MHz. This data rate was chosen because it offers the opportunity to compress the number of data lines on the backplane by a factor of four and because it should be realizable by available technology. More testing should be done on the prototypes, at these rates, to validate the design. All signals in this section, including clocks, are transmitted point to point. In the present design, all signals are differential.

3 Detector to Crate Mapping

A preliminary mapping of the calorimeter to the Level 1 regional trigger crates is presented here. Trigger tower geometry has yet to be optimized, and changes in the calorimeter tower layout will result in changes to this mapping. The efficiency of utilization of channels on Receiver cards may also be affected by changes in the calorimeter design.

3.1 Eta - Phi Space

The current proposal is for trigger towers to have a size of .087 in both phi and eta for all phi between eta of 0.0 and ~2.3. This granularity produces 72 towers in phi and 26 towers in eta for each half of the calorimeter. Between eta of ~2.3 and ~2.6 the tower size changes to .174 in eta, with the phi granularity unchanged. This produces another two towers in eta. Finally, between eta of ~2.6 and 3.0, there are two towers with a granularity of .195 in eta. Therefore, between eta of 0.0 and 3.0, there are 2160 Electromagnetic and Hadronic trigger towers in the half detector. The present proposal for the Very Forward Calorimeter has 12 trigger towers in phi and 12 towers in eta for eta between 3.0 and 5.0. The Electromagnetic and Hadronic towers are combined

on the detector, in the region of $3.0 < \eta \leq 5.0$, producing a single trigger tower for each pair. The grand total of trigger towers is 8928 for the full calorimeter. Refer to section 1.3 of this document for additional information on tower geometry and mapping.

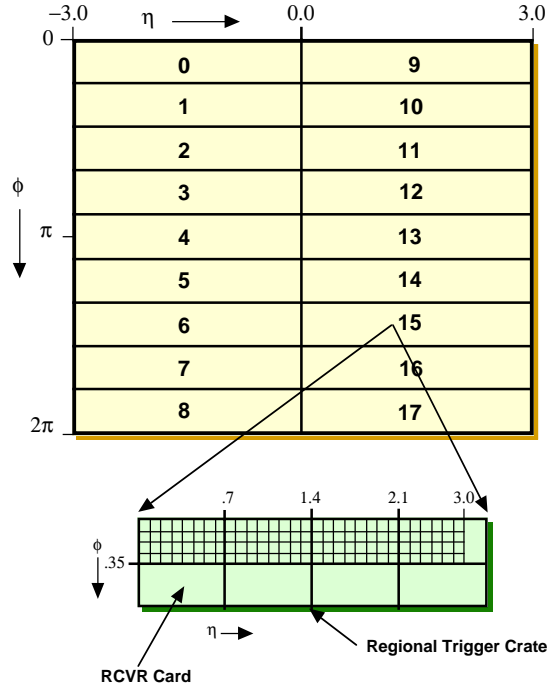


Figure 6. Mapping of Calorimeter Barrel and Endcap onto Trigger crates.

Figure 6 illustrates a mapping of the calorimeter onto the Regional Trigger Processor crates for the region between eta of -3.0 to 3.0. The 18 crates shown are required for the barrel and both endcaps. Another crate (not shown) is included for the Very Forward Calorimeter. This mapping minimizes the intercrate cabling in a way consistent with simplifying the backplane and producing a rack layout that minimizes the cable lengths between racks.

The Very Forward Calorimeter covers the region $3.0 < \eta \leq 5.0$ and is not used for the isolated electron triggers. The electromagnetic and hadronic information is combined on the detector and sent to the trigger processing hardware as a single sum along with a feature bit. The generation of this feature bit is not yet defined. This region can be covered with a single trigger crate containing six Receiver cards. The Jet Summary card forms the E_T sums and performs the trigger cuts on the data from up to twelve sub-regions of the Very Forward Calorimeter.

3.2 Backplane Layout

The map of the calorimeter onto crates is used to derive a card to slot mapping within the crate itself. The layout of cards within the crate is set up to minimize the length of traces on the backplane. Figure 7 illustrates a layout which attempts to satisfy this condition. For reference the schematic mapping of the calorimeter onto a single crate is repeated with a slot numbering (left to right) superimposed on the eight Receiver cards. This numbering is relative within the trigger data region of the crate and is not meant to represent a specific card slot. The sharing shown in the figure is representative of an "average" card and does not show the intercrate connections. Card 3, for instance, would share with cards 0, 1, 2, 4, and 5, within the crate, as well as with cards 0, 2, and 4 in the adjoining crate. Every card, except those covering $\eta \geq 2.4$, shares with eight other cards.

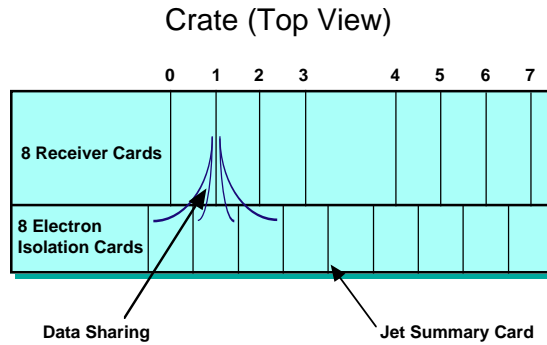
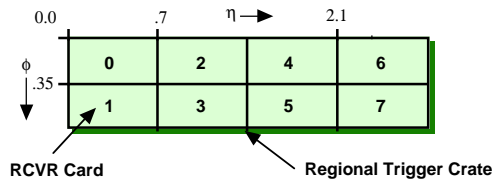


Figure 7. Card layout in the trigger data portion of the crate.

4 Receiver Card

The Receiver card is the largest board in the crate. It is 9U by 400mm. Both sides of the card are utilized to receive and process calorimeter trigger data. The rear side of the card receives the calorimeter data, converts from serial to parallel format, and transmits it to the front side. The front side of the card contains circuitry to align and re-phase the incoming data with the local clock, and check for data transmission errors. There are also lookup tables and adder blocks on the front. The lookup tables translate the incoming information to transverse energy on several scales. The memories were placed on this card, rather than the processing cards, because the sharing of data between processing cards would have required nearly twice as many memory chips. The energy summation tree begins on these cards in order to reduce the amount of data forwarded on the backplane to the Jet Summary card. Separate cable connectors and buffering are also provided for intercrate sharing.

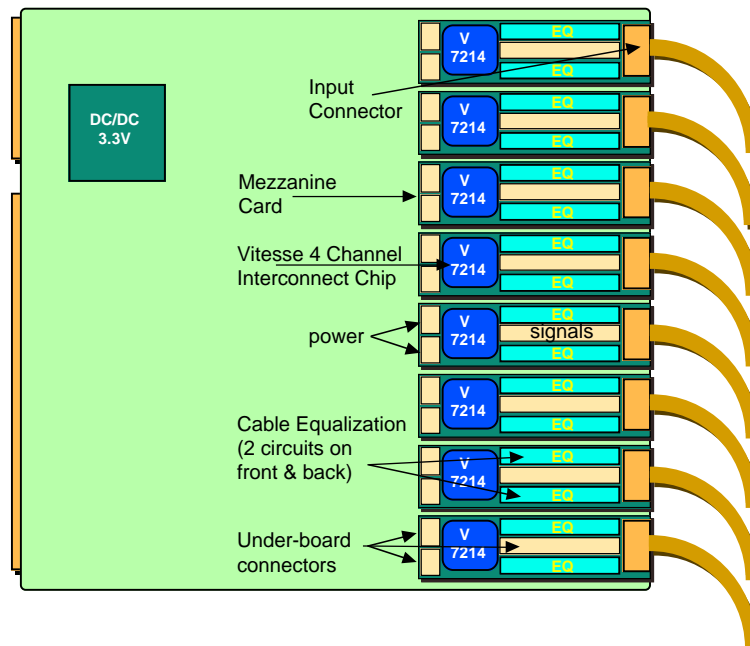


Figure 8. Rear view of the Receiver card and the receiver circuitry.

4.1 Inputs

Each card is designed to receive 32 channels from the ECAL[5] and HCAL[6] front-end readout system. Each channel transmits either two towers of hadronic or electromagnetic information per crossing. The energy is transmitted on copper twinax in a compressed eight bit format, providing a total of 16 data bits. A single bit is appended to each of the 8 bit fields providing information about the characterization of the energy deposition determined from the calorimeter energies before calculation of the trigger primitives. An additional 5 bits contain a single Hamming code generated from the 18 bits of data. This code is sufficient to detect all single and double bit errors as well as many multiple bit errors. The present design uses transmitter and receiver links capable of handling 24 bits of information in 25 nsec with a baud rate of 1.2 Gbaud. The rear of the Receiver card, containing the receiving circuitry is shown in Figure 8.

The mapping presented in section 3.1 shows two Receiver cards in each crate that are not fully utilized. For eta of ~ 2.6 to 3.0 we only partially fill two 4×4 regions in phi. The front end electronics, reading out the region between eta of 3.0 to 5.0, sums the electromagnetic and hadronic towers on the detector before sending the data to the Level 1 regional Trigger crates. The Endcap calorimeter ends at an eta of 3.0. The region $3.0 < \eta \leq 5.0$ is covered by the six receiver cards in the 19th crates as described in section 3.1.

4.2 Serial Cable Receiver

Two different receiver chips have been considered for this design. The first device, the VSC7214 made by Vitesse, has 4 full duplex channels capable of running between 1.2 and 1.3 Gbaud. It is designed to support Gigabit Ethernet. A slightly slower speed version runs 1.062 Gbaud Fibre Channel. The data is encoded 8B/10B on the chip. The serializer and deserializer is also included. The parallel data I/O is eight bits wide per channel. 3.3V bias is required for power. Inputs and outputs are low voltage TTL except for the serial data path which is PECL. Power dissipation is approximately 3.3W. The chip comes in a 160 pin PQFP and cost approximately \$75 in 1000's. If this device is chosen, we will run it at 1.2 Gbaud, transferring 24 bits of information per crossing per channel.

The second device under consideration is HP's HDMP-1014 Receiver. The transmitter has part number HDMP-1012. It is single channel, simplex only. It can run at rates between 120 Mbaud to 1.24 Gbaud with parallel data paths of 16, 17, 20, or 21 bits depending on the mode of operation. The encoding scheme is HP's own and they take pains to maintain the dc balance of the serial line. The chip is designed to interface to 100K ECL and is biased at -5.0V. Power dissipation is approximately 2.6W. The chip comes in an aluminum M-Quad 80 pin package. Current pricing is around \$60 in 100's. If this device is chosen we will run it around 960 Mbaud transferring 21 bits of information per crossing per channel. Using this device would require changing the data from 9 bits to 8 bits per tower. The ECL I/O of the HDMP-1014 is a better match for the rest of the circuitry on the Receiver Card.

The receiver chips will be placed on a mezzanine card along with the cable connector and an equalization circuit. The mezzanine card provides a certain amount of power supply isolation and allows for the replacement of faulty receivers with minimal trauma to the Receiver Card itself. There is also less conflict between the routing requirements of the receiver circuitry and the dense high speed ECL circuitry resident on the front side of the Receiver Card. Mounting the connectors for the serial link on the mezzanine card also avoids a collision between those connectors and the intercrate data connectors on the front side of the main card. Surface mount board to board connectors with locating pins are used to mount the mezzanine cards to the Receiver card. Two of these connectors are dedicated for power from the Receiver card to the mezzanine card. If the Vitesse chip is used, a DC/DC converter on the back of the Receiver card will provide the 3.3V.

4.3 Clock Synchronization and Re-phasing

The serial data arriving at the inputs to the Receiver Cards is generated in neighboring Calorimeter Readout crates and received over 20m of cable. We believe this length sufficient for the area containing the HCAL, ECAL, and Trigger racks. All cables will be cut to the same length. Equal length is required by equal timing and a single design for the equalization circuit on the receiving end of each cable. The Vitesse chip is capable of treating its four channels as a single word. Each channel has a deskewing buffer of ± 2 bit times. This buffer can compensate for different delays in cable routing and small phase drifts between transmitting and receiving ends. The four channels can also be treated independently. In either case the data may be clocked out of the receiver chip using either a local clock or a recovered clock from one of the channels. The HDMP-1014 does not have a deskewing buffer and provides a recovered clock timed in with its data. Detailed timing requirements will be developed after testing a transmitter/receiver pair.

The data is transferred from the mezzanine card to the Phase ASIC mounted on the front side of the Receiver Card shown in Figure 9. If the Vitesse 7214 is used as a receiver the input pads on the Phase ASIC will be chosen to accommodate LVTTTL. If the HDMP-1014 is used the input pads will be true ECL. In either case the output from the Phase ASIC will be true ECL. Two different designs are being considered for this ASIC. The first design is determined by the use of a recovered clock from the receiver chip to clock data into the ASIC and the second is determined by the use of the local clock to store the data into the Phase ASIC. The design effort and, accordingly, cost difference between the two approaches is significant. Further study is required to determine which approach should be implemented.

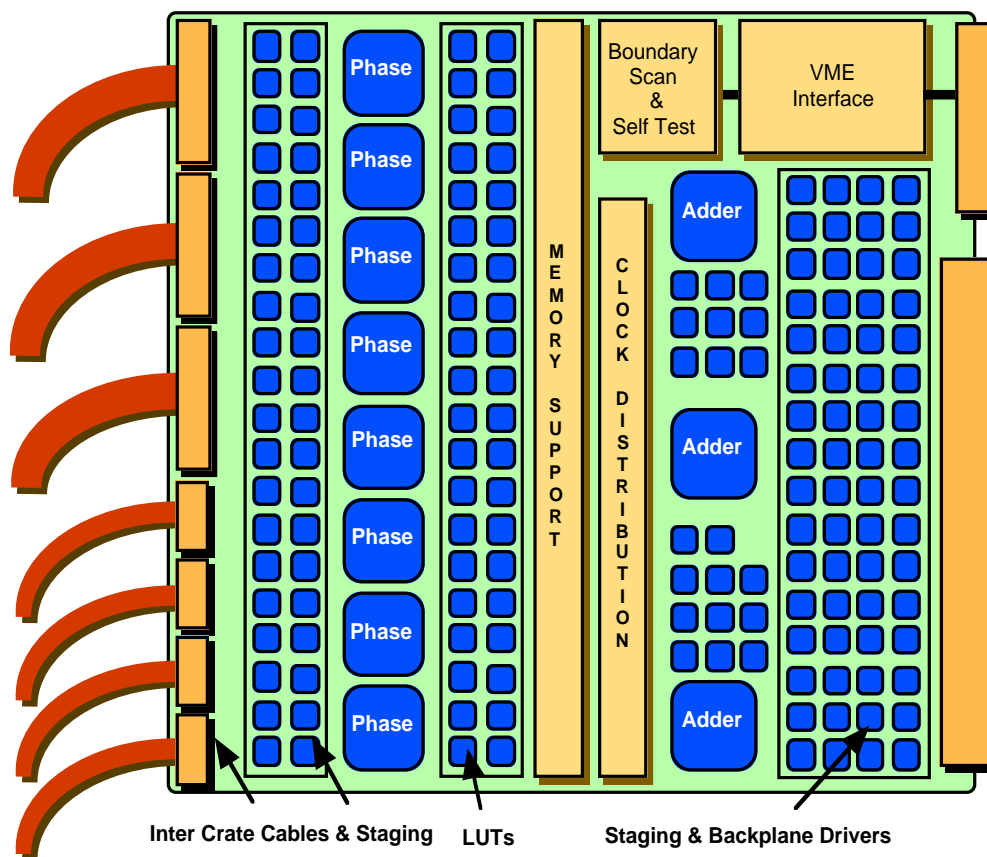


Figure 9. Front view of the Receiver card with Synchronization and Adder tree circuitry.

4.3.1 Phase ASIC

There are several possible implementations for the Phase ASIC depending on the choice of serial receiver and clock source. Regardless of the particular implementation, four channels of two tower data, multiplexed onto two output channels are a common feature. We describe one particular approach assuming the use of a VSC7214 along with its recovered clock. A block level diagram of the ASIC is shown in Figure 10.

Each of the four input channels is comprised of 8 bits of data, from the 10bit/8bit decodes, and 3 bits of status. One of the three status bits is an error bit set by the receiver as a result of several illegal conditions that might occur. The remaining two status bits can either indicate the current operating mode of the receiver chip or qualify the error bit. Each channel's parallel output is arriving at 120MHz. Three frames, or 24 bits of data per channel, complete the data transfer for a single bunch crossing. The four channels, taken together, produce 44 bits of information every 8.33ns. These 44 bits are clocked into the input stage of the Phase ASIC using the clock recovered from the VSC7214. A block diagram of the Phase ASIC is shown in Figure 10.

The input stage of the Phase ASIC is a 44 bit wide FIFO that is six frames deep. The FIFO can accommodate minor phase shifts between the transmitter and local clocks and is kept approximately half full. The FIFO is followed by a circuit which establishes the proper phase between the incoming data and the local bunch crossing clock. This circuit makes use of status information from the VSC7214 to set the final phase. Once properly phased, the data and error bits can be separated into 18 bits of data (two channels) and 5 bits of Hamming code.

The Hamming code is recomputed from the data and compared with the received Hamming code bits. The data leaves the Phase ASIC in two data channels, 9 bits apiece, and one 9 bit error channel. The error bits are made up of the transmitted EDC, a subset of the status bits from the VSC7214, and an overall error indicator. The status bits from the VSC7214 provide sufficient information to determine the state of the serial links at any point in time.

As we have four input channels, each handling two towers per crossing, the two output channels produce four towers of information per crossing. The outputs are clocked at 160MHz. This rate was chosen to match the processing circuitry on the rest of the board. By running the Receiver Card at 160MHz we realize a substantial savings in the amount of logic required to process the data.

The last storage element of the Phase ASIC will be implemented as a loadable counter. During normal operation the counter will be loaded with data each 6.25ns. During testing the counter can be reset and enabled to count synchronously with the rest of Phase ASIC outputs. The counter outputs will address the look up tables just as detector data would. The combination of these counters and look up tables can be used to provide any data pattern necessary to test the remainder of the Trigger Processor system. The error outputs will be idle during testing.

The Phase ASIC will have a JTAG controller and scan cells on all the outputs. Total signal pin count, including JTAG should be around 80. The technology for the Phase ASIC is expected to be the same Vitesse 0.6 micron GaAs process as used for the Adder ASIC described below.

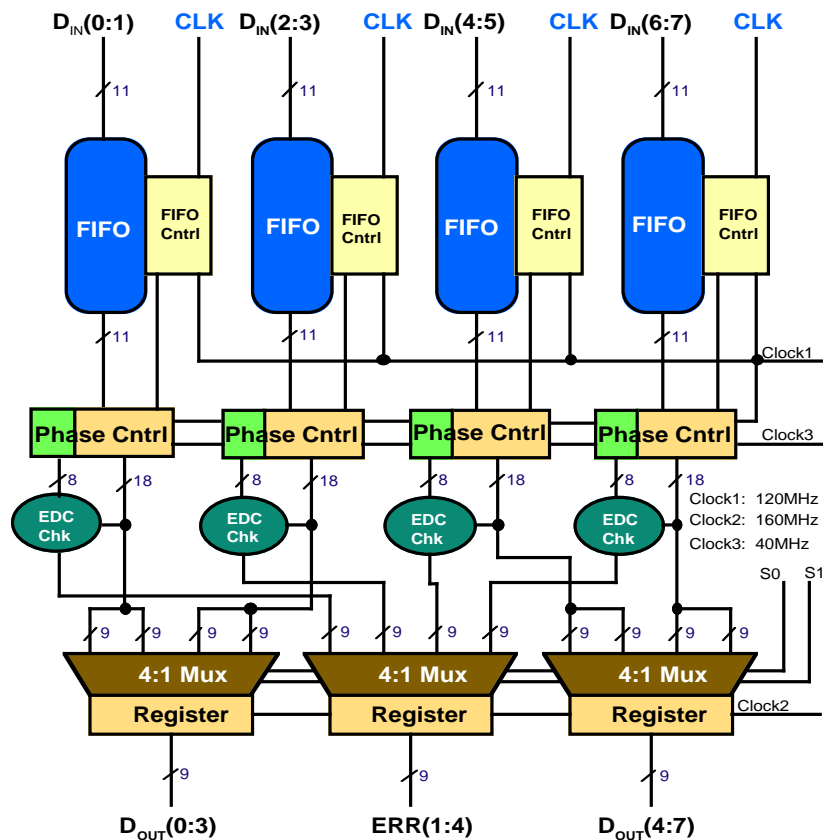


Figure 10. Block diagram of Synchronization ASIC.

4.4 Lookup Tables

Lookup tables are required to translate the information coming from the calorimeter front end electronics, in compressed format, onto the several different scales used by the energy adder tree and the Electron Isolation logic. The Hadronic and Electromagnetic energies are individually translated into eight bits of linear E_T with a resolution of approximately one GeV. These values are summed to provide total energy in 4 x 4 trigger tower

regions of the calorimeter. They are forwarded to the Jet Summary card for further combination in the total transverse energy calculation and used as the basis for E_X and E_Y missing transverse energy calculation.

There are several designs under consideration concerning the implementation of the Look Up Tables (LUTs) and number of bits used for the isolated electron algorithm and jet E_T sums. We will describe one of the proposals, reasonably consistent with the current isolation algorithm. The final choice will be made after we gain more feedback from the prototype Receiver card.

The processor on the Electron Isolation (Electron ID) card requires electromagnetic and hadronic transverse energy with several dynamic ranges. The reference tower needs 7 bits of electromagnetic transverse energy with a resolution of .5 GeV and 4 bits of hadronic transverse energy with a resolution of .5 GeV. The neighboring towers also use 7 bits of electromagnetic energy with a resolution of .5 GeV and 1 bit of hadronic energy veto based on thresholding. The corner towers for each 4 x 8 region are reduced to 3 bits with a resolution of .5 GeV. To guard against wrap-around when the 3 bit electromagnetic values and 4 bit hadronic values are generated, any value greater than the maximum of the bit range is set to the maximum three or four bit value. The algorithm described in this document is diagrammed in section 1.4 and described in greater detail in section 5.2.

With a 6.25 nsec period the memories must have access times less than or equal to 3.0 nsec in order to provide margin for the usual board propagation and setup and hold times. Data is downloaded to the memories and read back through the VME interface. This requires support circuitry located in the area of the memory chips. The data inputs to the memories can be tied in parallel for writing the chips, but all the address lines (128) need to be individually buffered. The buffering is located near the memory in order to maintain short board traces in the high speed section of the logic. Reading the data out of the memories back to the VME interface requires buffering for all the data output lines. This buffering is provided by an 8:1 multiplexer within each Adder ASIC. A separate read back path is used for the 7 bits of electromagnetic isolation energy and 4 bits of hadronic isolation energy.

4.5 Energy Summing

The beginning of the energy summation tree is on the Receiver card. The transverse energy for each of the two 4 x 4 trigger tower regions is independently summed and forwarded to the Jet Summary card. On the Jet Summary card these E_T sums are used to continue the energy summation tree and also sorted to provide the four highest Jet candidates from the crate. The E_T sums are applied to a set of lookup tables to generate E_X and E_Y for each 4 x 4 region. A separate adder tree is used to sum up E_X and E_Y from the regional values.

Though the input values at the top of the adder tree have only 8 bits of range, the adder tree has been designed to handle a dynamic range of 10 bits for either positive or negative values. This implies an overflow at approximately 1000 GeV, using the compressed scale described in the CMS Level 1 Calorimeter Trigger Performance Studies [5]. The exact value will depend on the resolution required of the input transverse energy for other trigger functions. Any overflow (or underflow) generated as the result of an arithmetic operation (A_{OV}) will stay in time with the data and be ORed with any other overflow that might have occurred in the same crossing. All values are handled as 11 bit 2's-complement numbers.

A second overflow condition can also occur. The value sent to the trigger processor from the calorimeter front end electronics may be at the highest possible count. The lookup tables will be programmed to output FF_H for this particular input. This output code is recognized, at the top level of the adder tree, as indicating an input data trigger tower overflow (T_{OV}). It is handled much like the arithmetic overflow in that it is ORed with other T_{OV} overflows and passed down the tree in time with the data that generated it. If the overflow is caused by a hardware failure, the lookup table can be re-written to zero out the affected channels. The arithmetic and tower overflow bits are handled separately through to the end of the adder tree. T_{OV} recognition can be disabled.

4.5.1 Adder ASIC

The adder ASIC is implemented as a 4-stage pipeline with eight input operands and 1 output operand. There are only three stages of adder tree, but an extra level of storage has been added to ensure chip processing is isolated from the I/O. We have determined that the ASIC must work reliably at a clock period of 5.0 nsec in order to ensure safe operation at an in-circuit period of 6.25 nsec.

This ASIC uses 4 bit adder macro cells to implement twelve bit wide adders. Eleven bits are wired, left justified, to each operand of an adder. The LSB of each adder will be internally set to ZERO. The MSB is treated as a sign bit. Therefore, although the adder tree may be constructed from three 4 bit adders, the width of the operand data paths has been limited to eleven bits.

An Adder ASIC chip is designated as 'master' if it is in the top rank of the adder tree and as 'slave' if it is further down. Masters can generate Tower overflow (T_{OV}), but slaves can only propagate T_{OV} . Both masters and slaves can generate and propagate arithmetic overflow/underflow (A_{OV}). These bits are appended to each input and output operand, making all operands 13 bits wide. T_{OV} becomes the twelfth bit of the output result and A_{OV} the thirteenth bit. The data outputs of the chip are forced to 3FF_H when either an overflow or underflow occurs.

4.5.1.1 Detailed Description

The top of the adder tree is composed of four 12 bit adders and includes the logic required to detect and propagate T_{OV} and A_{OV} . The T_{OV} generate circuitry is a filter designed to detect the input code 3FF_H. The A_{OV} generate circuitry examines the sign bits of the input operands and the results operand, together with the carry out, to determine whether or not an overflow or under flow has occurred. All eight of the T_{OV} bits are ORed together and all four of the A_{OV} bits are ORed together to form two separate overflow bits that are forwarded with the data in the pipeline. Edge triggered registers are used to store the results for the next stage of the adder tree. A block diagram of the Adder ASIC is shown in Figure 11.

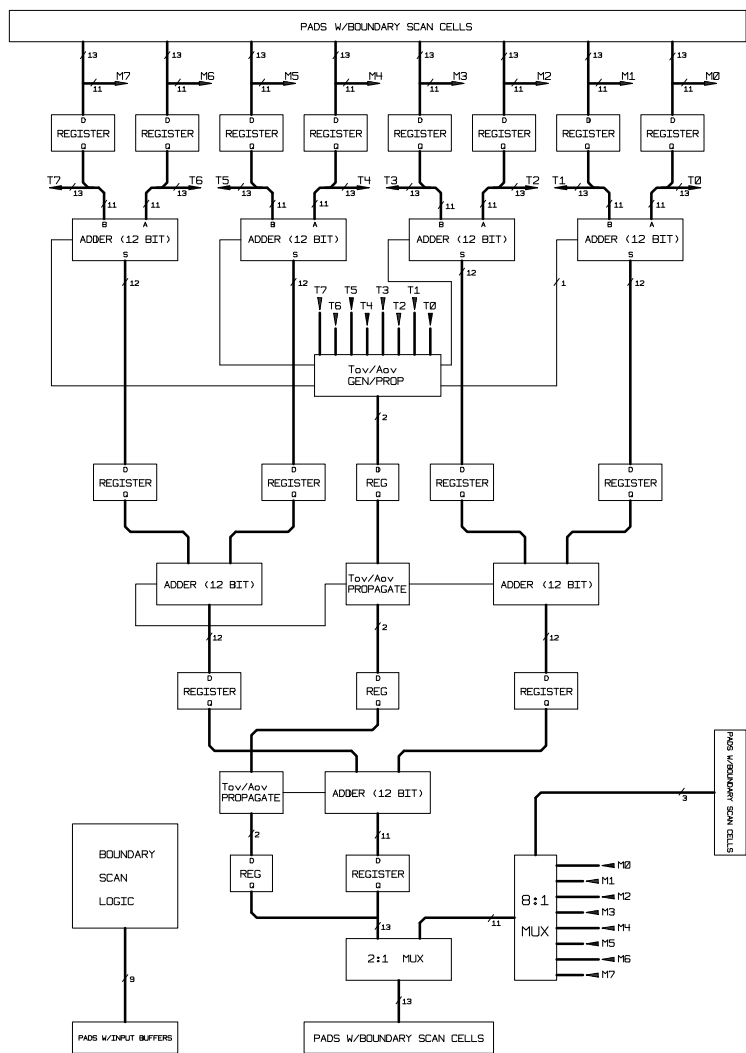


Figure 11. Block diagram of the Adder ASIC.

The second stage contains two more 12 bit adders and includes the logic needed to propagate T_{OV} and to detect and propagate A_{OV} . From this point on, T_{OV} is forwarded down the pipeline from register to register. A_{OV} is

generated in the same manner as in the first stage and the resulting two bits are ORed with the A_{OV} from the previous stage. Edge triggered registers are used to store the results for the next stage of the adder tree.

The third stage contains the final adder as well as a continuation of the T_{OV}/A_{OV} circuitry. The register at this level is the last storage element before the ASIC output. If either T_{OV} or A_{OV} have been detected, the output operand stored in this register has the value $3FF_H$. T_{OV} and A_{OV} are stored along with the operand. Adder Tree ASICs further down in the tree are designated "slaves" and are blocked from using the operand $3FF_H$ to generate T_{OV} . Thus we retain the identity of the tower overflow bits through the entire tree.

The last register is presented to one input of a 2:1 multiplexer before leaving the chip through the boundary scan cells and pads. The other side of the multiplexer is fed by an 8:1 multiplexer which passes any one of the eight input operands, less the two overflow bits, to the output of the ASIC. This feature was provided to minimize the external logic needed to read back the values of the lookup tables that feed the first stage of the adder tree logic.

The equations below provide definitions for A_{OV} , T_{OV} , and the output operand. Clock cycle $n+1$ is the time at which these three values are present at the outputs of the ASIC.

$$\left. \begin{aligned} T_{OV}(n+1) &= 1 \text{ if any input operand } OP_{IN}^{1 \rightarrow 8}(n-3) = 3FF_H \text{ for the masters.} \\ T_{OV}(n+1) &= T_{OV_IN}^1(n-3) + \dots + T_{OV_IN}^8(n-3) \text{ for the slaves.} \end{aligned} \right\} (1)$$

$$\left. \begin{aligned} Out_{0 \rightarrow 10}(n+1) &= S_{1 \rightarrow 11}^7(n), \text{ if } A_{OV}(n) \text{ and } T_{OV}(n) \text{ both equal ZERO.} \\ Out_{0 \rightarrow 10}(n+1) &= 3FF_H, \text{ if either } A_{OV}(n) \text{ or } T_{OV}(n) \text{ equal ONE.} \end{aligned} \right\} (2)$$

$$\left. \begin{aligned} A_{OV}(n+1) &= A_{OV}(n) + A_{OV}(n-1) + A_{OV}(n-2) + A_{OV}(n-3) \\ &\text{where} \\ A_{OV}(n-3) &= \bigcup_{p=1}^{p=8} A_{OV_IN}^p(n-3), \\ A_{OV}(n-2) &= \bigcup_{r=1}^{r=4} \left[\overline{(A_{11}^r(n-2) \oplus B_{11}^r(n-2))} * (S_{11}^r(n-2) \oplus A_{11}^r(n-2)) \right], \\ A_{OV}(n-1) &= \bigcup_{r=5}^{r=6} \left[\overline{(A_{11}^r(n-1) \oplus B_{11}^r(n-1))} * (S_{11}^r(n-1) \oplus A_{11}^r(n-1)) \right], \\ &\text{and} \\ A_{OV}(n) &= \overline{(A_{11}^7(n) \oplus B_{11}^7(n))} * (S_{11}^7(n) \oplus A_{11}^7(n)). \end{aligned} \right\} (3)$$

S_{11}^x is the sign bit of the x th sum. $A_{OV_IN}^p$ is the overflow input for the p th operand. A_{11}^r and B_{11}^r are the sign bits of the A and B operands of the r th adder. $T_{OV_IN}^x$ is the tower overflow bit for the x th operand. Finally, n is the n th clock cycle in the pipeline.

4.5.1.2 ASIC Boundary Scan

The chip also contains boundary scan support. The ASIC boundary scan implementation, along with a proper board level implementation should provide full testing capability of the ASIC while it is in circuit. The boundary cells can also be used to verify circuit integrity (shorts, opens, and stuck at one/zero) at the board level. IEEE standard 1149.1 has been strictly adhered to in order to ensure compatibility with other ASIC and board level boundary scan controllers. The full JTAG controller and a major subset of the commands has been implemented. All inputs and outputs, with the exception of the five boundary scan control signals, have scan I/O cells.

The following instructions are recognized by the JTAG controller: BYPASS, IDCODE, SAMPLE/PRELOAD, EXTEST, and INTEST. BYPASS collapses the scan loop to a single bit, thus bypassing the ASIC as seen by the board level scan loop, providing faster testing of other chips on the board. IDCODE serially outputs an identification code indicating the manufacturer, part number, and revision level of the ASIC. The four least significant bits are used to provide an address for the chip. This address will be set at the board level by hardwiring four input pins. SAMPLE/PRELOAD samples and preloads the boundary scan cells on two separate phases of the instruction. EXTEST tests the communication with the exterior by setting up values on the ASIC outputs and sampling values on its inputs. INTEST is used to test the internal circuitry. It accomplishes this by setting up known vectors on the input scan cells and capturing the results, after single stepping the core logic, in the output scan cells.

The prototype Adder ASIC implements all the above features. It was manufactured by Vitesse in 0.6 μ GaAs technology and is packaged in a 195 pga. It requires approximately 4 W of power.

4.6 Staging Circuitry for the Electron Isolation Board

Thirty-two towers, in a 4 x 8 array, are processed on each Electron Isolation board. Data from twenty-eight neighboring towers is required to determine isolation for towers on the edge of the 4 x 8 region. Data is transferred between the Receiver card and the Electron Isolation card at 160 MHz. In order to retain point to point transmission, data going to a neighboring Electron Isolation board must be transmitted through separate drivers on separate backplane lines.

Every Receiver card shares its data with at most 6 Electron Isolation cards within the same crate. In addition each Receiver card sends some of its data off crate at 80 MHz to a maximum of three neighboring crates. Crate to crate communication is handled by special cables running between the Receiver cards. This distributes the inter-crate buffering among the eight Receiver cards in a crate rather than attempting to put it all on one or two special cards at the ends of each crate. The maximum amount of intercrate information that can enter and leave a Receiver card is carried on 120 twisted pair cable.

The order in which the data is transmitted to the Electron Isolation card is important. Since connector pins are at a premium, it is necessary to ensure that all lines have useful data for each of the four 6.25 nsec cycles making up a 25 nsec crossing. Board space is also at a premium, so it is necessary to limit the amount of circuitry committed to staging the data for the backplane. The most efficient way to satisfy these goals simultaneously is to pay careful attention to the order of cabling between the detector front end electronics and the input channels of the Receiver card. This, in conjunction with the multiplexing of data in the Phase ASIC, handles most of the data staging. Some of the data transmitted between the Receiver card and Electron Isolation (Electron ID) card comes from neighboring crates. This data has been delayed in time with respect to the data originating on the local Receiver card. The local data must be delayed to allow the shared data to "catch up". This function will be incorporated into an ASIC that includes the differential drivers for the backplane data and the JTAG boundary scan.

4.7 Boundary Scan

The board level boundary scan is still under design. The boundary scan commands supported by the Adder ASIC have already been described, and the board level controller will support them as well. The following is an outline of features under consideration.

The other two main components to incorporate boundary scan are the Phase ASIC and the BSCAN ASIC. The Phase ASIC has boundary scan on its outputs only. However, this should be sufficient to provide JTAG control over most of the circuitry on the card. The Phase ASIC can be used to set up data across all the inputs to the look up tables. The Adder ASIC can capture the resulting data on its inputs or pass it through to the downstream logic. The BSCAN ASIC has scan cells on both its inputs and outputs. The inputs can be used to capture test data set by either the Phase or Adder ASICs. The outputs can be used to set up test data for the backplane. Scan registers in ASICs on the Electron Isolation card and Jet Summary card can capture the data

directly off the backplane. The BSCAN ASIC also provides the differential drivers for the backplane data and delay registers for data alignment. The delay is programmable from zero to seven 6.25 ns cycles.

The board level boundary scan controller will have a hardwired program that is entered on power-up or by command through the VME interface. This program will use vectors stored in a PROM on the board to perform a minimal test on intra-board circuit integrity and make simple tests of data paths within the ASICs. The vectors will check continuity, stuck-on ones and stuck-on zeros, and shorts for those nets in the data processing path. The results of the applied vectors will be read back into the boundary scan controller via the scan loop and compared with the expected results, also stored in PROM.

The boundary scan controller interprets commands sent through the VME controller to perform the individual JTAG instructions implemented in the ASICs, captures the resulting data, and sends it back to the crate controller on request. Several boundary scan loops will be implemented rather than a single long loop in order to minimize the time required for tests of a specific sections of the logic.

4.8 Outputs

Even at 160 MHz there are a considerable number of outputs to deal with. The Electron Isolation (Electron ID) card directly associated with a given Receiver card must have 32 towers of 7 bit electromagnetic and 4 bit hadronic information per crossing. Transmission of this information requires 176 pins in differential mode. In addition the neighboring cards to the left, right, top, and bottom, as shown in the top half of Figure 7, need 24 towers of 7 bit electromagnetic and 1 bit hadronic veto information per crossing. These neighbors require an additional 96 pins. The corner neighbors must have 1 bit of hadronic veto information and 3 bits of electromagnetic information transmitted each crossing. Since the corner information must go to four separate cards it is necessary to send it at 40 MHz, using 32 pins in differential mode. Finally, two Fine Grain bits, computed by the logical OR of all the Fine Grain bits received in each 4 x 4 region, are sent to the Electron Isolation (Electron ID) card on a single pair of pins. This totals to 306 pins required to transmit data from one Receiver card to several Electron Isolation cards.

The adder tree information is sent to the Jet Summary card. There are two totals, one for each of the 4 x 4 trigger tower regions covered by a Receiver card. These two 12 bit numbers will be multiplexed onto a single set of 12 differential pairs at 160 MHz. One of the remaining two 6.25 nsec data frames is used to transmit the two HAC Feature bits, determined by a logical OR of all the input bits for each of the two 4 x 4 trigger tower regions. The remaining bits in that data frame and all the bits in the fourth 6.25 nsec data frame are presently undefined, but may be used in support of error logging. The total number of output pins required is 330.

4.9 VME Interface

The VME interface is a full implementation of the VME specifications, excluding READ/MODIFY/WRITE. At present only 16 bit transfer modes are implemented. Addressing may be limited to A24 for a more compact hardware implementation, but the final decision has not been made. Interrupts will be supported as these are useful during the boundary scan operations. The implementation of Block Transfers is under consideration. While they could be useful for the memory operations, the extra logic may not be justified.

4.10 Clock Distribution

The on-board clock distribution is still being studied. The initial concept is discussed here. We will continue this development as our experience with the prototypes warrants.

The most successful clock distribution scheme is likely to be one in which the clock travels parallel to the data path towards the outputs on the backplane. All of the trigger data flow on the board is in the direction from the Phase ASIC to board output. Also, there are no re-entrant adds within the adder tree. As long as both the clock and the data take roughly the same path, it can be assumed that the extra delay of clock to data out, plus any combinational logic in the data path, is sufficient to ensure the clock will always arrive far enough ahead of the data at each successive storage element to guarantee hold times at that element. Setup times must be carefully determined since they are easily overrun by too much logic between registers. A second approach would be to distribute the clock from the backplane to the front of the card anti-parallel to the data. We have chosen to implement the first method on the prototype Receiver card.

5 Electron Isolation (ID) Card

The Electron Isolation (Electron ID) Card, shown in figure 12, receives data at 160 MHz in a staged fashion from at most nine Receiver Cards and performs the isolated electron algorithm described in the introduction. Some of the data originates from Receiver cards in neighboring crates, but is transmitted through the local

Receiver cards. The Electron Isolation card is 9U x 280mm and resides in the front of the crate, offset from the Receiver cards by 1.78cm. The electron isolation algorithm is performed on this card and the final results sorted to identify the largest two tower E_t isolated and non-isolated sum from each 4 x 4 region.

The Electron isolation algorithm is implemented in a custom ASIC. One ASIC covers one 4 x 4 region of towers. The results from each ASIC are ranked in two look up tables, then transmitted over the backplane to the Jet Summary card for further processing. The Jet Summary card performs a sort on the data from all eight Electron Isolation cards producing the four largest isolated and non-isolated candidates. These values are forwarded, along with the total E_t , E_x , and E_y information to the global trigger processor.

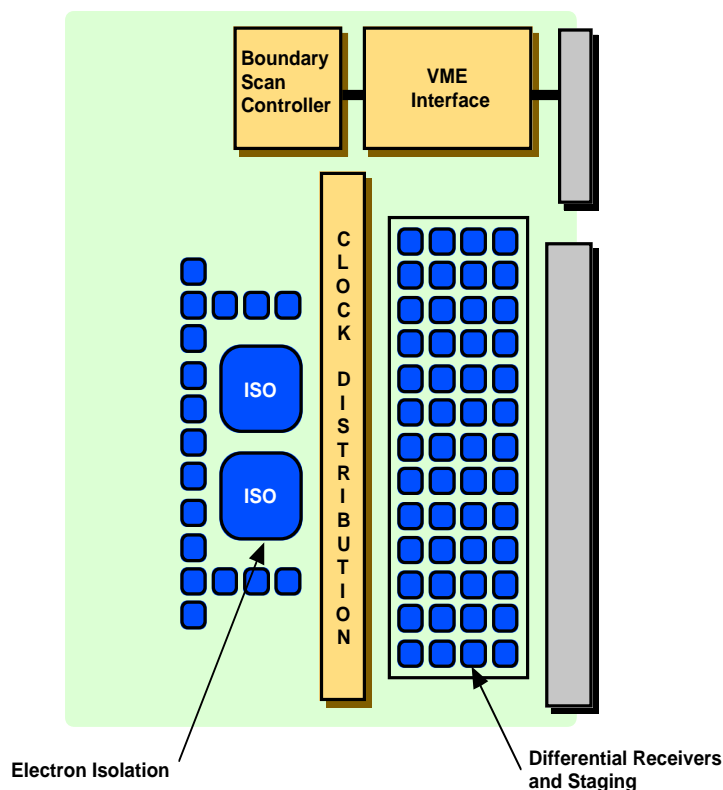


Figure 12. The Electron Isolation Card.

5.1 Inputs

All data received by the Electron Isolation card comes from local Receiver cards in differential mode. Terminations for the lines will be on the cards rather than the backplane. Each card processes 32 towers of electromagnetic and hadronic information organized in a 4 x 8 array. Data is also required from the neighboring 28 towers to determine isolation on the boundaries of the 4 x 8 region. Section 4.8 itemizes the 306 lines required by the Electron Isolation card. A 340 pin AMP stripline connector will be used as the main data connector. The additional pins beyond 306 will be used to forward the results to the Jet Summary card and to input clock and control information. As in the case of the Receiver card, the top part of Electron Isolation card will use a 128 pin DIN connector to interface to a 32 bit VME bus.

5.2 Isolation

The input data is staged on the Receiver card to arrive in a particular order in time at the Electron Isolation card. Careful data organization makes it possible to process the data as it is being received, rather than storing it for a full crossing to use in parallel on the card. The Isolation ASIC is designed to shift in the data for 16 towers, 4 towers at a time, over a single bunch crossing time. The data for the 20 neighboring towers is loaded in the same time period. The entire 4 x 8 region is processed by two ASICs in twelve 160 MHz cycles. A detailed description of the order of the data is given in the next section.

The algorithm used to determine isolation examines the individual sums of a reference tower with each of its four nearest neighbors. The maximum sum is chosen and several cuts are applied on the longitudinal and

transverse isolation of the ECAL energy deposit. The first cut, the HAC Veto, requires the central tower HCAL to ECAL energy ratio to be < 0.05 when ECAL energy is significant. The cut on transverse isolation requires the OR of HAC Veto bits in the eight nearest neighbors to be zero. In order to reduce the number of bits exchanged between cards we may use a simple thresholding to compute the HAC Veto for shared towers. A second cut on transverse isolation, the EM Veto, examines the electromagnetic energy deposited in four 5 tower groups centered on each of the corners. The EM energy entering the ASIC is thresholded against a programmable 3 bit value (.5 GeV resolution). The resulting bits are ORed in groups of 5 for each corner and these four results ANDed together to form the central tower's EM Veto bit.

The output of the ASIC is the maximum 2-tower sum, with seven bits of dynamic range, along with its associated HAC Veto bit, the neighbor HAC Veto bit, and the EM Veto bit. These results are produced every 25 nsec. They are combined with the 4×4 region's Fine Grain bit and passed on to two look up tables which produce two 6 bit ranks. One rank is an isolated electromagnetic candidate and the other is a non-isolated electromagnetic candidate. The two 4×4 regions produce a total of four 6 bit ranks which are sent, via the backplane, to the Jet Summary card.

5.2.1 Isolation ASIC

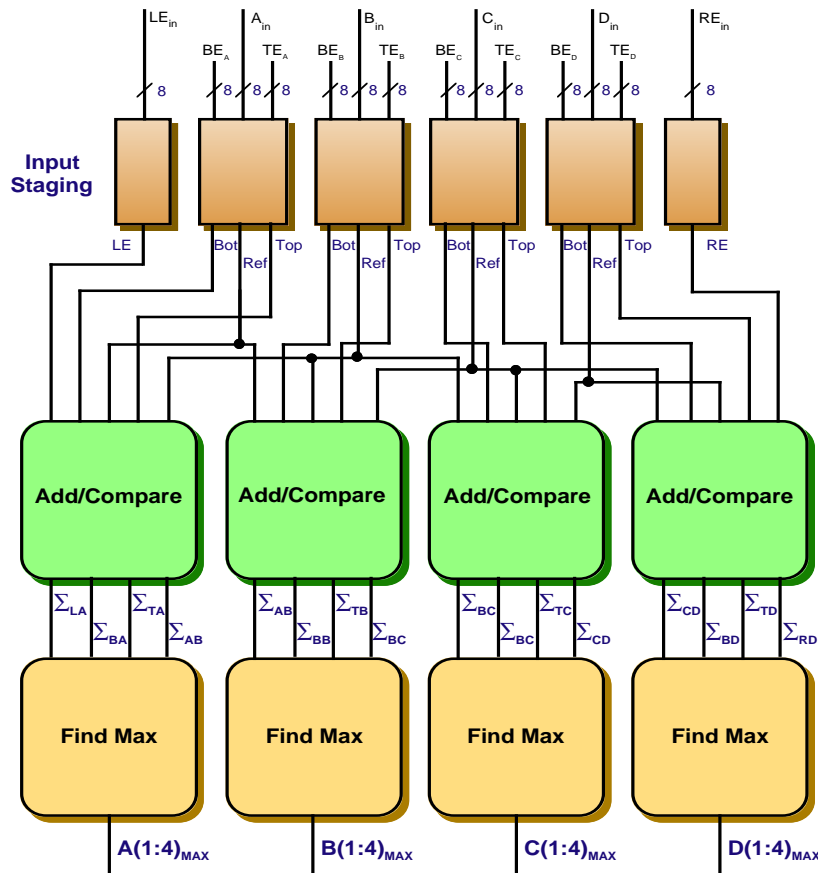


Figure 13. Block diagram of the Electron Isolation ASIC.

The Isolation ASIC, shown in Figure 13, handles four electromagnetic energies on an 7 bit scale along with the corresponding HAC Veto bit, every 6.25 nsec. These inputs are designated as A_{in} , B_{in} , C_{in} , and D_{in} in the figure. Nearest neighbors are also included in the data flow. During the first cycle of every crossing the four neighboring energies (TE_A , TE_B , TE_C , TE_D) from the adjacent 4×4 region (top) are also be strobed into the ASIC. The neighbors along either edge of the 4×4 region (LE_{in} , RE_{in}) are also included, two at a time (left and right edges), during each 6.25 nsec period. Finally, the last cycle strobes in the four neighboring towers of the bottom edge (BE_A , BE_B , BE_C , BE_D). Thus, in one bunch crossing time, a total of 36 towers are clocked into the Isolation ASIC.

Separate inputs are used to clock in the top and bottom neighboring towers in order to avoid unfavorable routing or extra components on the board due to board level multiplexing. The top and bottom neighboring edges require a total of $2 \times 4 \times 8 = 64$ input pins. The central region needs $4 \times 8 = 32$ input pins, and the left and right edges need $2 \times 8 = 16$ pins. The total number of data inputs is 112 pins, for 36 towers of information. In addition pins are allocated for three bits of EM threshold, reset, and clock inputs. All signal I/O, with the exception of the clock, is single-ended.

Figure 13 does not show a stage of logic added recently to determine the single maximum two tower sum for the full 4×4 region. This is accomplished by comparing the four values output by the Find Max block to determine the largest of the four values in each 6.25 ns time frame and retaining the largest of four values generated over the four 6.25 ns cycles required to process the region. The neighbor EM Veto block diagram is presented in a later section. The HAC neighbor Veto and EM Veto computations are performed within the ASIC in parallel with the max two tower logic.

5.2.1.1 Input Staging

The main data flow of the Isolation ASIC processes the data through three separate blocks. The first of these, the Input Staging, is illustrated in Figure 14. The purpose of this block is to receive the data at the time when it is available and change the time relationship to one suitable for the processing that follows. Only one column of input data is represented in the figure.

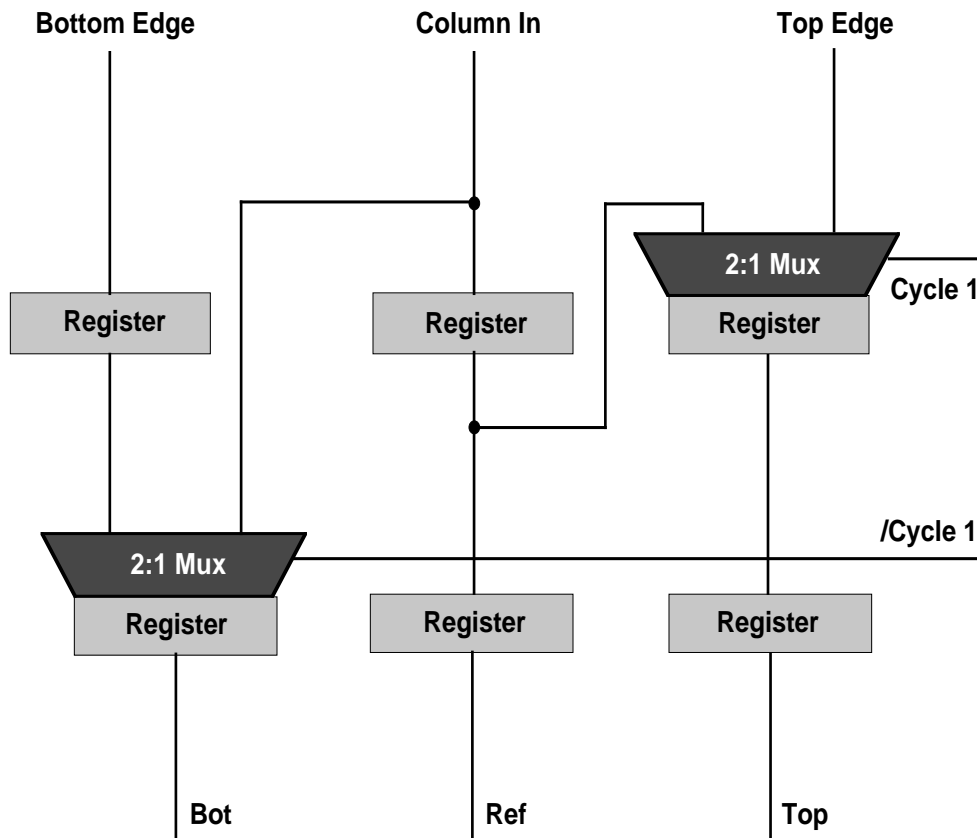


Figure 14. Isolation ASIC input staging.

At the beginning of a crossing, the first row of the 4×4 array is available, along with the top edge. The signal **Cycle 1** selects the **Top Edge** input on the right hand multiplexer. After the first 6.25 nsec clock, the first rank of registers contain one of the towers in the 4×4 array (a reference tower) along with its top neighbor. The left-most register in the top rank is undefined at the beginning of the sequence. After a second clock cycle, the reference tower is in the middle register of the bottom rank of registers and its top neighbor is in the right hand register. The left-most register in the bottom rank contains the next successive reference tower, as does the middle register in the top rank. This value is the bottom nearest neighbor for the first reference tower. The

sequence continues through to the cycle where the last reference tower in a column of 4 towers is clocked into the middle register in the bottom rank. During the same cycle the **Bottom Edge** data is available from the neighboring card. It is clocked into the bottom left register during **Cycle 1** at the beginning of the next sequence.

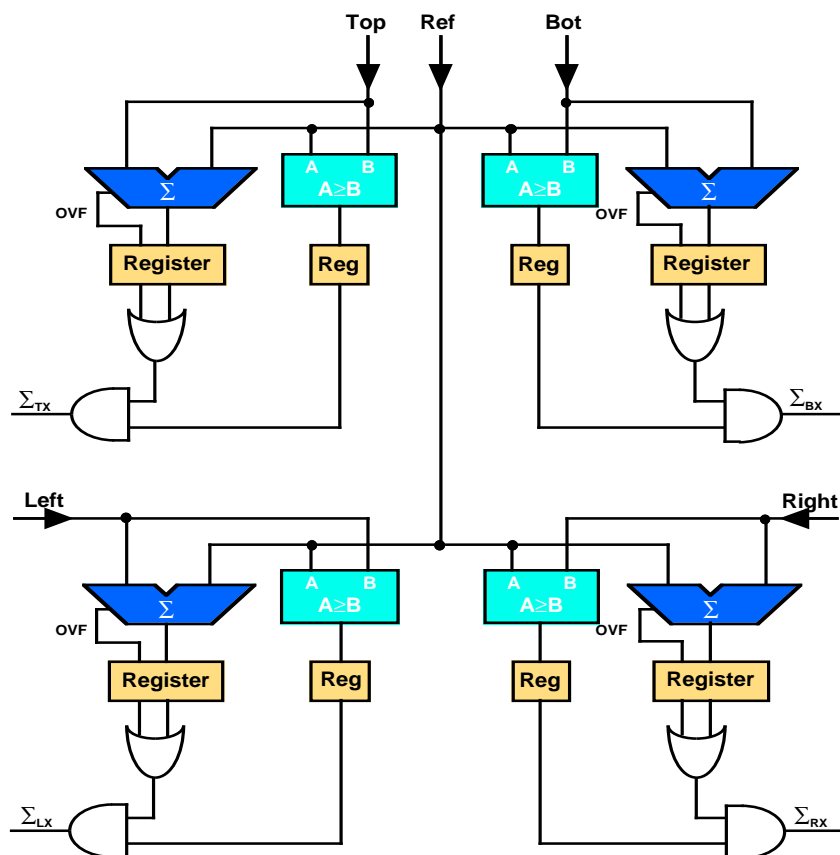


Figure 15. Electron Isolation ASIC Add/Compare block.

Once the pipeline has been filled, data will continue to be output from the Input Staging block four towers at a time each with their corresponding top and bottom neighbor. The left and right neighbors are either the adjacent reference towers in the 4 x 4 array or the left and right columns of data from neighboring boards.

5.2.1.2 Add/Compare

The Input Staging block places each reference tower and its neighbors in the same time frame. The remaining blocks in the chip can now handle the processing in parallel. The function of the Add/Compare block, shown in Figure 15, is to form four sums between a reference tower and its top, bottom, left and right neighbors. At the same time the sums are being formed, four compares are made to determine for each pair of towers whether the reference tower is larger than or equal to its neighbor (“equality check”).

When a reference tower and its neighbor satisfy the “equality check” the sum of the pair is enabled to the Find Max block. When the sum is disabled, a value of zero is passed on to the next block. If the adder has overflowed (carry out equals one) the results of the addition are set to 7FH.

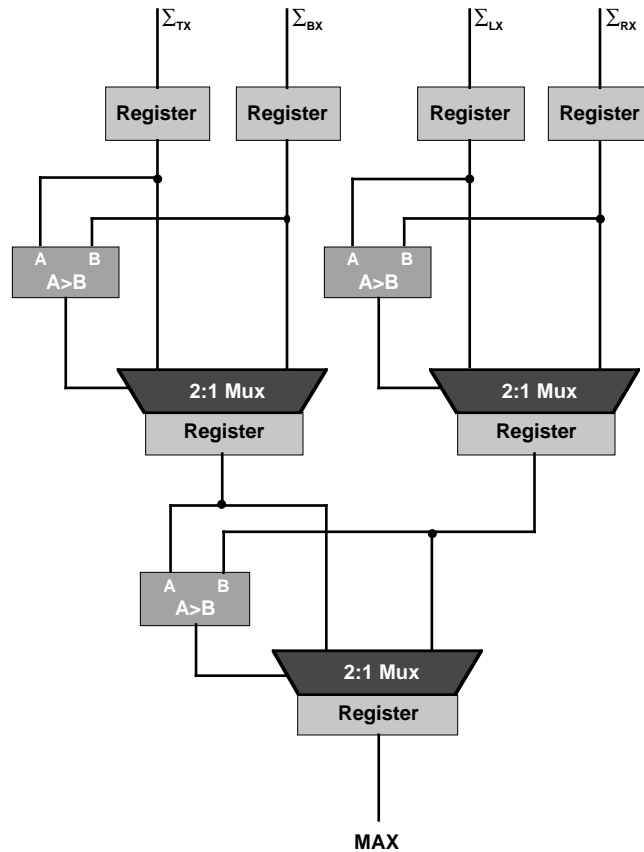


Figure 16. Electron Isolation ASIC block which determines the maximum pair.

5.2.1.3 Find Max

The next to last stage in processing the electromagnetic information, the Find Max block, is shown in Figure 16. The four sums (Σ_{TX} , Σ_{BX} , Σ_{LX} , and Σ_{RX}) are presented, in parallel, to two comparators. The outputs of these comparators are used to select the maximum of each pair which are placed in intermediate storage. These two maxima are presented to a single comparator during the next clock cycle. The output of this comparator is the maximum two tower sum for an individual reference tower. The single maximum from the original four values is stored in the bottom register shown in Figure 16. The HAC Veto, neighbor HAC Veto, and neighbor EM Veto are stored with each of these sums. A final stage of logic sorts through all 16 maxima generated over a bunch crossing time and places that value, along with its Vetos, on the outputs of the ASIC. The total latency for the electromagnetic data path is 12×6.25 nsec or 3.0 bunch crossing times.

5.2.1.4 Nearest Neighbor Hadronic and E_t Vetos

A tower's hadronic Veto enters the ASIC in the same time frame as the 7 bit E_t information. The same staging circuitry used to equal time the neighbor E_t information for a single reference tower is also used to put the HAC Vetos into the proper time sequence. Once all eight neighbors are timed in an eight way OR is performed to arrive at the HAC neighbor Veto.

The EM neighbor Veto requires a little more processing than that used on the HAC neighbor Veto. The E_t information has already been timed in by the staging circuitry. It is presented to a bank of comparators where each value is compared against the same three bit threshold. The single bit results from each of the compares is passed on to a large OR - AND array. The ORs check that each group of five towers, centered on one corner of a reference tower, are all below threshold. The ANDs gather the four results from the ORs for each reference tower and form the AND. If any one corner of the five tower ORs has a value of zero, the AND (EM Veto) will be zero. Figure 17 illustrates the section of the chip that checks the EM neighbor isolation.

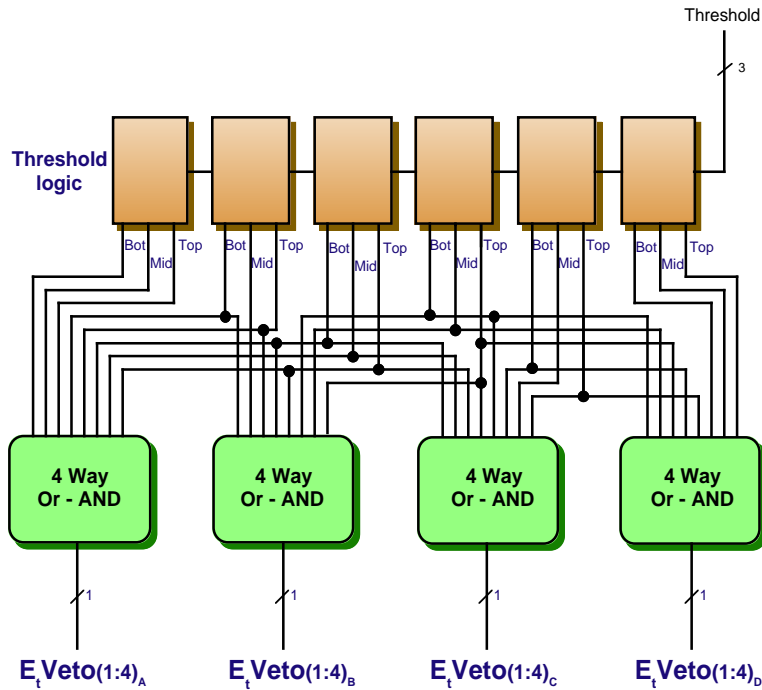


Figure 17. Electron Isolation ASIC Hadronic isolation block.

The results from the EM Veto logic are produced ahead of the two tower sums and must be delayed within the ASIC by two clock cycles. This Veto, along with the HAC neighbor veto and HAC veto, is appended to the two tower E_t sum before it enters the Max tower circuitry. The result from the Max tower block has the correct Veto information associated with it and all 10 bits are placed on the outputs of the Electron Isolation ASIC.

5.2.1.5 Boundary Scan

We have implemented the same controller and instruction decoder for boundary scan as used in the Adder ASIC. All ASICs in the Level 1 trigger processor will have compatible boundary scan circuits.

5.3 Lookup Tables

Space is limited on the Receiver card, so we may find it necessary to put the H/E lookup tables on the Electron Isolation card. This look up must be performed before the E_t data enters the Electron Isolation ASIC to produce the HAC Veto bit used within the ASIC. Eight memories will be used to cover the two 4×4 regions. The address to each memory is comprised of the top four bits of electromagnetic E_t and the bottom four bits of hadronic E_t . Since data is entering the card and ASIC at 160 MHz, the memories must operate at the same speed. While this approach (as opposed to forming H/E on the Receiver card) requires more pins on the backplane connector, it does reduce the number of look up tables on the Receiver card as well as some problems associated with bussing the address bits to so many different locations. HAC Veto bits from neighboring towers will be formed on their respective Receiver cards by applying a simple threshold on the hadronic energy.

A second set of lookup tables is used to produce a ranking of the electron trigger information based on the 7-bit two tower sums, HAC Veto bit, HAC neighbor Veto bit, and the EM Veto bit from each Isolation ASIC. The Fine Grain bits associated with each 4×4 region are appended to these 10 bits and the resulting 11 bits used to address two memory look up tables. Each look up table produces a separate data stream, one for isolated electrons, the other for non-isolated electrons. The data from each 4×4 region is multiplexed into each look up memory at 80 MHz. The 6 bits of output from each of the look up memories is merged into a single 160 MHz data stream. This data is sent to the Jet Summary card, over 12 lines, for final sorting.

5.4 VME Interface

The VME interface is a full implementation of the VME specifications, excluding READ/MODIFY/WRITE. At present only 16 bit transfer modes are implemented. Interrupts will be supported as these are useful during the boundary scan operations. The implementation of Block Transfers is under consideration. While they may be useful for the memory operations, the extra logic may not be justified.

5.5 Outputs

Each Electron Isolation (Electron ID) card produces four ranked trigger category values 6 bits in length – two isolated and two non-isolated. These results are produced once every 25 nsec crossing. Every 6.25 nsec one of the values is placed on the backplane using a set of 6 differential pairs. All four values are transmitted to the Jet Summary card during the period of one crossing. These 12 lines, together with the 306 input lines noted above, use 318 pins on the 340 pin connector. Additional pins will be used for clock, controls, and status information.

6 Jet Summary Card

The Jet Summary card sits near the middle of the trigger data processing section of each regional trigger processing crate. It is shown in Figure 3 situated in the front portion of the crate between the 4th and 5th Electron Isolation cards. It collects and summarizes data from both the Receiver cards and the Electron Isolation cards at 160 MHz. The Jet Summary card has the same form factor as the Electron Isolation card, 9U x 280mm. It has a VME interface via a 128 pin, 4 row DIN connector. The trigger data is received on an AMP 340 pin stripline connector. A block diagram of the card is provided in Figure 18.

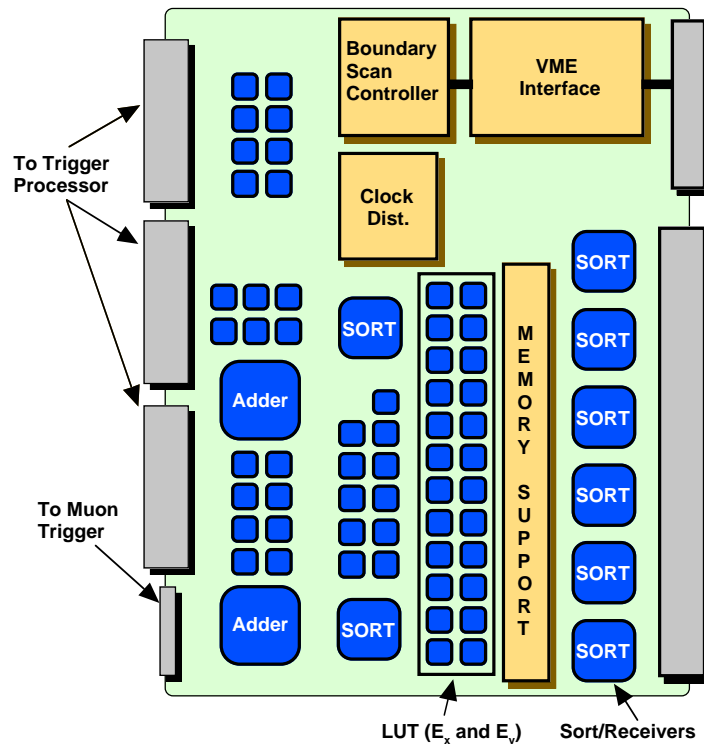


Figure 18. Jet Summary card.

The electron trigger rank information from eight Electron Isolation cards (32 values) is sorted to produce the four highest ranked isolated and non-isolated electron candidates. These values have a 4-bit address appended to them which indicates which 4 x 4 trigger tower region, covered by the crate, produced them. The E_T information from the Receiver cards is also on a 4 x 4 tower resolution. These values are summed by a pair of Adder ASICs to produce a total E_T sum. The input E_T values are processed by Sort ASICs to determine the four largest E_T values produced by the crate. This is used as the jet trigger. The E_T information from the Receiver card is also sent to memory lookup tables which generate E_X and E_Y for each 4 x 4 region. The E_X and E_Y values are summed individually in Adder ASICs to produce total E_X and E_Y for the 256 tower region of the calorimeter covered by the crate.

6.1 Inputs

Each of the eight Electron Isolation cards transmits 6 bits of trigger rank every 6.25 nsec in differential mode. Therefore, the Jet Summary card receives 6 differential pairs from each Electron Isolation card for a total of 96 input pins.

The Receiver cards send the 12 bits of E_T information for the two 4 x 4 trigger tower regions differentially on 24 lines. This data is transmitted at 160 MHz, requiring two 6.25 nsec time frames. The third 6.25 nsec time frame contains the HAC Feature information for the two 4 x 4 regions. The remaining bits in the third and fourth 6.25 nsec time frames are reserved for future assignment. The Jet Summary card receives this data from the eight Receiver cards on 192 input pins. Therefore, the total number of signal pins dedicated to trigger data is 288.

6.2 Sort

In order to limit the amount of information transmitted from the Jet Summary card to the Calorimeter Global Trigger Processor, we have chosen to send only the four highest ranked trigger categories from each crate. Thus we require a sort function to reduce the large amount of information coming into the Jet Summary card. The trigger categories to be sorted are the Isolated electron candidates, the Non-isolated electron candidates, and the 4 x 4 region Jets. The energy sums do not require sorting. In order to minimize the sort circuitry the four values produced by the sort function are not themselves ordered. The final ordering is left for the Global Trigger Processor to perform.

6.2.1 Sort ASIC

The Sort ASIC will have differential inputs so that data may be received directly from the backplane. This will reduce the amount of receiver logic on the Jet Summary card and allow us to use the JTAG Boundary Scan built into the ASIC to do backplane testing and to set up test data for the board itself. In addition to the data inputs we need three bits of positional information to tag the location of the 4 x 4 region providing each piece of data. These bits will be differential as well so that we may use the Sort ASIC in another application described below.

The Sort ASIC is designed to find the four largest of eight 6-bit values. Six bits is sufficient to handle both the E_T sums and the electron candidates. Figure 19 is an illustration of the major functional blocks that make up the ASIC. Rather than try to design an ASIC that will handle eight 6-bit operands in parallel, it was decided to shift the data in, four operands at a time, over two 6.25 nsec cycles. The electron candidates come from the Electron Isolation card in two groups of two. The first group will be the Isolated electrons, and the second group will be the Non-isolated electrons. The two groups are separated in time within the ASIC with the results of a sort appearing every 12.5 ns. In the case of the E_t energy sums, the two regions are received from each Receiver card by the Sort ASIC in successive 6.25 ns cycles. The results from this sort appear at the output of the ASIC once every bunch crossing.

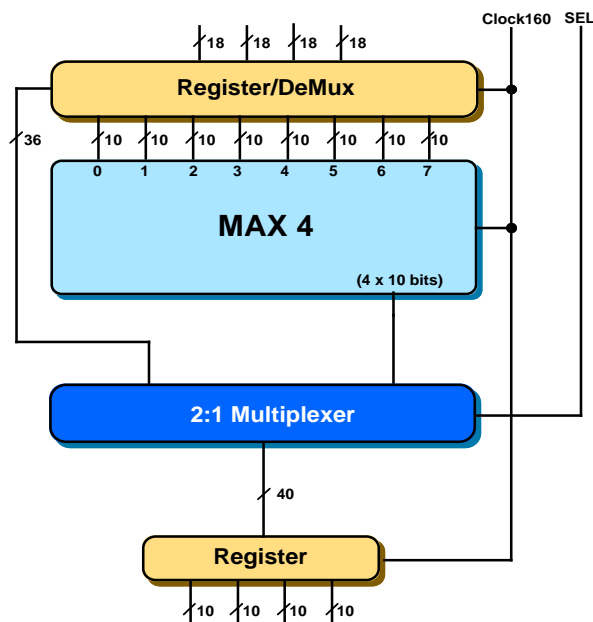


Figure 19. Sort ASIC block diagram.

Two ASICs are required to receive the data from the Electron Isolation cards and four more are required to handle the data from the Receiver card. Each pair of ASICs generates eight values. These eight values will be muxed together in pairs and each fed into a single Sort ASIC to produce the final set of four max values. The outputs from the Sort ASIC are the four largest 6 bit values along with 4 bits each of positional information. These results are single-ended.

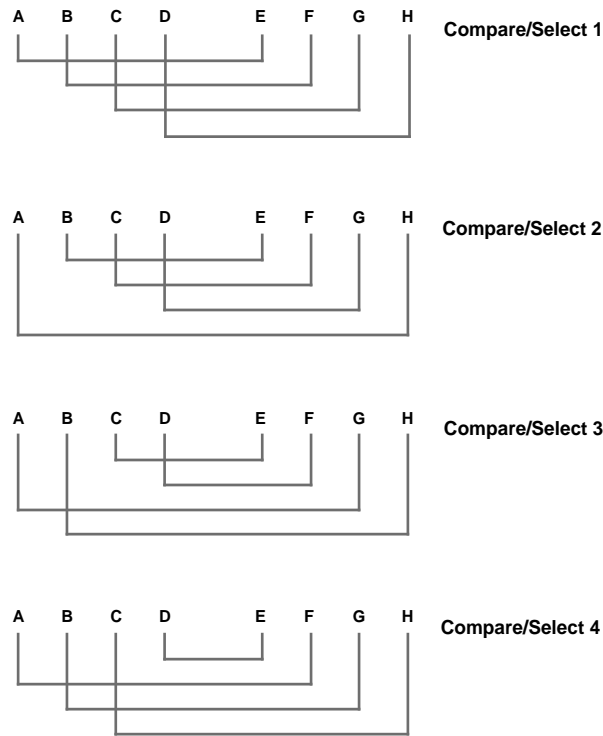


Figure 20 Sort ASIC compare pattern.

The algorithm implemented within the Sort ASIC is based on a simple rotation of operands and is shown schematically in Figure 20. The eight operands are divided into two groups of four. The operands are compared in pairs between the two groups, with the larger of the two taking over the position of the left hand member of the pair. This comparison is performed in four stages with a rotation of compared pairs occurring between each stage. By the end of the fourth stage a sufficient number of comparisons have been made to ensure the four largest values are in the left-hand group. In order to save steps, and thus minimize the total latency, these four values are not placed in any rank order. The final four values, produced by the Calorimeter Global Trigger Processor, are ordered during the final sort.

6.2.1.1 Register/DeMux

The first functional block of the Sort ASIC is the Register/DeMux. The main purpose of this block is to provide storage for the incoming data to isolate it from board propagation delays. It also stages two cycles of 4 operands into a parallel data path of 8 operands. In addition a single bit of position information is appended to the three bits of positional information entering the ASIC along with the data. This bit is appended, if enabled, during the second cycle of data input. The addition of this bit will be enabled for the Sort ASICs in the second level of sort.

6.2.1.2 MAX4

The next block in the sequence is the MAX4 block. A more detailed picture is given in Figure 21. The MAX4 block is made up of four Compare/Select blocks. One of the Compare/Select blocks is illustrated in greater detail in Figure 22. Each of the four blocks is different from its neighbor in that each has one of the four stages of pairing, shown in Figure 20, hardwired in the circuit.

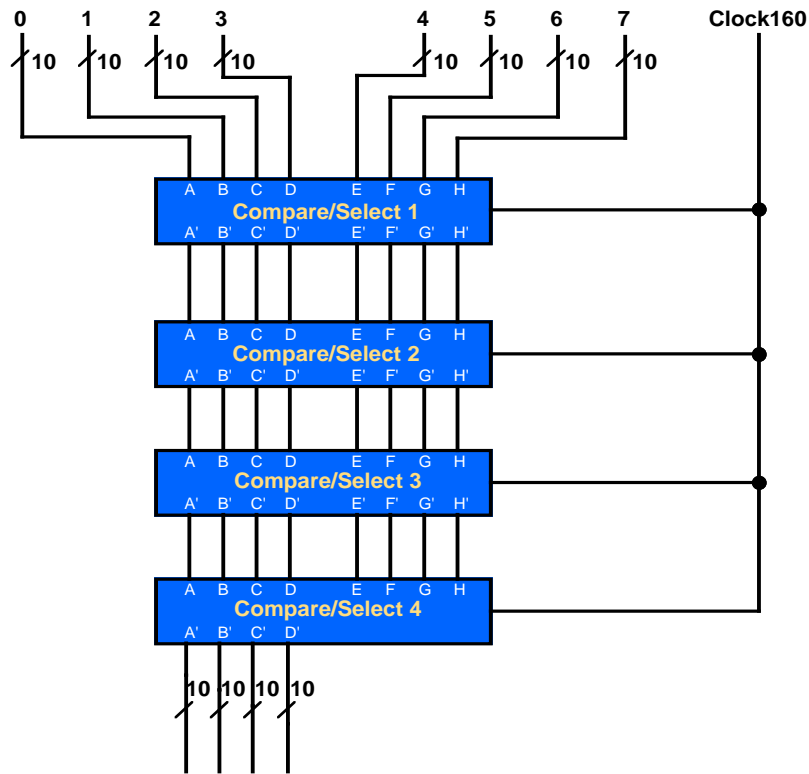


Figure 21. Sort ASIC MAX4 block diagram.

The Compare/Select block performs all four compares in parallel. Ten bits arrive and leave at the inputs and outputs. The top four bits are the positional information mentioned above. They are carried along with the data through the 2:1 multiplexers. The bottom six bits (raw data) are used by the compare to drive the select lines of the multiplexers. Each pair of multiplexers has the same operand wired to opposite inputs. The results from the compare force the left hand multiplexer to store the larger of the two values and the right hand multiplexer to store the smaller of the two. After one 6.25 nsec clock cycle the eight operands have been reorganized with the larger of each pair of values stored in the registers in the left hand column.

During the next three 6.25 nsec clock cycles the data is passed through the remaining three Compare/Select circuits. Only the left four operands are saved at the end as they contain the four maxima of the original eight operands. The output of the MAX4 block is sent on to a 2:1 Multiplexer. The Multiplexer is used to bypass the sort circuit. This feature is useful in handling the energy sums from the Receiver card. The input data requires two cycles to enter the ASIC. The sorted results only require one cycle to exit the ASIC. The multiplexer is used to pass the input data (two cycles worth) directly to the outputs of the ASIC before the sorted information is available. The two input operands are sent to memory look up tables and generate E_x and E_y values for each 4 x 4 region. They also are used in the E_t adder tree to complete the energy sum for the crate. When the sorted values are available they are received, along with data from the second Sort ASIC of the pair, by a third Sort ASIC. The third ASIC completes the sort of the original 16 values.

In the case of the sort of electron candidates the inputs are used in all four cycles. The sort reduces data so that only two cycles are needed for the output data. One cycle produces four Isolated candidates, the other produces four Non-isolated candidates. Two Sort ASICs produce eight values (Isolated or Non-isolated) in the same cycle at 80 MHz. These values are Muxed at 160 MHz into a third Sort ASIC. The output from this last ASIC produces four sorted Isolated electron candidates and four Non-isolated electron candidates on two cycles every bunch crossing.

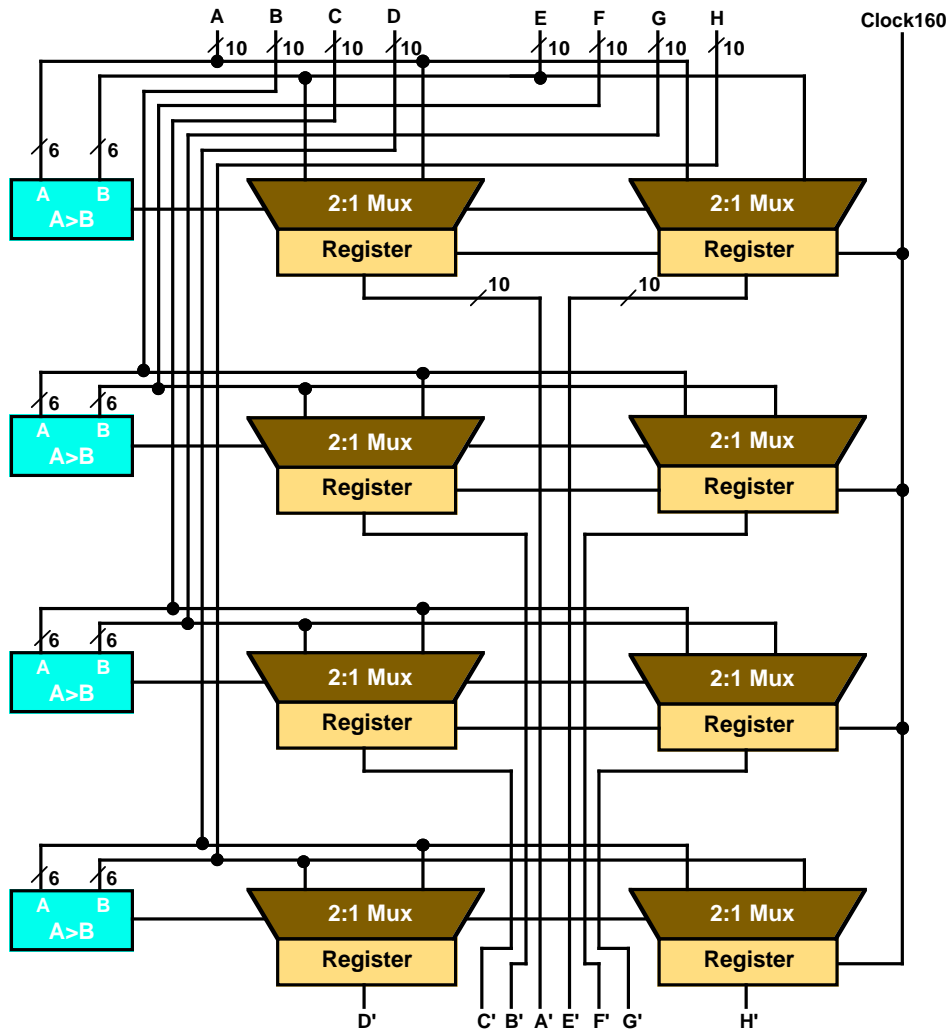


Figure 22. Typical Sort ASIC Compare/Select block.

The portion of E_t energy not used in the sort must also be received on the Jet Summary card and used in the formation of E_x , E_y , and E_t sums. The simplest way to receive this data is to use two more Sort ASICs with the multiplexer set to permanently bypass the sorting logic. The Sort ASIC then becomes a differential receiver with JTAG Boundary Scan on all the inputs and outputs.

The economics of the situation suggest that we should use this ASIC to receive the input data on the Electron Isolation card as well. In this case the positional information is unnecessary so those inputs can be used as additional data inputs.

6.2.1.3 Boundary Scan

We intend to implement the same controller and instruction decoder for boundary scan as used in the Adder and Isolation ASICs. All ASICs in the Level 1 trigger processor will have compatible boundary scan circuits.

6.3 Outputs

The outputs from the Jet Summary card are placed on connectors at the front edge of the card. Transmission is differential ECL via twisted pair cable at 40 MHz. Four connectors are shown in Figure 18, one to the Muon Trigger and three to the Calorimeter Global Trigger Processor. The present design is not detailed enough to define the actual number of connectors we will use due to uncertainties in connector size and segmentation of data within the Calorimeter Global Trigger Processor system.

In the present design we send 12 bits of E_t (10 bits of energy with 2 bits of overflow) and 12 bits each of E_x and E_y (11 bits of signed energy with 1 bit of arithmetic overflow) for crate wide energy totals. The ranked electron candidates are sent as 6 bits of rank with 4 bits of position information. Four Isolated and four Non-isolated

electron candidates total to 80 bits of information. The four ranked region Jets also each require 6 bits of value and 4 bits of position for a total of 40 bits. Finally we have reserved 2 channels of Tau information at 10 bits per channel. The total number of bits going to the Global Trigger Processor is 176. Additional error summary bits and bunch crossing information is likely.

The bottom connector is for the Muon Trigger and contains a map of the HAC Feature bits (one bit per 4 x 4 region).

7 Latency

The overall latency of the level 1 calorimeter trigger regional logic design described in this document is approximately 19 crossings, or 375 nsec. This latency follows a latency of 4 crossings after the interaction for the physics signals to propagate to the calorimeter front-end electronics, 18 crossings to account for the maximum possible fiber optic cable length of 90 m for transmission of the data from the detector to the readout electronics in the electronics barracks, 13 crossings for processing by the calorimeter front end electronics. Another 4 crossings are required to transmit the data from the readout electronics to the calorimeter regional trigger logic. We estimate that the transmission of the output of the regional logic information to the Calorimeter Global Calorimeter Trigger Processor will take another 4 crossings (including one crossing for synchronization). The result is that the calorimeter trigger information is provided at the input of the global calorimeter trigger approximately 62 crossings after the interaction occurred.

The 19 crossing latency of the regional calorimeter trigger logic is divided amongst several stages. Since the logic is mostly clocked at 160 MHz, the operations are composed of 6.25 nsec cycles, four of which add up to a single 25 nsec crossing time. The Receiver card uses 6.25 crossings to process data. This includes the time for the serial data to enter the receiver chip, re-phasing of the data with the local clocks, intercrate sharing, and staging for the backplane. Transmission over the backplane requires .25 of a crossing. The Electron Isolation card uses 4.5 crossings to complete its processing before forwarding the data to the Jet Summary card. The sort path on the Jet Summary card requires the longest time on the card. This path, from card input to card output takes 4.0 crossings. We have added an additional 4 crossings of latency to the calorimeter regional trigger logic to allow for all foreseeable changes in the design.

References

- [1] J. Varela *et al.*, Preliminary specification of the baseline calorimeter trigger algorithms, CMS-TN/96-010.
- [2] S. Dasu *et al.*, CMS Level-1 Calorimeter Detailed Simulation, CMS Note 1998/027, and references therein.
- [3] J. Lackey *et al.*, CMS Calorimeter Level 1 Trigger Conceptual Design, CMS-TN/94-284.
- [4] B.G. Taylor, RD-12. Timing, Trigger and Control Distribution for LHC Detectors, ECP Division Working Document.
- [5] CMS Electromagnetic Calorimeter Technical Design Report, CERN/LHCC 97-33.
- [6] CMS Hadronic Calorimeter Technical Design Report, CERN/LHCC 97-31.