Trigger Subsystem Summary

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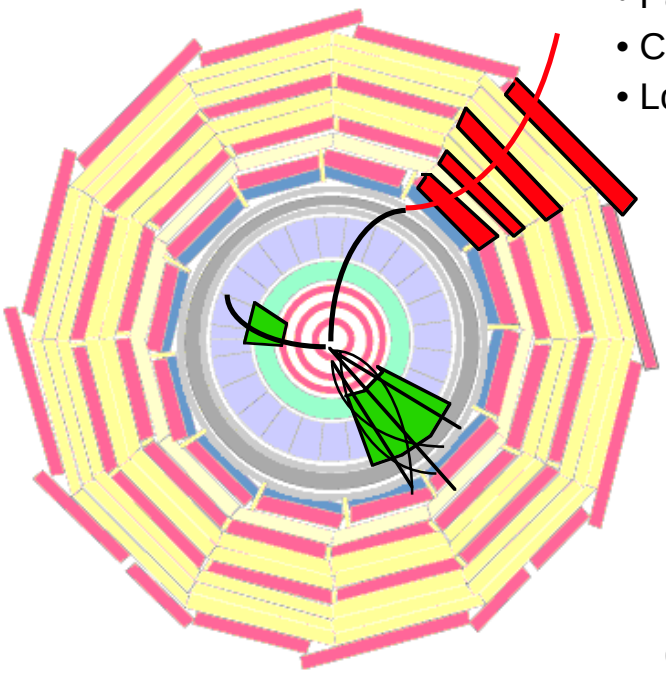
CMS Trigger Project Manager

Outline:

- System Overview
- Organization
- Milestones
- Status and Progress
- WBS Summary
- Schedule (MS Project) summary
- Manpower Profile
- Obligation Profile
- Concerns and actions taken

CMS Trigger Levels

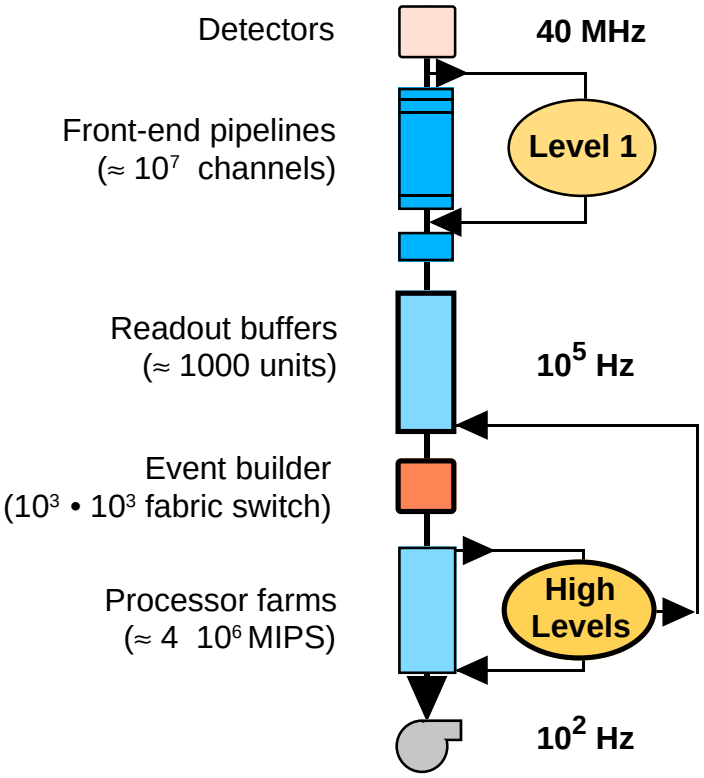
40 MHz

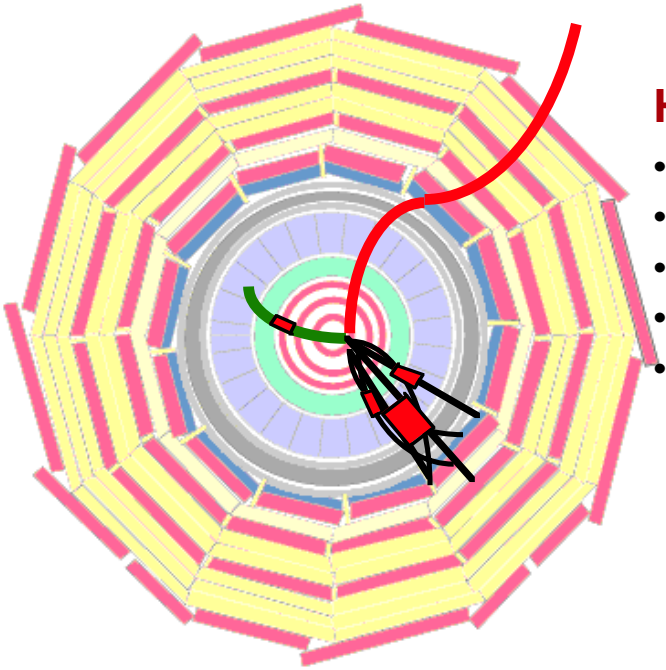


up to 100 kHz

Level-1. Specialized processors

- Particle ID: electron/γ, muon, jets, missing E_T
- Coarse granularity to reduce data volume
- Local pattern recognition and energy sums

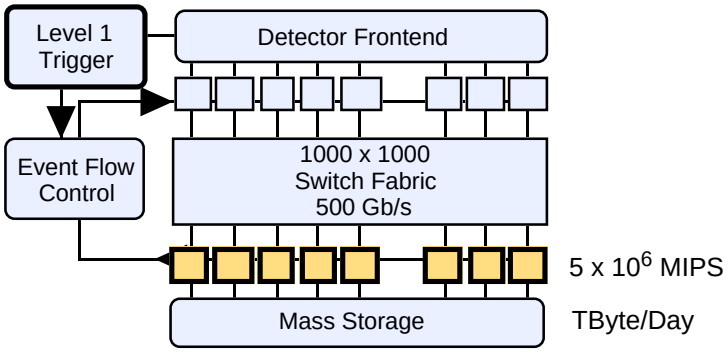




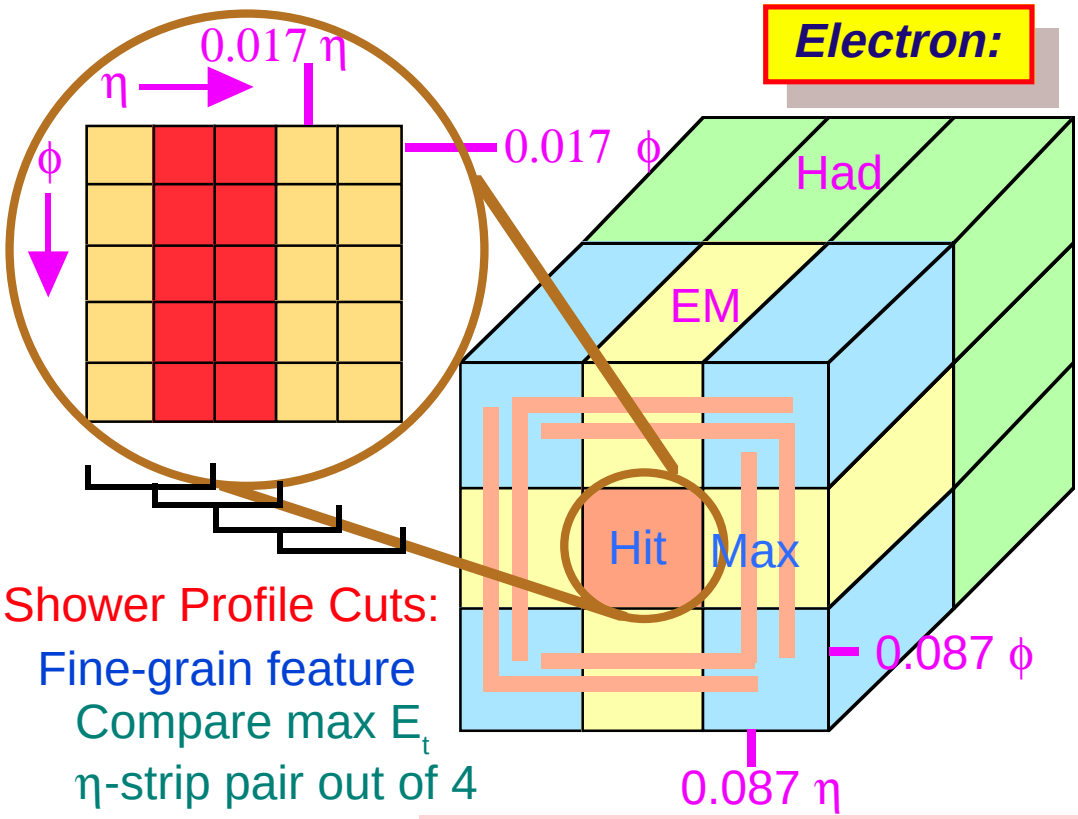
≈ 100 Hz

High trigger levels. CPU farms

- Clean particle signature (Z, W, quarks..)
- Finer granularity precise measurement
- Kinematics. Effective mass cuts and topology
- Track reconstruction and detector matching
- Event reconstruction and analysis



Electron & Jet Triggers



Electron:

3 x 3 sliding window centered on ECAL/HCAL trigger tower pairs
Tower count = 72ϕ x 54η x 2 = 7776

Shower Profile Cuts:

Fine-grain feature
Compare max E_t η-strip pair out of 4 pairs vs. total E_t

HAC Veto
Compare HCAL versus ECAL E_t

Candidate Energy:

Max — Max E_t of 4 Neighbors

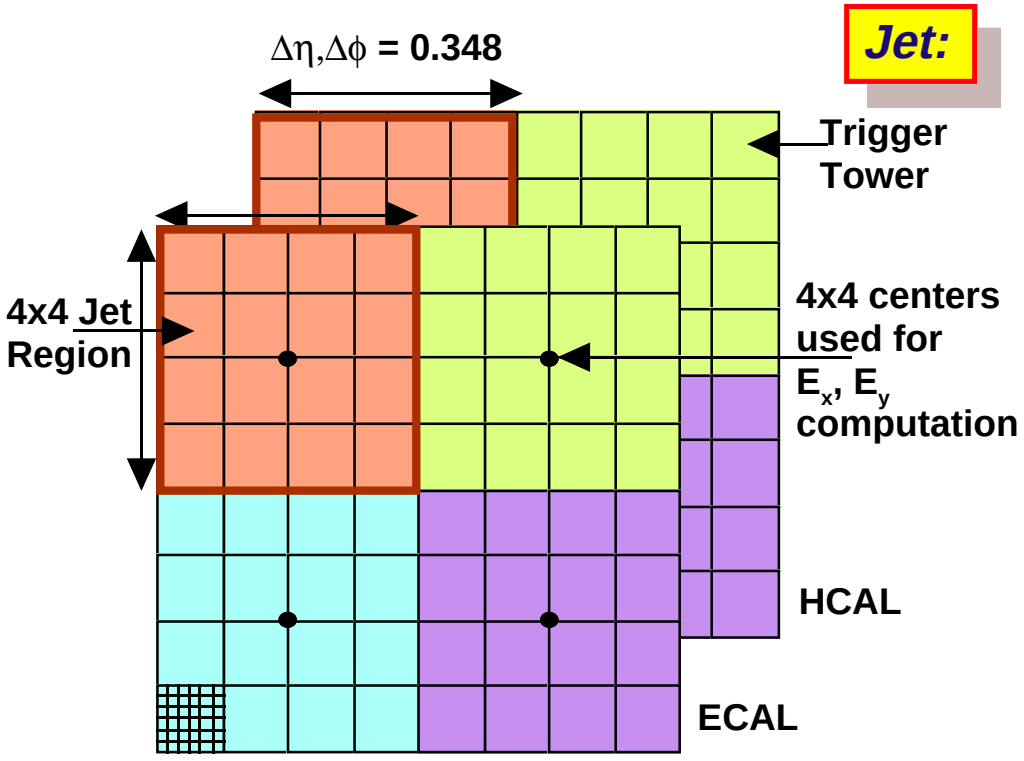
Hit — Hit + Max E_t > Thrsh

Isolation Cuts:

Neighbor HAC Veto
HAC Veto passes on all 8 neighbors.

Neighbor E_t Veto
Σ_5 Neighbors E_t
At least one of four corners has $\Sigma_5 E_t$ < 1.0 GeV

Jet:

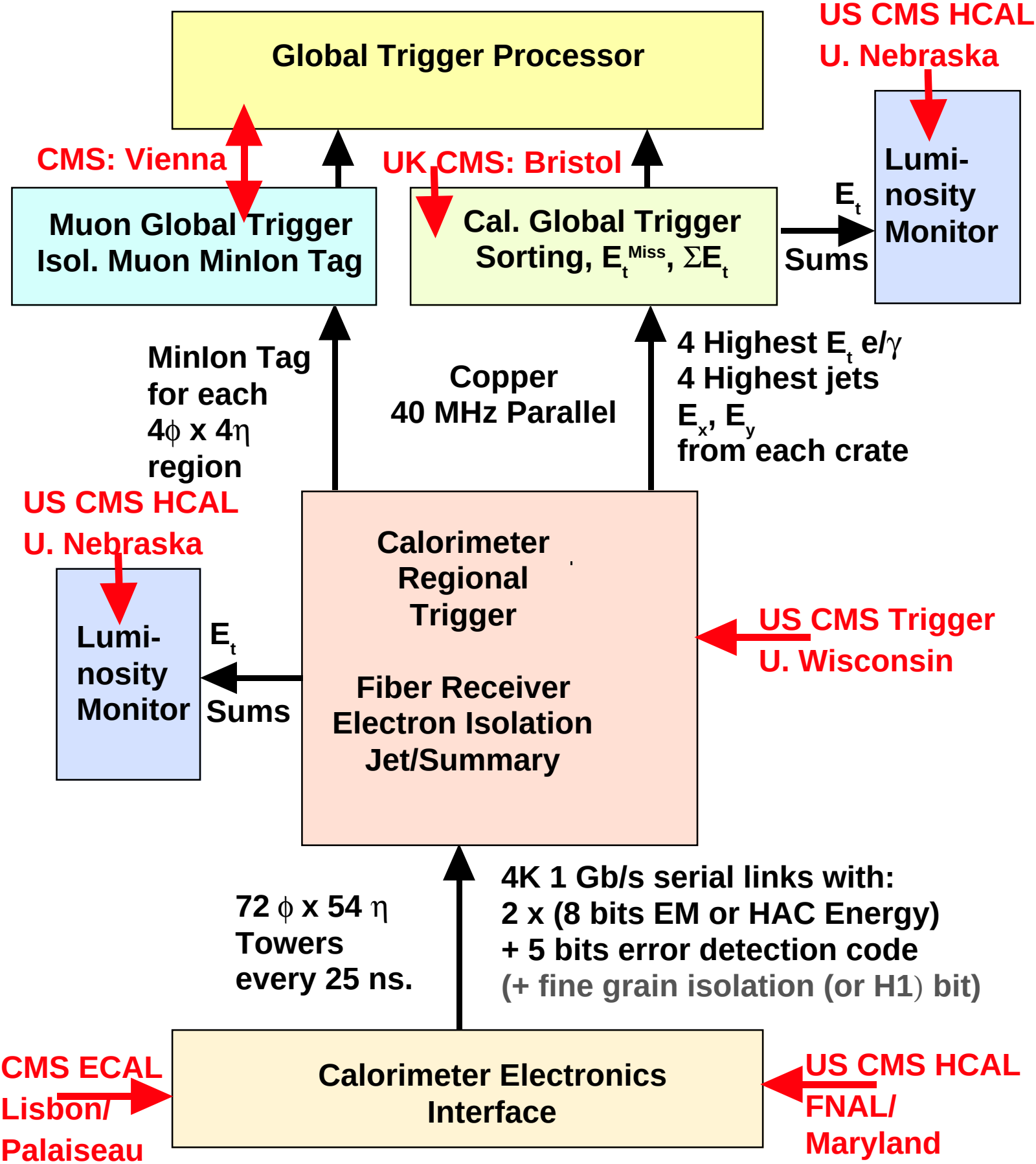


Jet E_t from sum of ECAL& HCAL trigger tower E_t in non-overlapping 4x4 regions

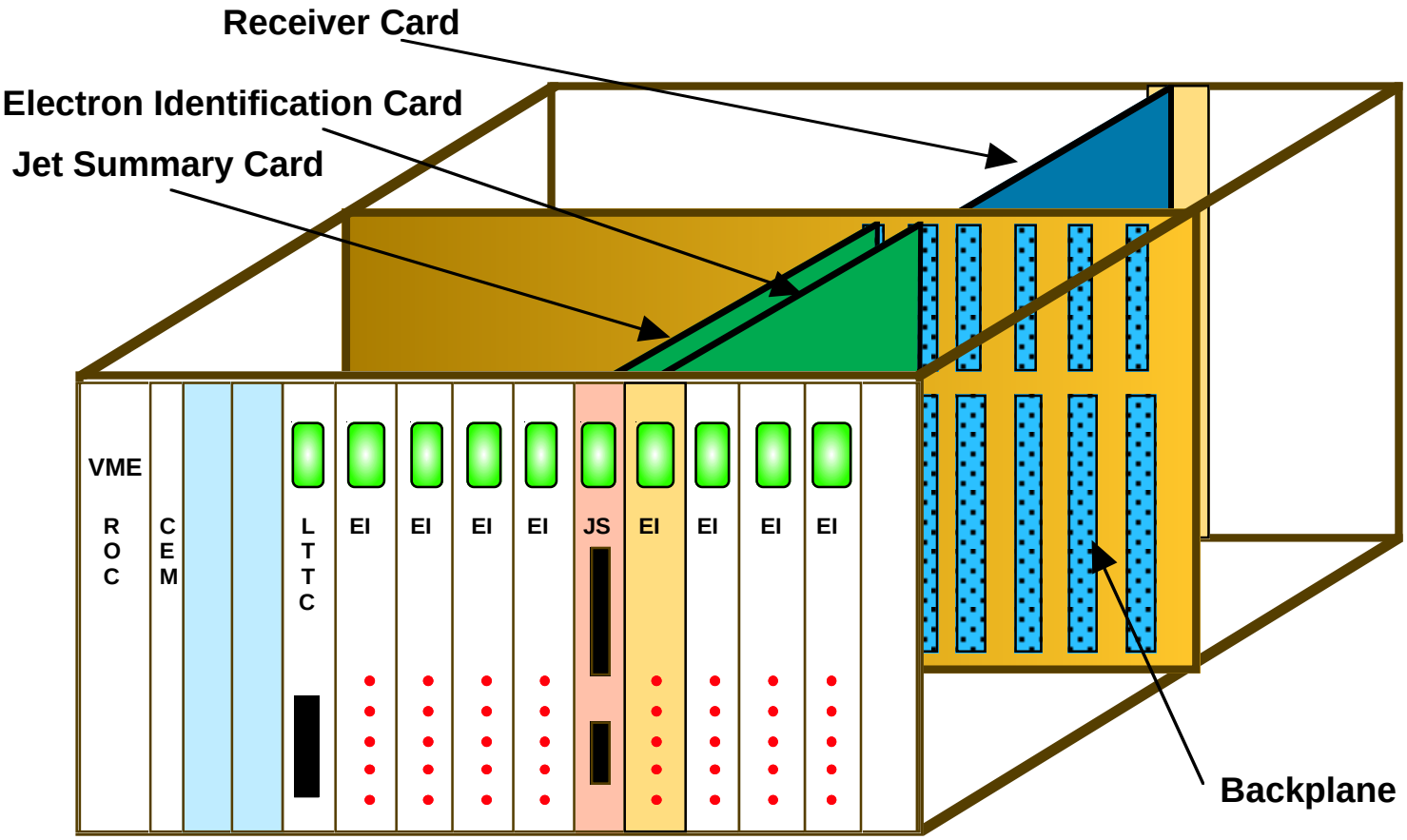
Use multijet triggers

Jet candidates are sorted to find highest energy jets

Calorimeter Trigger Overview



Regional Calorimeter Crate



Data from calorimeter FE on Cu links @ 1.2 Gbaud

- Into rear-mounted Receiver Cards **(proto. being built)**

160 MHz point to point backplane (built!)

- Clock&Control **(built!)** , Electron Identification, Jet/Summary, Receiver Cards operate @ 160 MHz

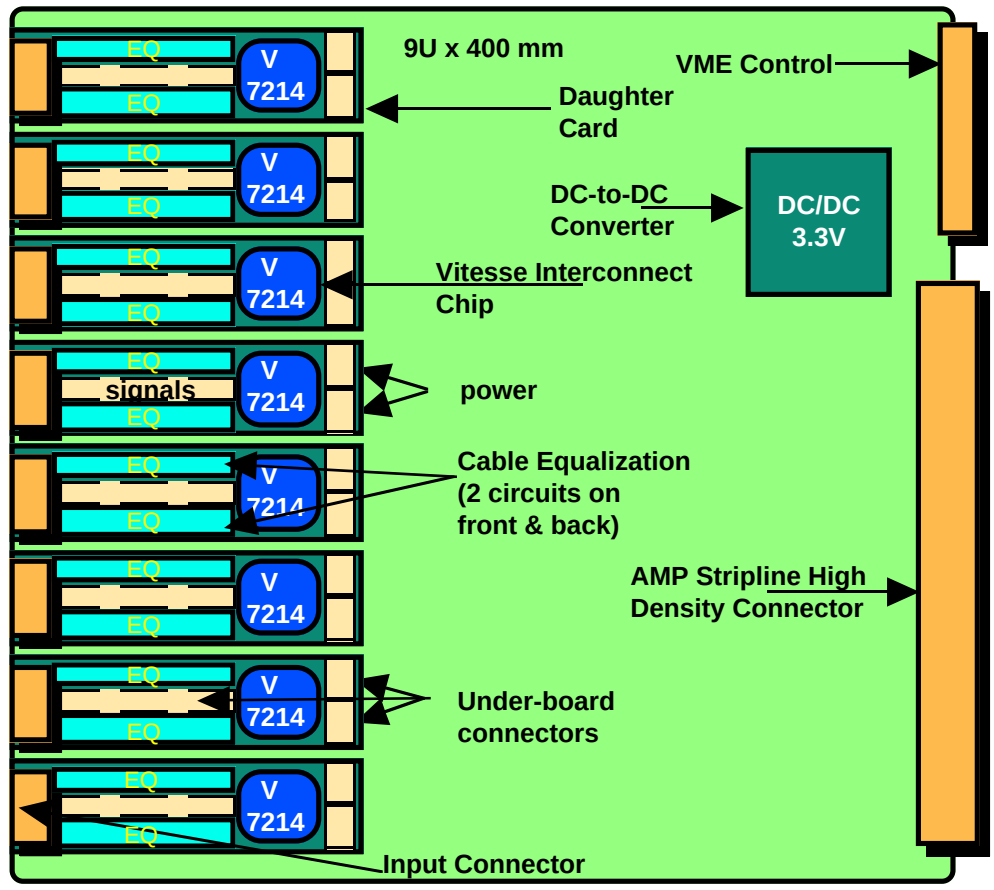
Output to calorimeter global trigger

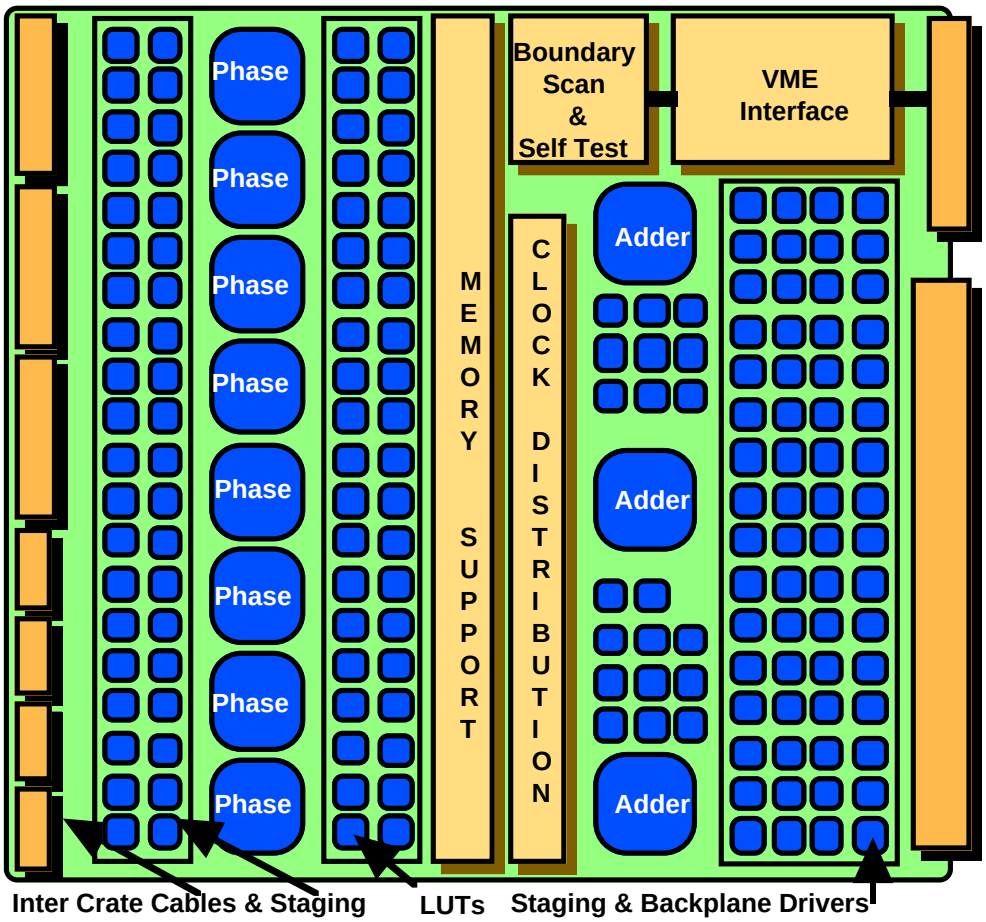
- From Jet Summary Card

Min Ion and Quiet bits to muon trigger

Receiver Card

(prototype being built by U. Wisconsin)





Rear:

32 Channels = 4 Ch. x 8 daughter cards

1.2 GBaud copper rcvrs

18 bit (2x9) data + 5 bit error det. codes

Vitesse Chip Converts Serial to Parallel

Front:

Data from Rear @ 120 MHz TTL

Phase ASIC: Deskew, EDC, Mux @ 160MHz ECL, Test vectors

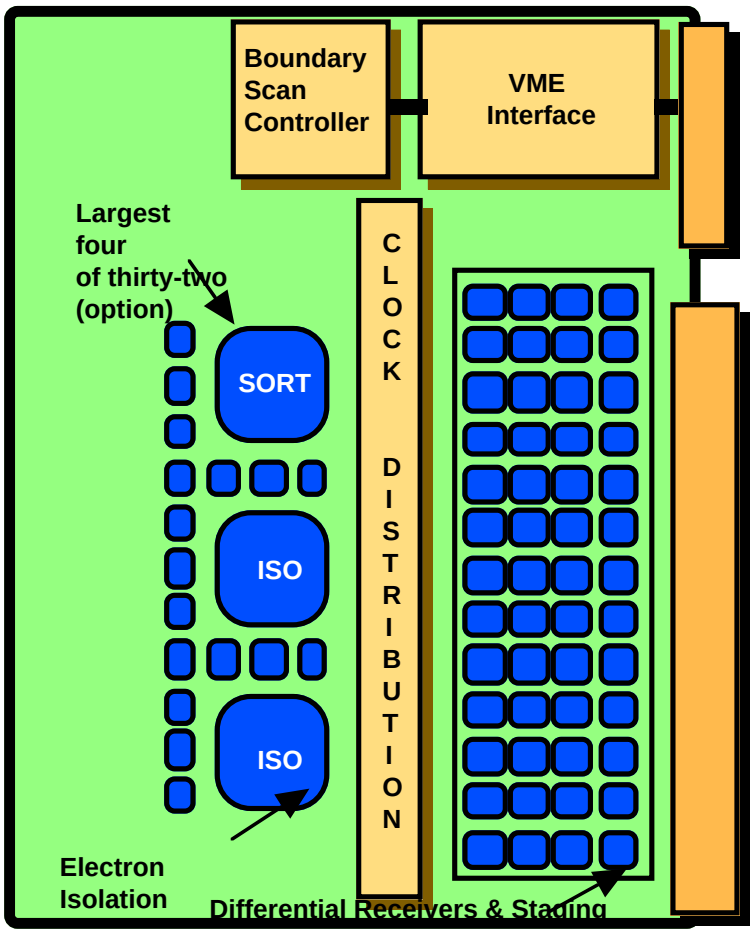
Error bit for each 4x4

Memory LUT @ 160 MHz

Adder ASIC: 8 inputs @ 160 MHz in 25 ns. (built!)

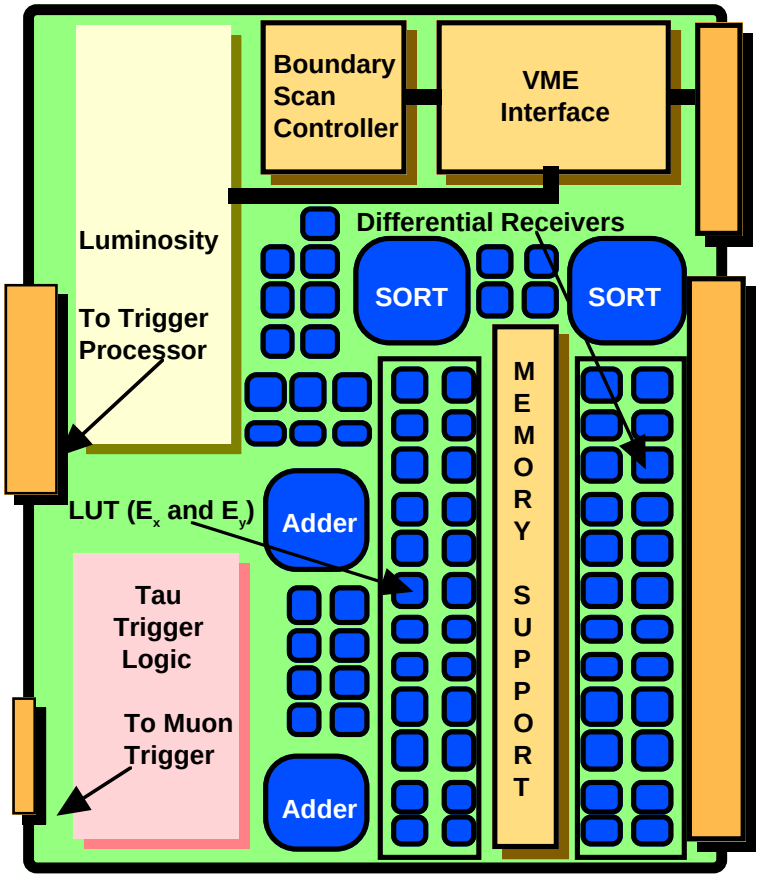
Differential Out@160 MHz

Electron ID & Jet/Summary Cards
(U. Wisconsin)



Electron Identification:

- Processes 4x8 region @ 160 MHz
- Electron isolation on ASIC
- Lookup tables for ranking
- Sort highest 4 rank candidates (option to take max)

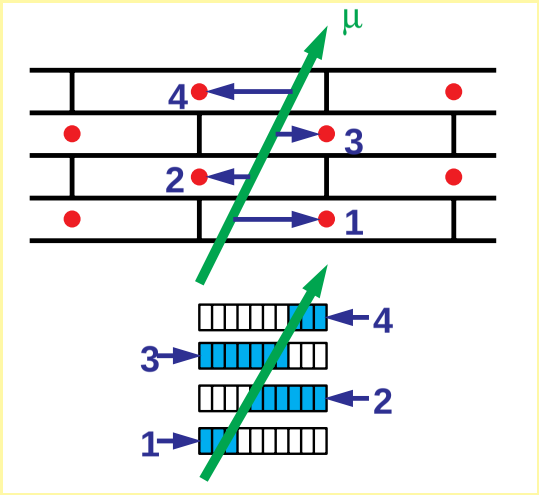


Jet/Summary:

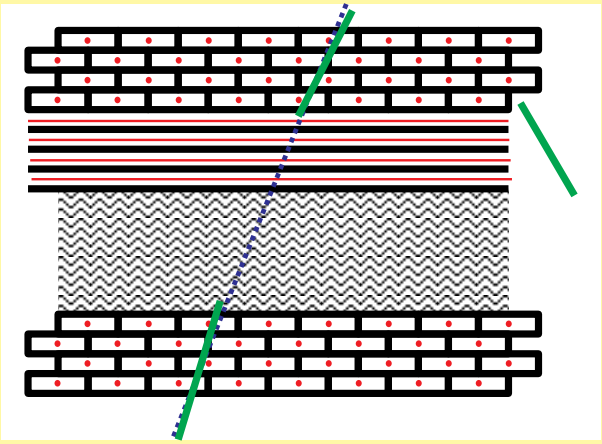
- Summarizes full crate:
- Sorts 32 electrons for top 4
- Sorts 32 4x4 E_t sums for top 4 jets
- LUTs generate E_x & E_y from E_t for 4x4 region
- Adder tree for crate E_t, E_x and E_y sums
- Quiet/MinI bits for each 4x4 region
- Reserved space for Tau & Lumi
- 40 MHz output to global and muon systems

Muon Chamber Trigger Logic

Drift Tubes

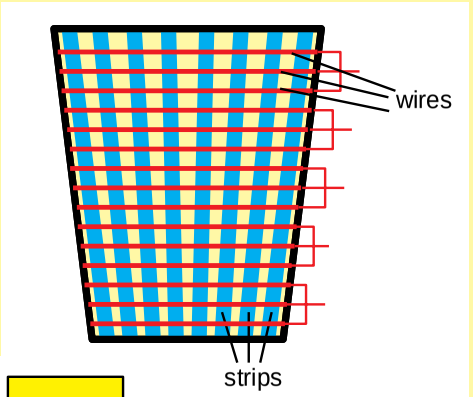


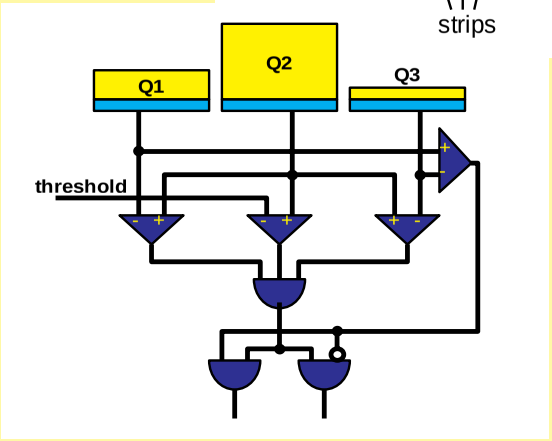
Meantimers recognize tracks and form vector / quartet.



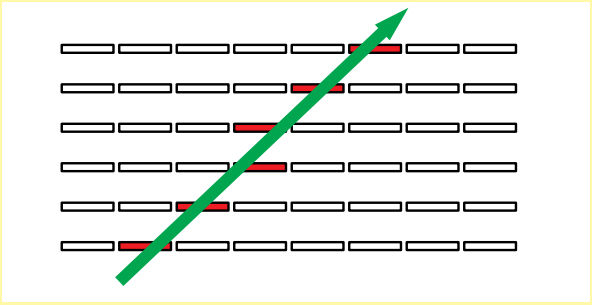
Correlator combines them into one vector / station.

CSC



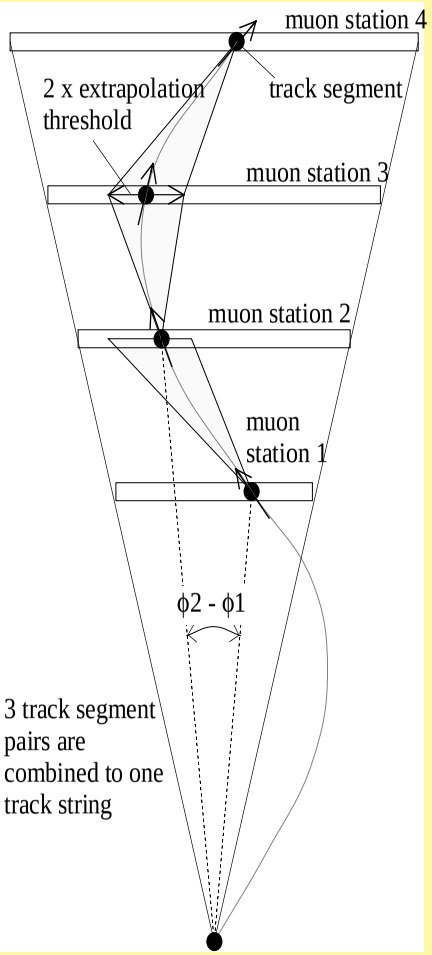


Comparators give 1/2-strip resol.



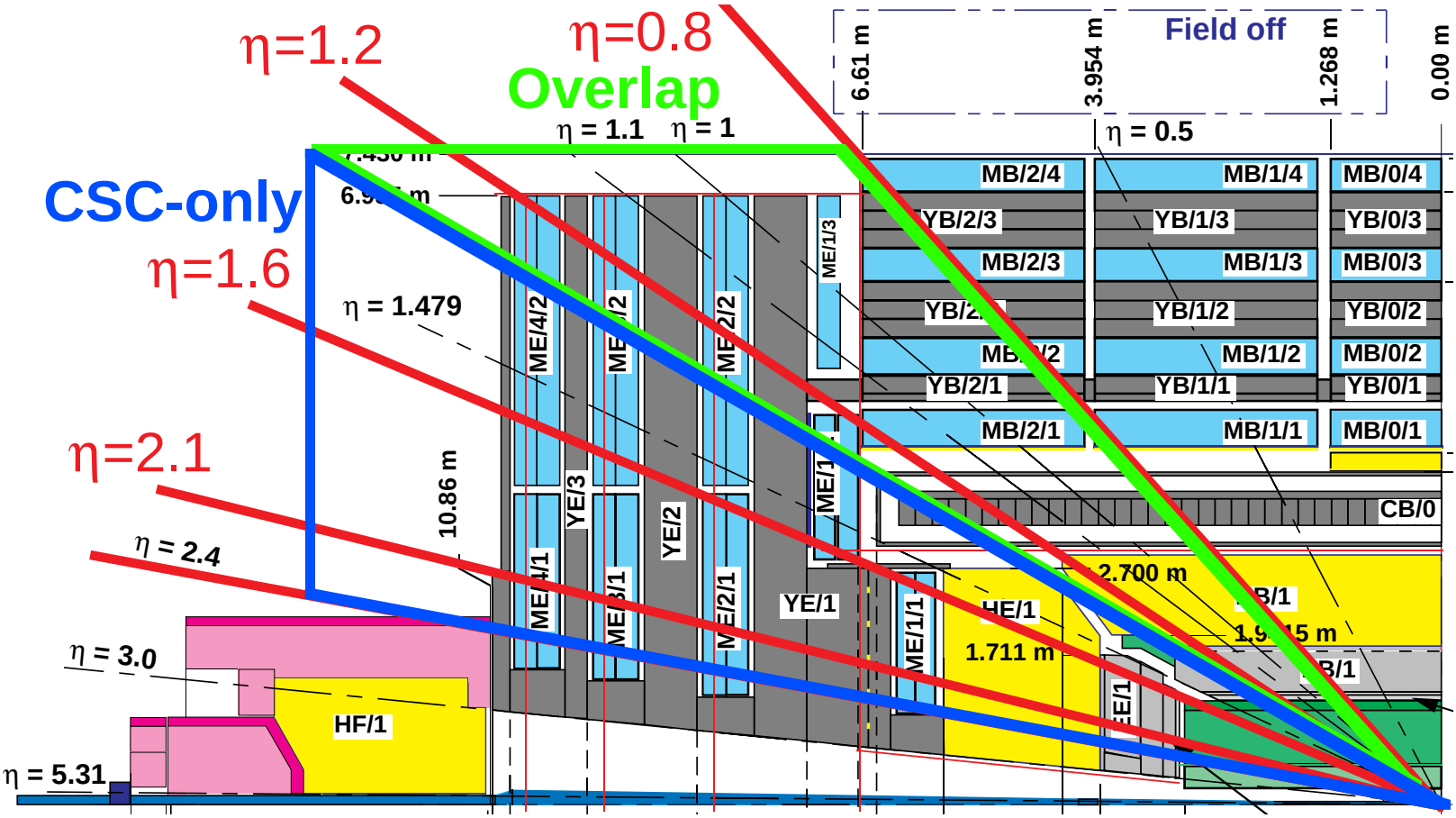
Hit strips of 6 layers form a vector.

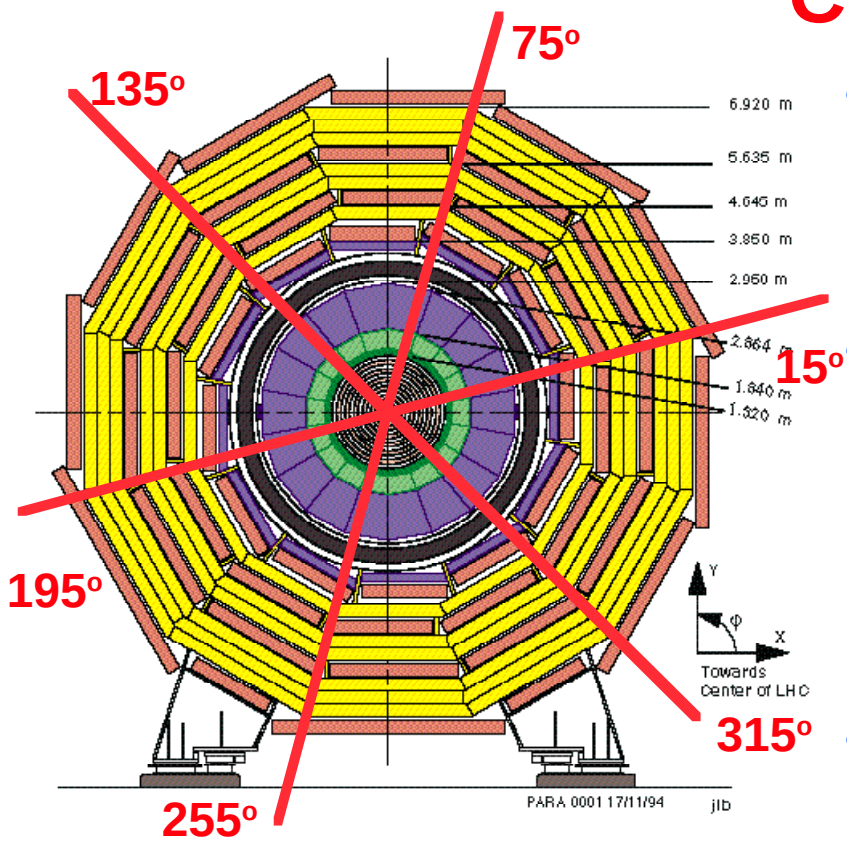
Track Finder



- combines vectors,
- forms a track,
- assigns p_t value.

CSC Muon Trigger Geometry

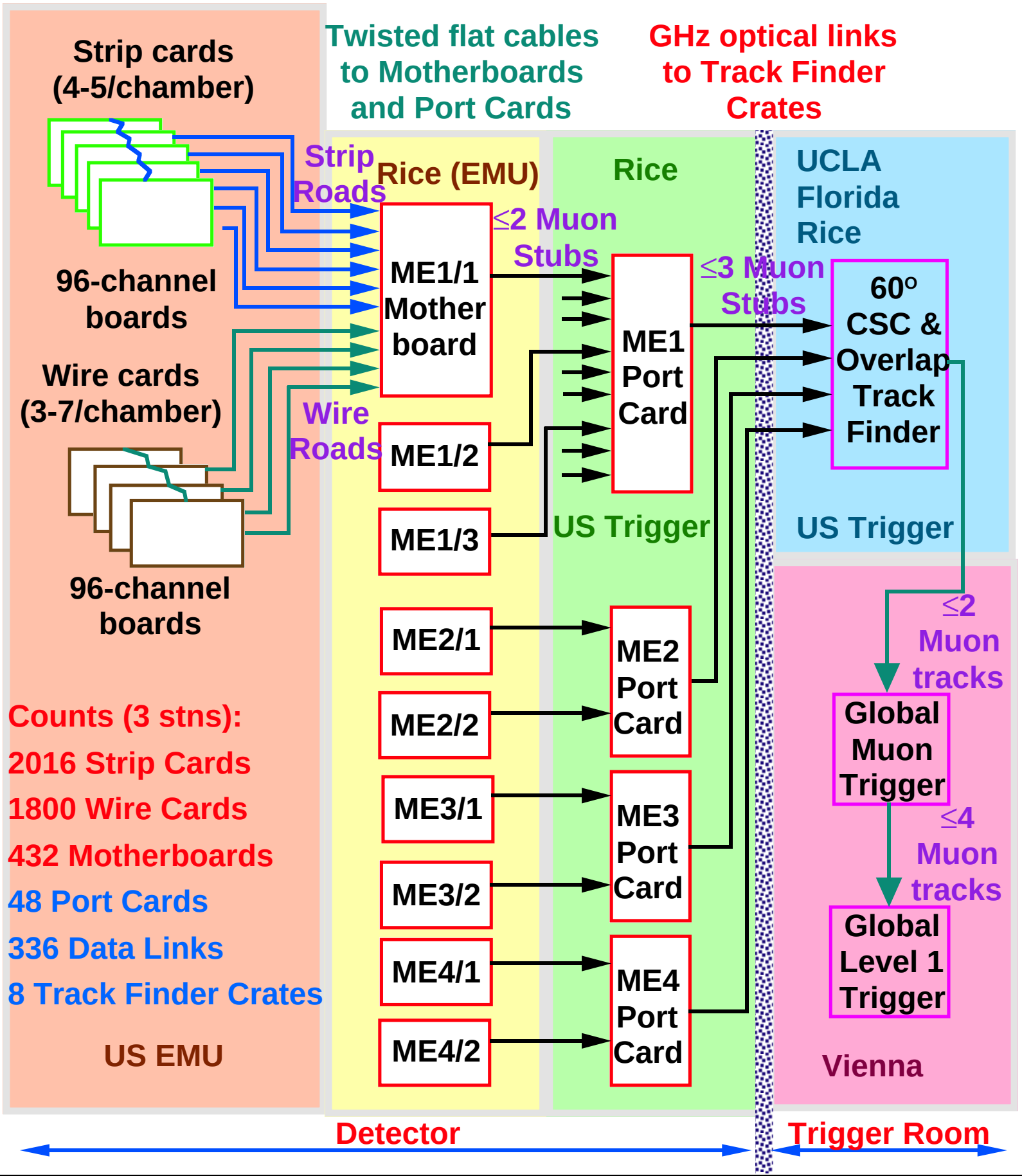




CSC Track-finding:

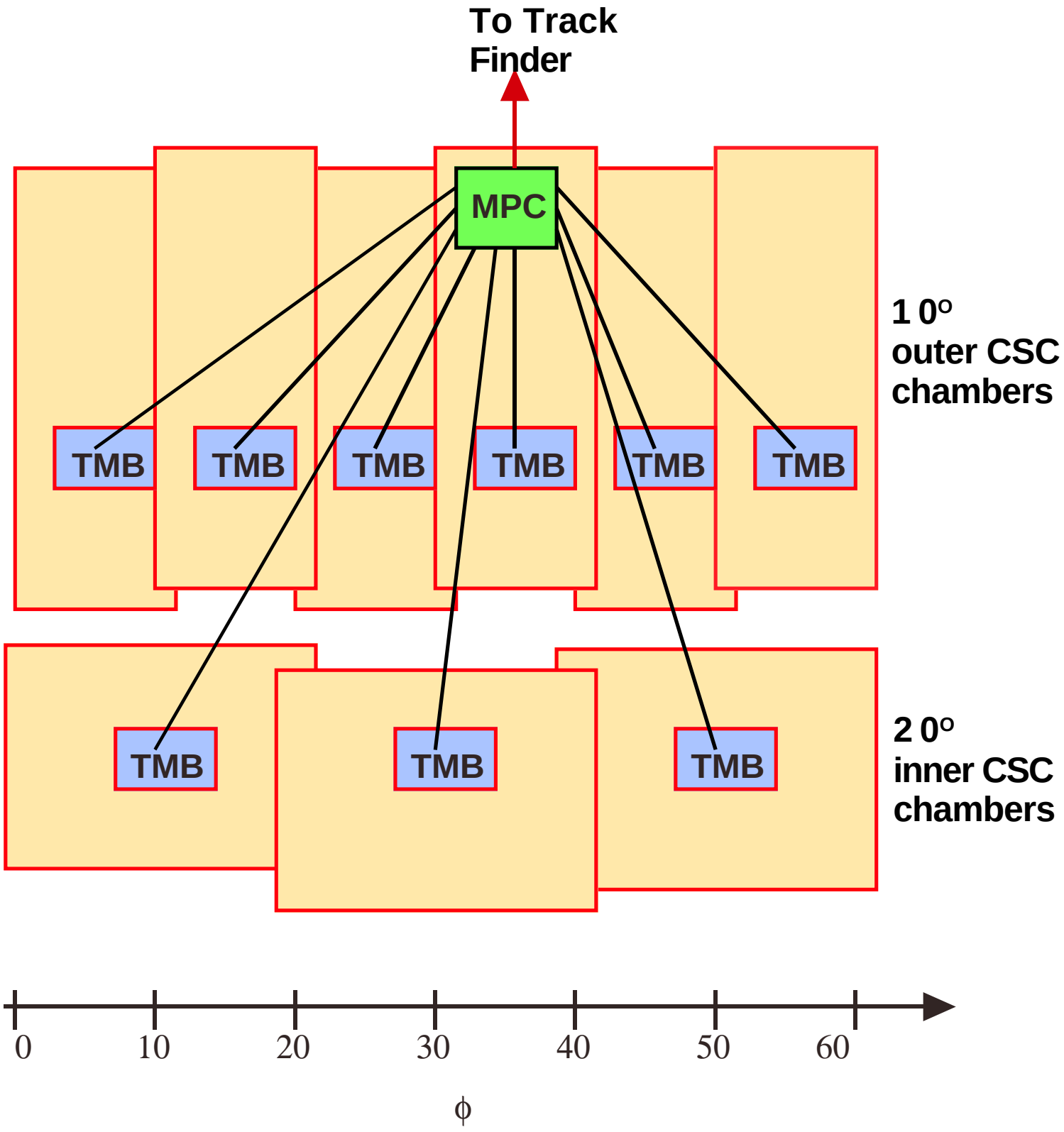
- **Two Types of Crates:**
  - 4 Overlap Crates
  - 4 CSC-only Crates
- **Two Sector Processors**
  - SP-Overlap
    - CSC's & Barrel DT's
  - SP-CSC
    - CSC's only
- **One Receiver Card:**
  - Either DT's or CSC's

CSC Trigger Layout

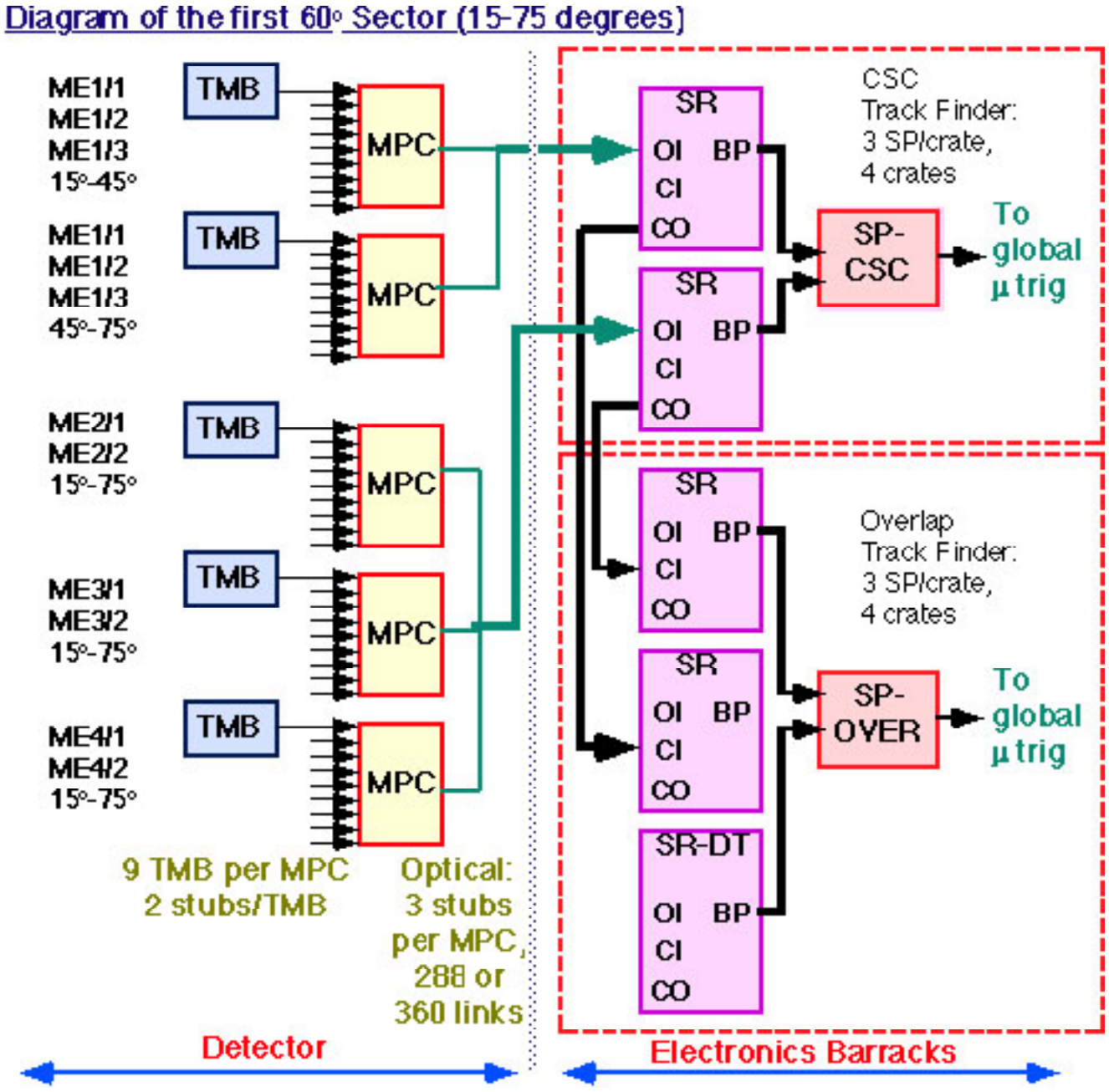


CSC Trigger Port Cards

TMB = Trigger MotherBoard
MPC = Port Card



CSC & Overlap TF Block Diagram



Glossary and Part Count

TMB: Trigger Motherboards (432 or 540)
MPC: Muon Port Cards (48 or 60)
SR: Sector Receivers for CSC (24)
SR-DT: Sector Receivers for DT (12 or 24)
SP-CSC: Sector Processors for CSC region (12)
SP-Over: Sector Processors for Overlap region (12)
OI, CI, CO, BP: Optical in, copper in, copper out, backplane

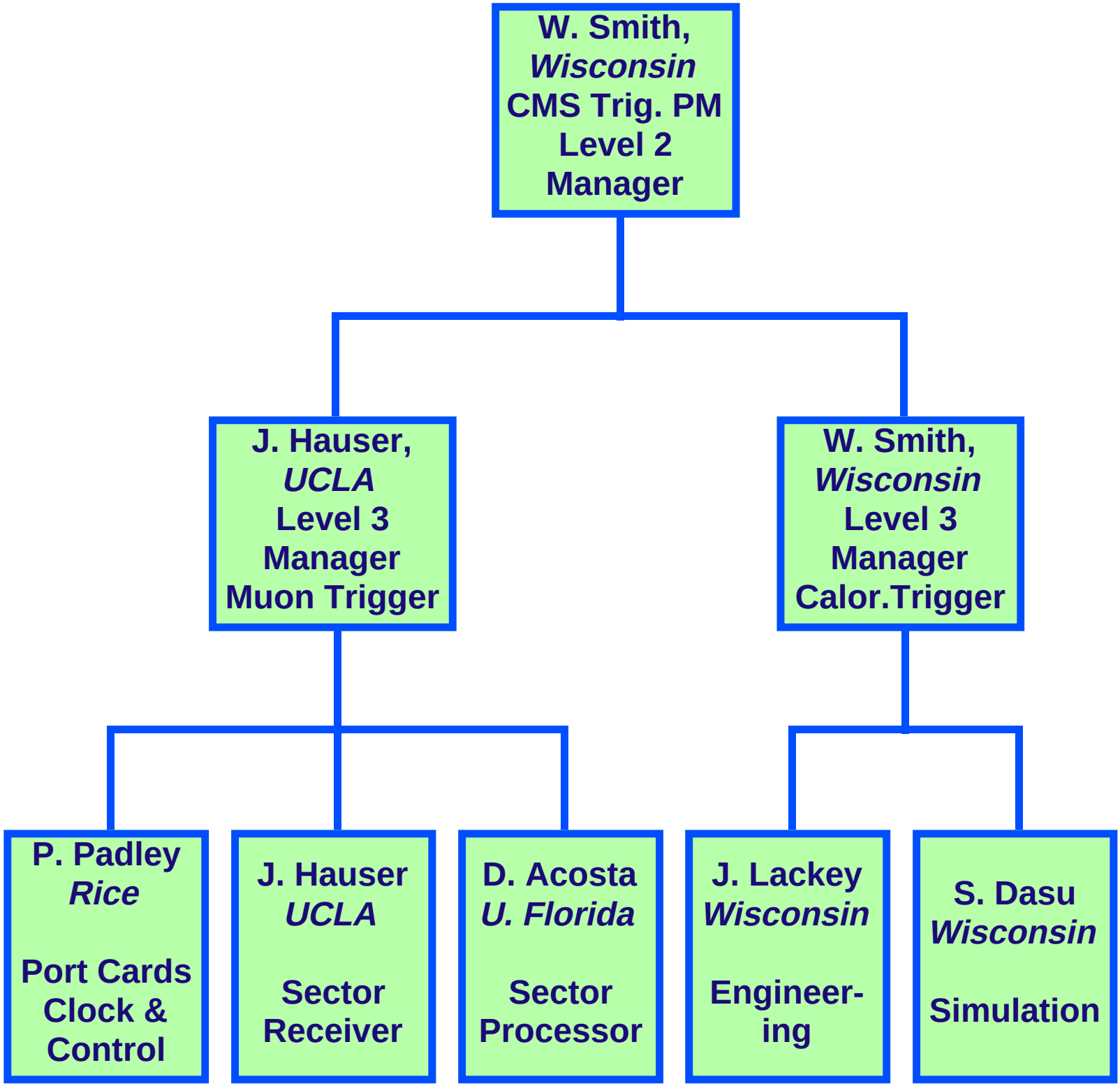
Muon & Cal. Trigger Rates

High Luminosity: $L = 10^{34}$ cm^{-2} s^{-1}

trigger type	threshold [GeV]	rate [kHz]	cumulative rate [kHz]
μ	20	7.8	7.8
$\mu\,\mu$	4	1.6	9.2
μ e	4, 8	5.5	14.4
μ j	4, 40	0.3	14.4
μ E_t^{miss}	4, 60	1.0	15.3
μ ΣE_t	4, 250	0.2	15.3
μ	7	9.8	9.5
$\mu\,\mu$	2-4	0.5	10.1
μ e	2-4, 6	2.5	12.2
μ e_b	2-4, 5	3.5	13.4
μ j	2-4, 12	2.2	14.5
μ E_t^{miss}	2-4, 40	0.8	14.7
μ ΣE_t	2-4, 150	0.8	14.7

Low Luminosity: $L = 10^{33}$ cm^{-2} s^{-1}

U.S.Trigger Organization



Cal. Trig. Milestones

Prototype Design Finished	May '99
Proto. test w/ECAL Proto. Elect.	Jun '99
Proto. Boards & Tests Finished	Nov '99
Begin ASIC Preproduction	May '00
Proto. test w/HCAL Proto. Elect.	Jun '00
Begin Backplane & Crate Production	May '01
ASIC Development Complete	Jun '01
Finish ASIC Preproduction	Oct '01
Begin Trigger Board Production	Mar '02
Begin Tests w/Final ECAL Elect.	Jul '02
Begin ASIC Production	Aug '02
Begin Tests w/Final HCAL Elect.	Sep '02
Crate & Backplane Complete	Sep '02
Begin Production Board Tests	Jan '03
Designs Finished	May '03
Finish ASIC Production	Nov '03
Finish Trigger Board Production	Feb '04
Finish Production Board Tests	Apr '04
Begin Trigger Installation	Apr '04
Begin Final System tests w/E,HCAL	May '04
Trigger Installation Finished	Sep '04

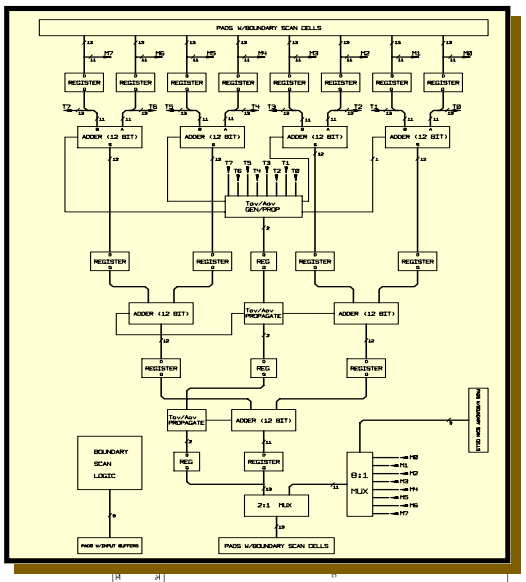
Muon Trig. Milestones

Finish Initial System Design	May '98
Begin Prototype Design	Oct '98
Begin Prototype Construction	Apr '99
Finish Prototype Design	May '99
Finish Prototype Construction	Oct '99
Begin Final Design	Jun '00
Begin Prototype Test w/Chamb FE	Aug '00
Finish Prototype Test w/Chamb FE	Jul '01
Begin Production	Jan '02
Finish Final Design	Jul '02
Final Electronics Sector Test	Oct '02
Finish Production	Nov '03
Begin Installation	Aug '03
Finish Installation	Apr '04
Begin Trigger System Tests	Apr '04
Finish Trigger System Tests	Sep '04

Calorimeter Trigger Status

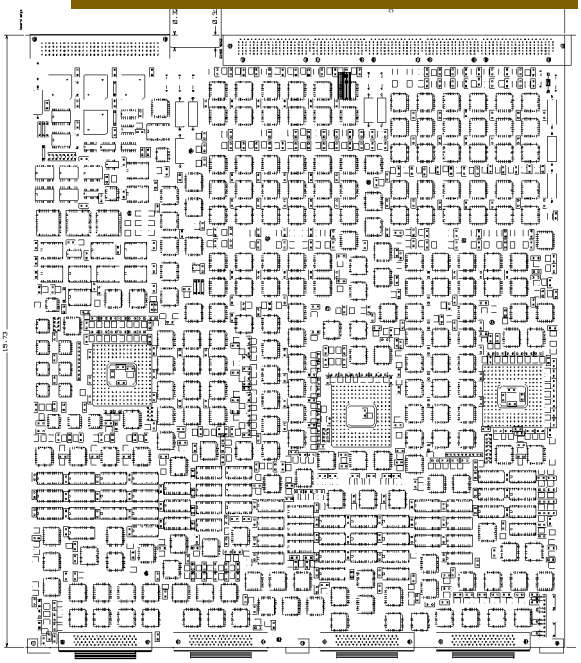
13 x 8 bit Adder ASIC

- tested > 160 MHz



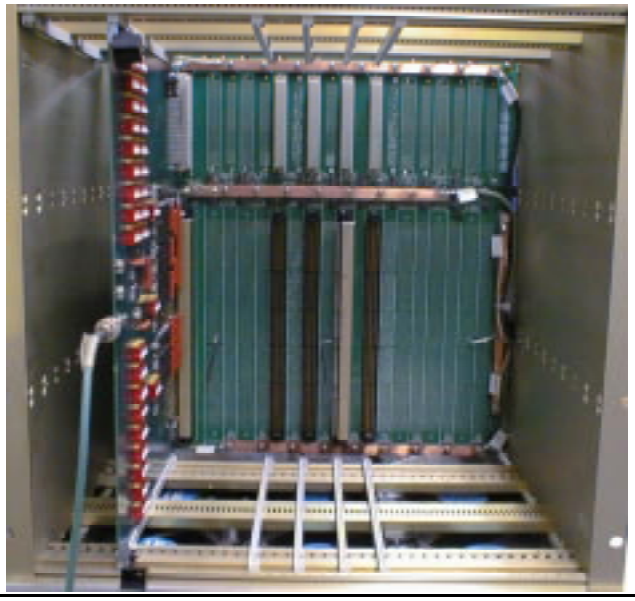
Receiver Card

- Designed for 160 MHz
- Being built



Backplane for VME & trigger data

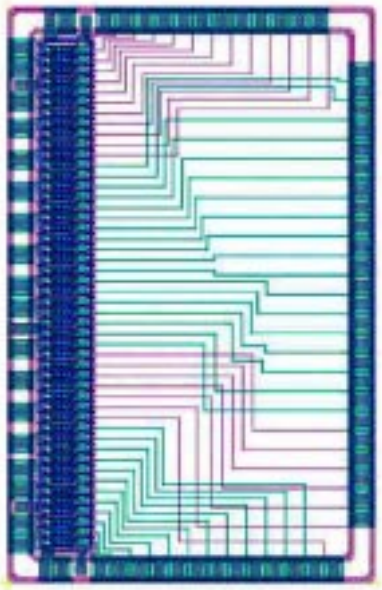
- Prototype constructed
- Prototype Clock & Control Card built
- Signal performance excellent @ 160 MHz
- Confirmation of design feasibility



Muon Trigger Status

16-ch Comparator ASICs ready

- Excellent performance (1mV offsets)
- Comparator board routed, sent to be manufactured

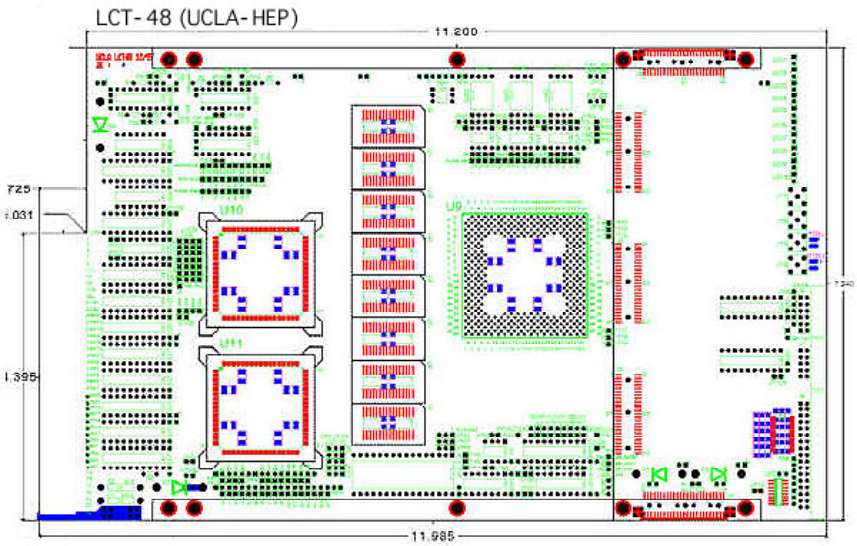


First Cathode LCT card built

- Software being debugged

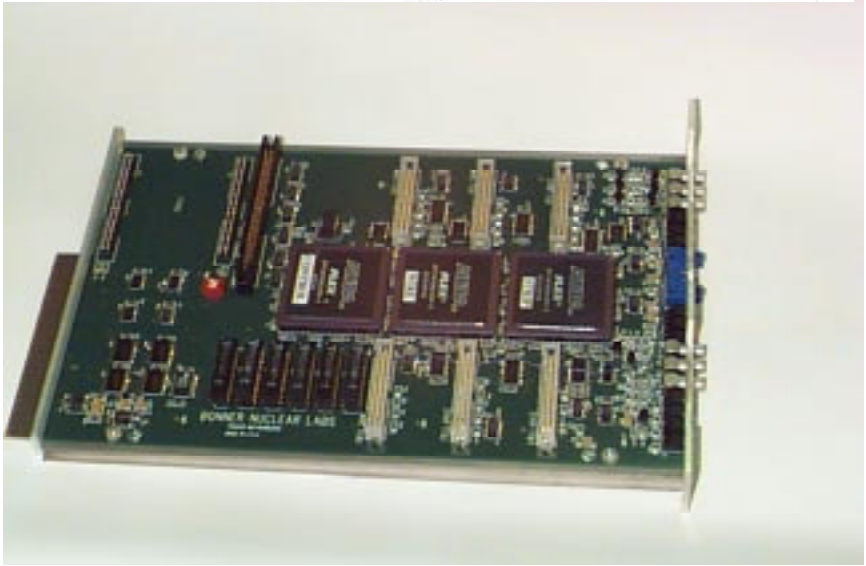
First Anode LCT card built...

- But not stuffed (1 week)
- Software being developed



First Trigger Motherboard built

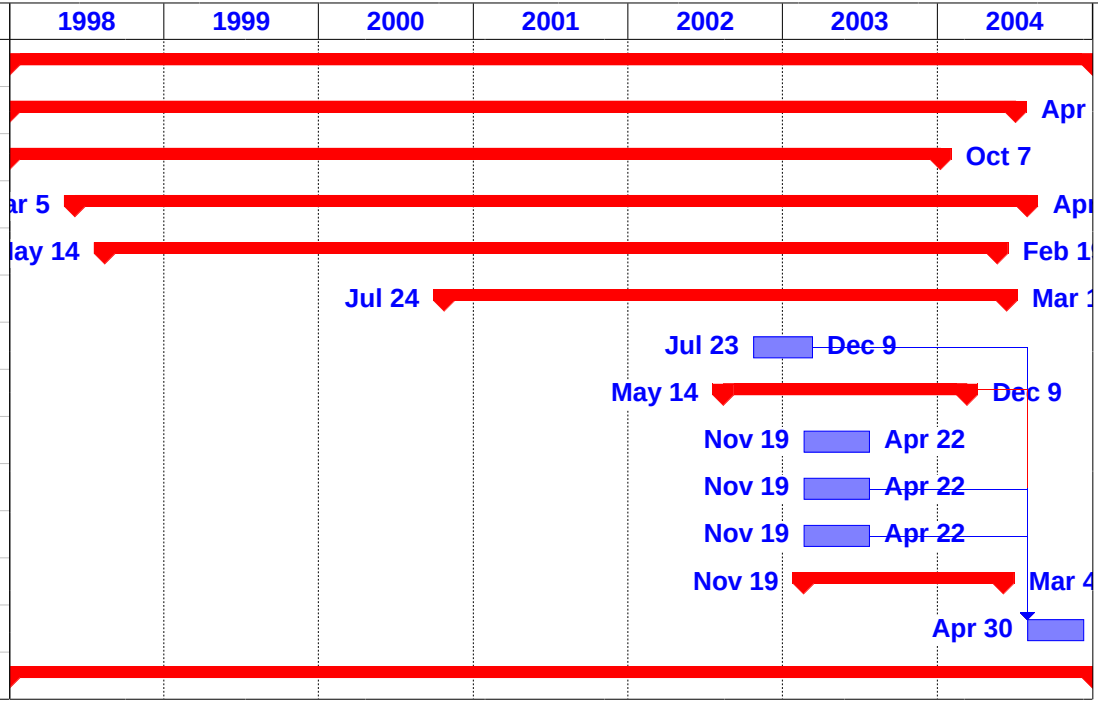
- Ready for test w/LCT cards



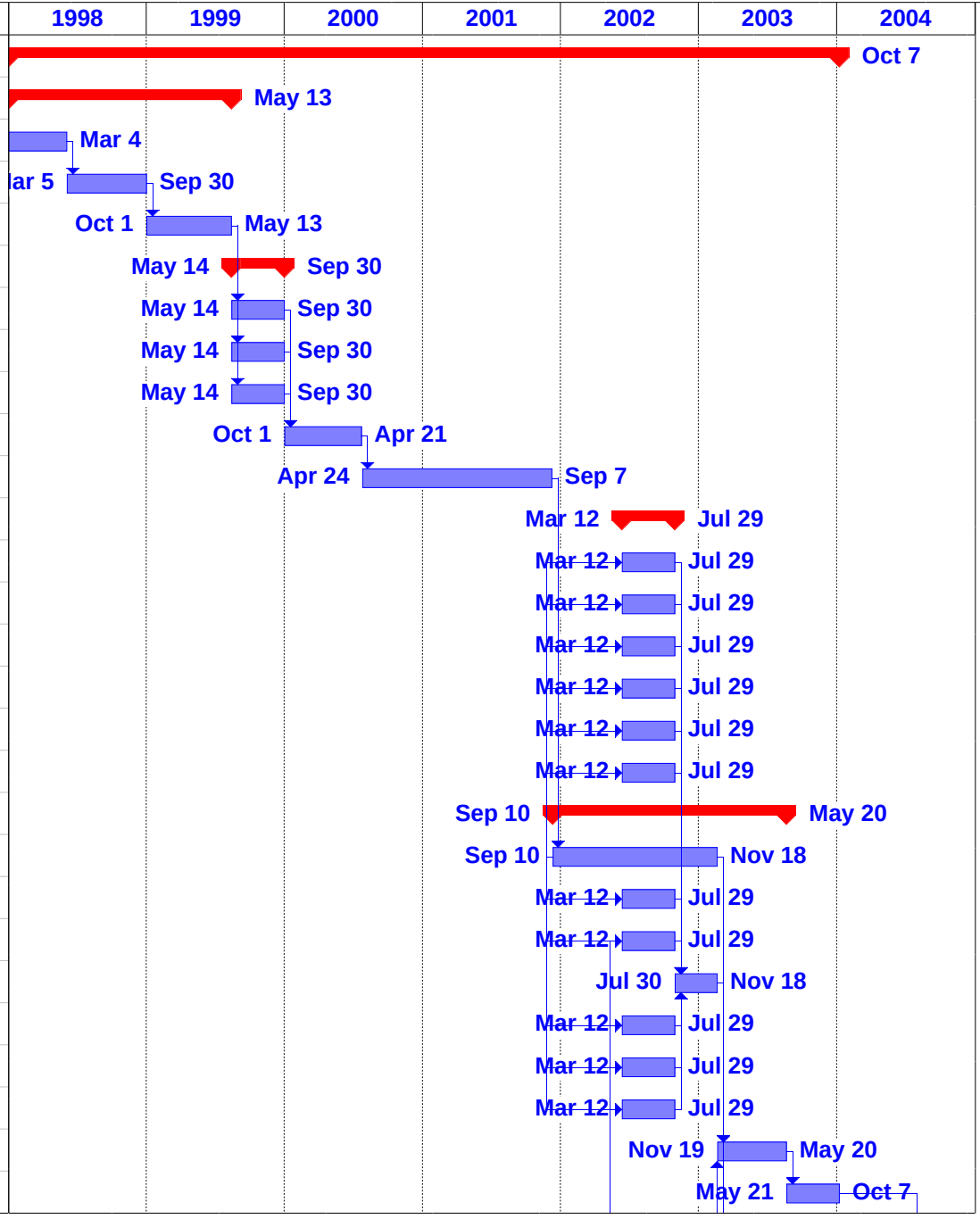
Operation in Summer '98 test beam

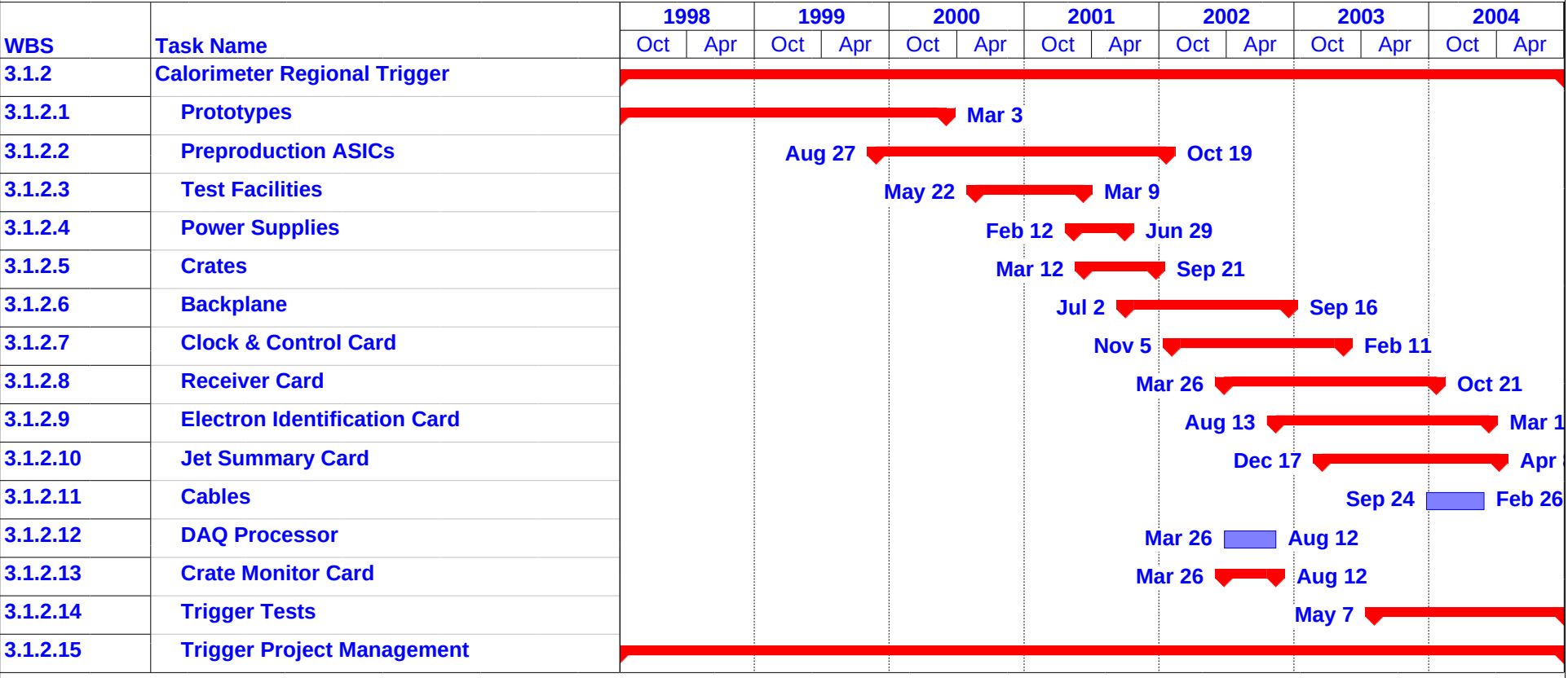
WBS Number	Description	Mfg M&S (k$)	EDIA (k$)	Base Cost (k$)	Cont (k$)	Cont (%)	Total Cost (k$)	DOE Request (k$)
3	**Trigger and Data Acquisition**	**7,461**	**3,454**	**10,915**	**5,711**	**52**	**16,626**	**15,663**
3.1	***Trigger***	***3,953***	***2,185***	***6,137***	***3,128***	***51***	***9,265***	***9,265***
3.1.1	CSC Muon Trigger	812	937	1,749	885	51	2,634	2,634
3.1.1.1	Muon Port Cards (MPC)	292	215	507	253	50	760	760
3.1.1.2	Sector Receivers (SR)	208	202	410	205	50	615	615
3.1.1.3	CSC Sector Processors (SP-CSC)	76	170	246	160	65	406	406
3.1.1.4	Overlap Sector Processors (SP-OVR)	76	170	246	160	65	406	406
3.1.1.5	Clock&Control Cards (CCC)	36	78	114	34	30	148	148
3.1.1.6	Crate Monitor Cards	10		10	3	30	13	13
3.1.1.7	Muon Backplanes	20	60	80	34	43	114	114
3.1.1.8	Crate Controllers	35		35	11	30	46	46
3.1.1.9	Muon Crates	6		6	1	10	7	7
3.1.1.10	Muon Power Supplies	23		23	2	10	25	25
3.1.1.11	Additional Cables	30		30			30	30
3.1.1.12	Trigger System Tests		43	43	21	50	64	64
3.1.1.13	Trigger Project Management							
3.1.2	Calorimeter Regional Trigger	3,141	1,247	4,388	2,244	51	6,631	6,631
3.1.2.1	Prototypes	140	301	441	193	44	635	635
3.1.2.2	Preproduction ASICs	310	243	553	258	47	811	811
3.1.2.3	Test Facilities	60	18	78	39	50	117	117
3.1.2.4	Power Supplies	79	3	82	8	10	90	90
3.1.2.5	Crates	13	21	35	3	10	38	38
3.1.2.6	Backplane	130	64	194	83	43	277	277
3.1.2.7	Clock & Control Card	65	67	132	40	30	172	172
3.1.2.8	Receiver Card	1,561	109	1,670	1,019	61	2,688	2,688
3.1.2.9	Electron Identification Card	649	95	744	372	50	1,116	1,116
3.1.2.10	Jet Summary Card	103	67	170	85	50	254	254
3.1.2.11	Cables	7		7	2	30	9	9
3.1.2.12	DAQ Processor							
3.1.2.13	Crate Monitor Card							
3.1.2.14	Trigger Tests	22	260	282	141	50	423	423
3.1.2.15	Trigger Project Management							

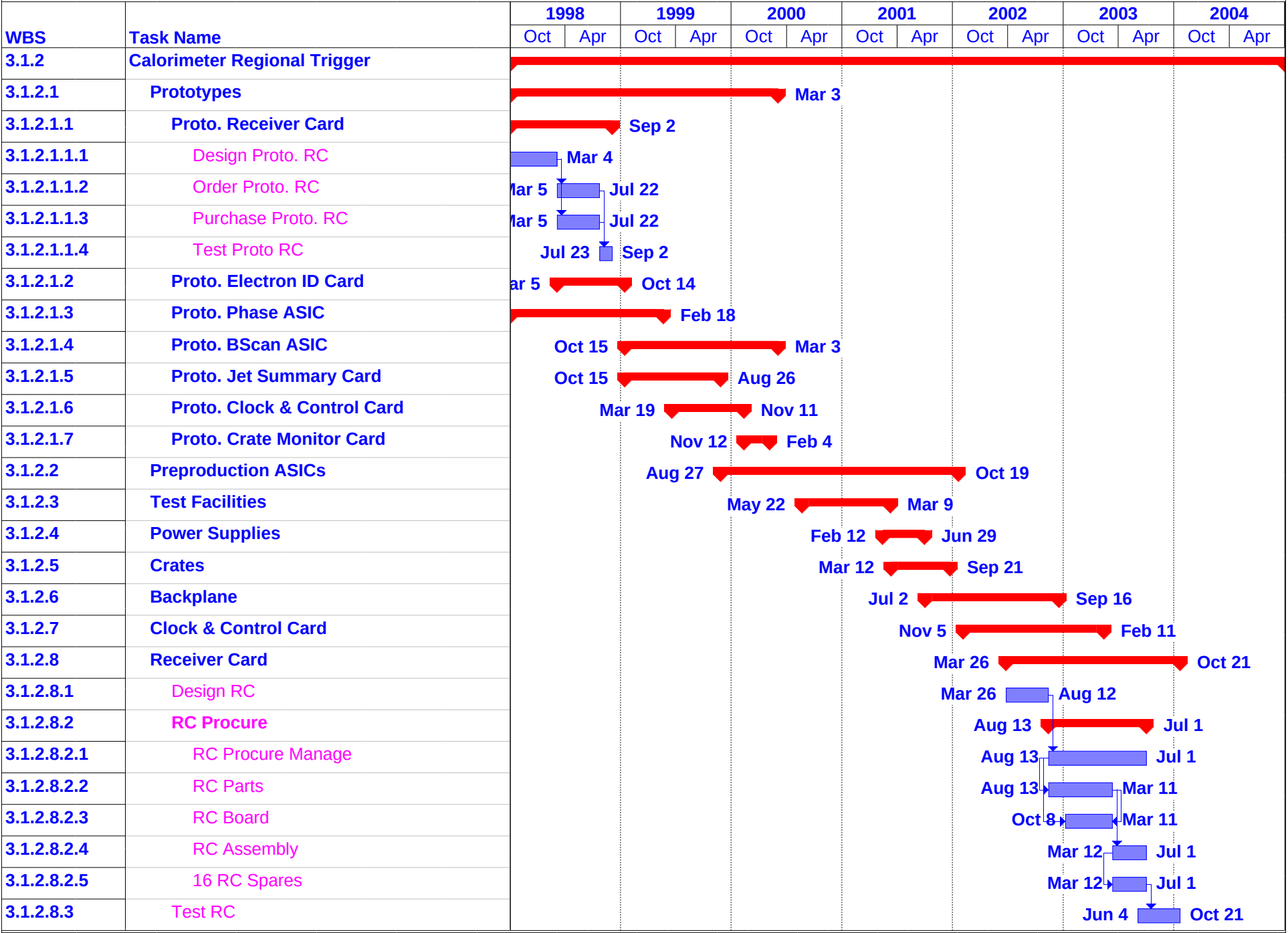
WBS	Task Name
3.1.1	CSC Muon Trigger
3.1.1.1	Muon Port Cards (MPC)
3.1.1.2	Sector Receivers (SR)
3.1.1.3	CSC Sector Processors (SP-CSC)
3.1.1.4	Overlap Sector Processors (SP-OVR)
3.1.1.5	Clock&Control Cards (CCC)
3.1.1.6	Crate Monitor Cards
3.1.1.7	Muon Backplanes
3.1.1.8	Crate Controllers
3.1.1.9	Muon Crates
3.1.1.10	Muon Power Supplies
3.1.1.11	Additional Cables
3.1.1.12	Trigger System Tests
3.1.1.13	Trigger Project Management



WBS	Task Name
3.1.1.2	**Sector Receivers (SR)**
3.1.1.2.1	**SR Design**
3.1.1.2.1.1	SR Initial System Design
3.1.1.2.1.2	SR Initial Proto. Design
3.1.1.2.1.3	SR Proto. Design
3.1.1.2.2	**SR Proto. Construction**
3.1.1.2.2.1	SR Proto. Constr. Manage
3.1.1.2.2.2	SR Proto. Components
3.1.1.2.2.3	SR Proto. Boards
3.1.1.2.3	**SR Proto. Test**
3.1.1.2.4	**SR ASIC and Board Design**
3.1.1.2.5	**SR Active Components**
3.1.1.2.5.1	SR FPGA's
3.1.1.2.5.2	SR Glink Receivers
3.1.1.2.5.3	SR EPROMs
3.1.1.2.5.4	SR FIFOs for DAQ
3.1.1.2.5.5	SR Buffers
3.1.1.2.5.6	SR Memory Lookups
3.1.1.2.6	**SR Boards**
3.1.1.2.6.1	SR Const. Manage
3.1.1.2.6.2	SR Board Setup
3.1.1.2.6.3	SR Board Fabrication
3.1.1.2.6.4	SR Board Assembly
3.1.1.2.6.5	SR Connectors-copper
3.1.1.2.6.6	SR Misc components
3.1.1.2.6.7	SR Front Panels and Hardware
3.1.1.2.6.7	SR Inspection and test
3.1.1.2.7	**SR Installation**




WBS
Task Name
1998
1999
2000
2001
2002
2003
2004
Oct
Apr
3.1.2
Calorimeter Regional Trigger
3.1.2.1
Prototypes
Mar 3
3.1.2.2
Preproduction ASICs
Aug 27
Oct 19
3.1.2.3
Test Facilities
May 22
Mar 9
3.1.2.4
Power Supplies
Feb 12
Jun 29
3.1.2.5
Crates
Mar 12
Sep 21
3.1.2.6
Backplane
Jul 2
Sep 16
3.1.2.7
Clock & Control Card
Nov 5
Feb 11
3.1.2.8
Receiver Card
Mar 26
Oct 21
3.1.2.9
Electron Identification Card
Aug 13
Mar 1
3.1.2.10
Jet Summary Card
Dec 17
Apr
3.1.2.11
Cables
Sep 24
Feb 26
3.1.2.12
DAQ Processor
Mar 26
Aug 12
3.1.2.13
Crate Monitor Card
Mar 26
Aug 12
3.1.2.14
Trigger Tests
May 7
3.1.2.15
Trigger Project Management


1998
1999
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2002
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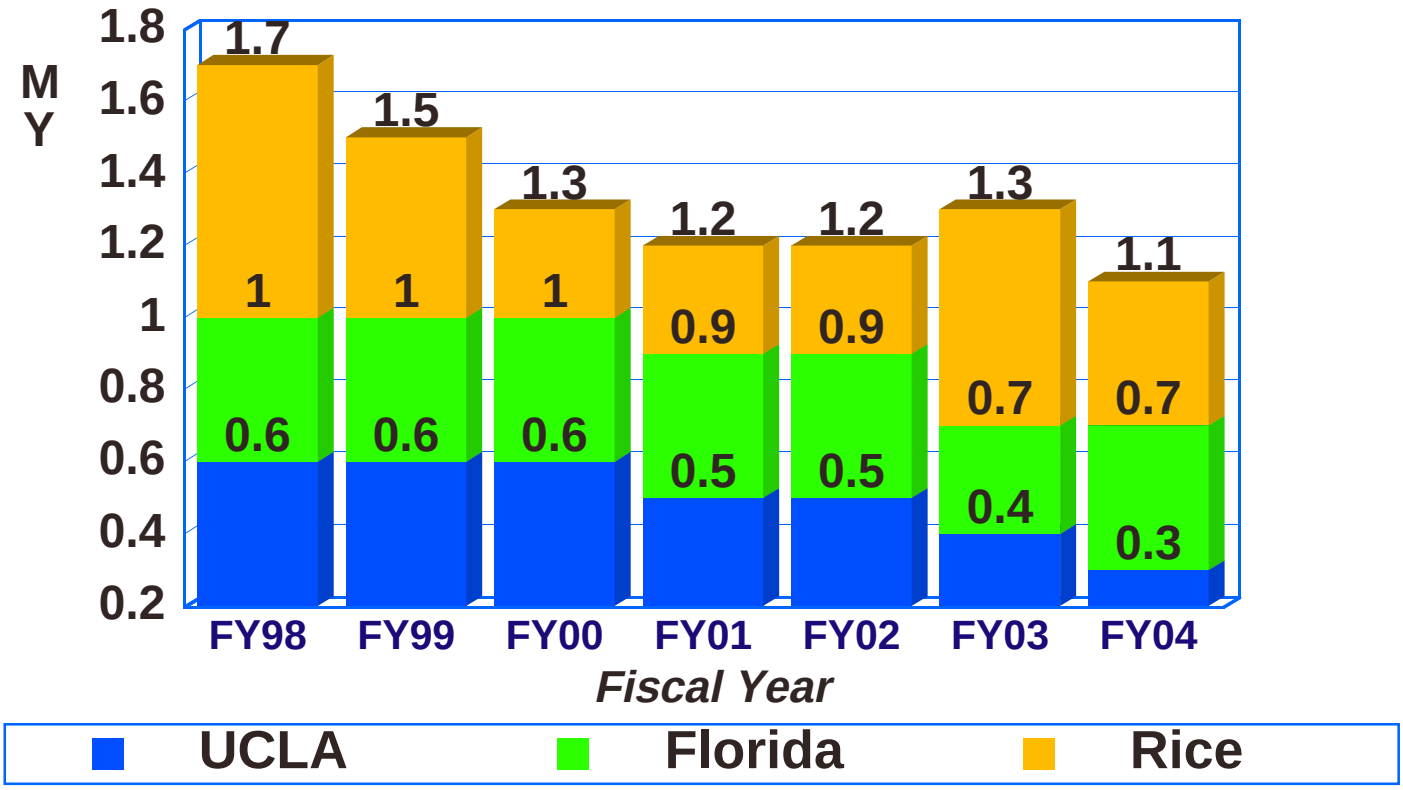
2004
Oct
Apr
WBS
Task Name
3.1.2 Calorimeter Regional Trigger
3.1.2.1 Prototypes
Mar 3
3.1.2.1.1 Proto. Receiver Card
Sep 2
3.1.2.1.1.1 Design Proto. RC
Mar 4
3.1.2.1.1.2 Order Proto. RC
Jul 22
3.1.2.1.1.3 Purchase Proto. RC
Jul 22
3.1.2.1.1.4 Test Proto RC
Jul 23
Sep 2
3.1.2.1.2 Proto. Electron ID Card
Oct 14
3.1.2.1.3 Proto. Phase ASIC
Feb 18
3.1.2.1.4 Proto. BScan ASIC
Oct 15
Mar 3
3.1.2.1.5 Proto. Jet Summary Card
Oct 15
Aug 26
3.1.2.1.6 Proto. Clock & Control Card
Mar 19
Nov 11
3.1.2.1.7 Proto. Crate Monitor Card
Nov 12
Feb 4
3.1.2.2 Preproduction ASICs
Aug 27
Oct 19
3.1.2.3 Test Facilities
May 22
Mar 9
3.1.2.4 Power Supplies
Feb 12
Jun 29
3.1.2.5 Crates
Mar 12
Sep 21
3.1.2.6 Backplane
Jul 2
Sep 16
3.1.2.7 Clock & Control Card
Nov 5
Feb 11
3.1.2.8 Receiver Card
Mar 26
Oct 21
3.1.2.8.1 Design RC
Mar 26
Aug 12
3.1.2.8.2 RC Procure
Aug 13
Jul 1
3.1.2.8.2.1 RC Procure Manage
Aug 13
Jul 1
3.1.2.8.2.2 RC Parts
Aug 13
Mar 11
3.1.2.8.2.3 RC Board
Oct 8
Mar 11
3.1.2.8.2.4 RC Assembly
Mar 12
Jul 1
3.1.2.8.2.5 16 RC Spares
Mar 12
Jul 1
3.1.2.8.3 Test RC
Jun 4
Oct 21

Peak Engineering Level

Muon Trigger

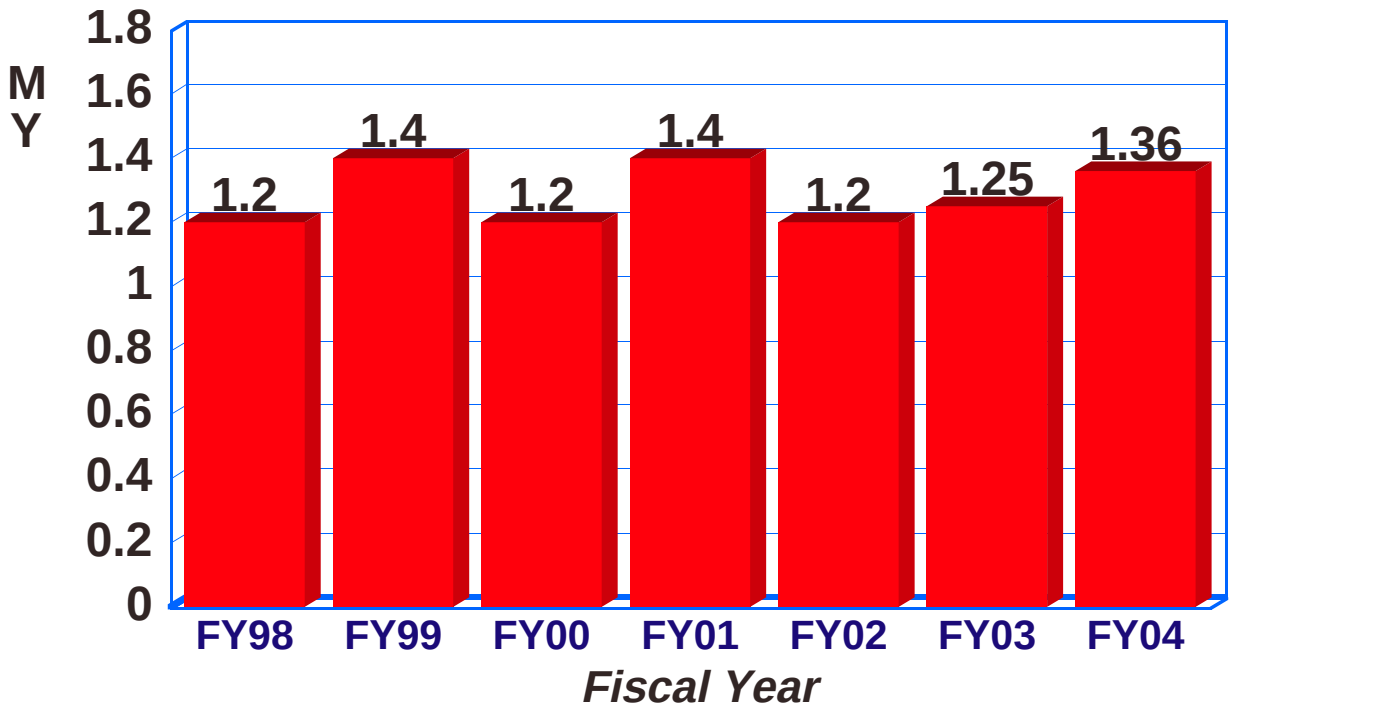
WBS 3.1.1



UCLA | Florida | Rice

Calorimeter Trigger

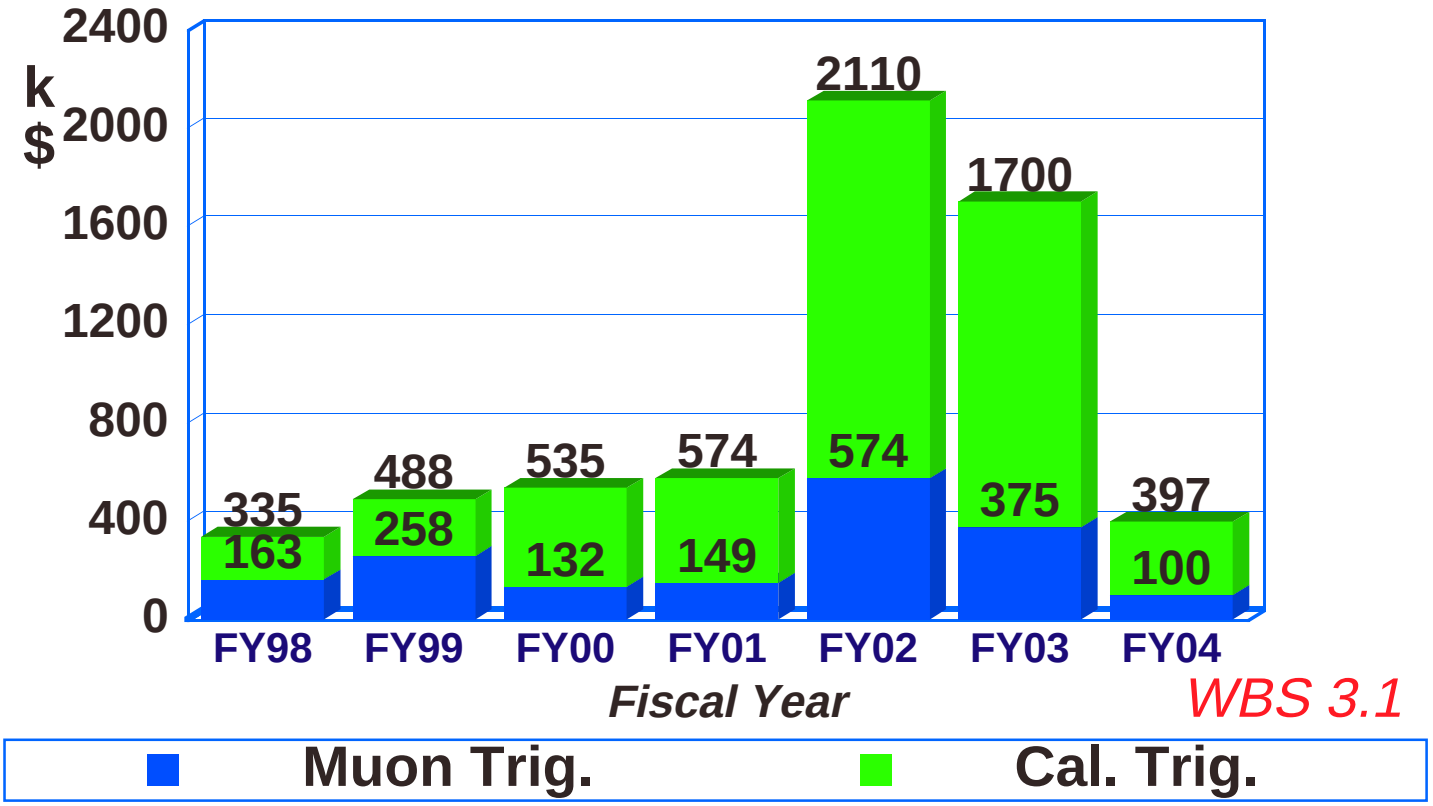
WBS 3.1.2



Wisconsin

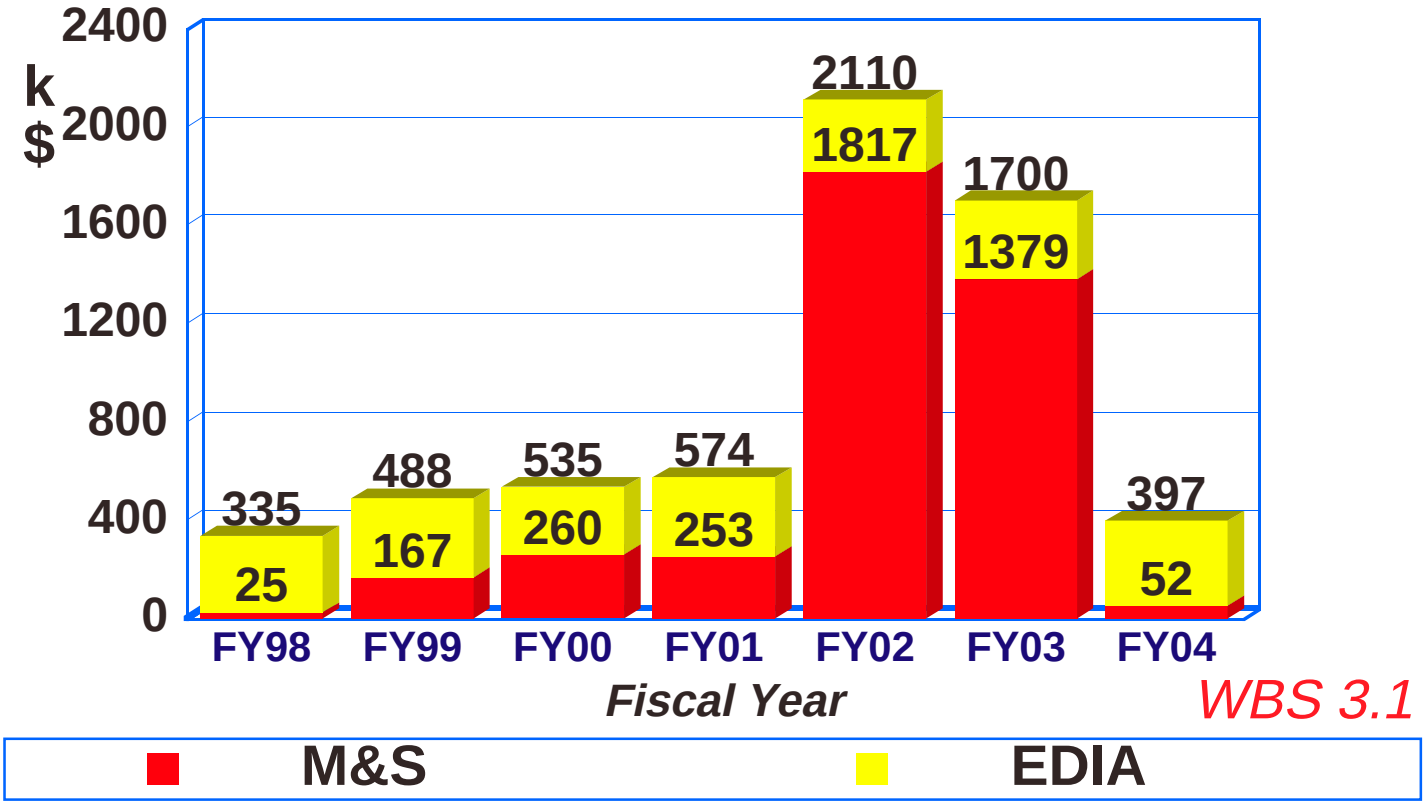
Obligations Profile

Obligations for Muon & Cal Triggers



WBS 3.1

Trigger M&S and EDIA Obligations



WBS 3.1

Concerns

Calorimeter Trigger

- **Processing Data at 160 MHz**
  - Built 160 MHz Adder ASIC
  - Built 160 MHz Backplane
  - Receiver Card being built
- **Input data on 1.2 Gbaud Cu links**
  - Receiver Card Test
    - Links on daughter cards
    - Card being built
- **Trigger performance**
  - Simulation studies
  - Safety factor of 3

Muon Trigger

- **Chamber/Trigger Performance**
  - Prototype test in Summer '98
- **Integration of DT/CSC's**
  - Design collaboration with Vienna
- **Algorithm finalization**
  - New Simulation effort (FPGA's are flexible)
- **FPGA vs. ASIC**
  - Rapidly changing market....

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Conclusions - Trigger

..."our budget is safe"

- **Design progress good**
  - Design matched to physics performance
    - extensive simulation
  - All parts have at least a conceptual design
  - Many are prototyped or engineering design
- **Extensive prototyping**
  - Many critical items
  - Comprehensive testing program
- **Long R&D program**
  - Extends back to SSC
    - Muons: GEM
    - Calorimeter: SDC
- **Well developed cost & schedule**
  - Fully resource-loaded
  - Contingency by item at lowest level
- **Experience Driven:**
  - Muons: CDF XFT
  - Calorimeter: ZEUS
- **Management structures in place**
  - Well-integrated with CMS