Tests of the CMS Level-1 Regional Calorimeter Trigger Prototypes

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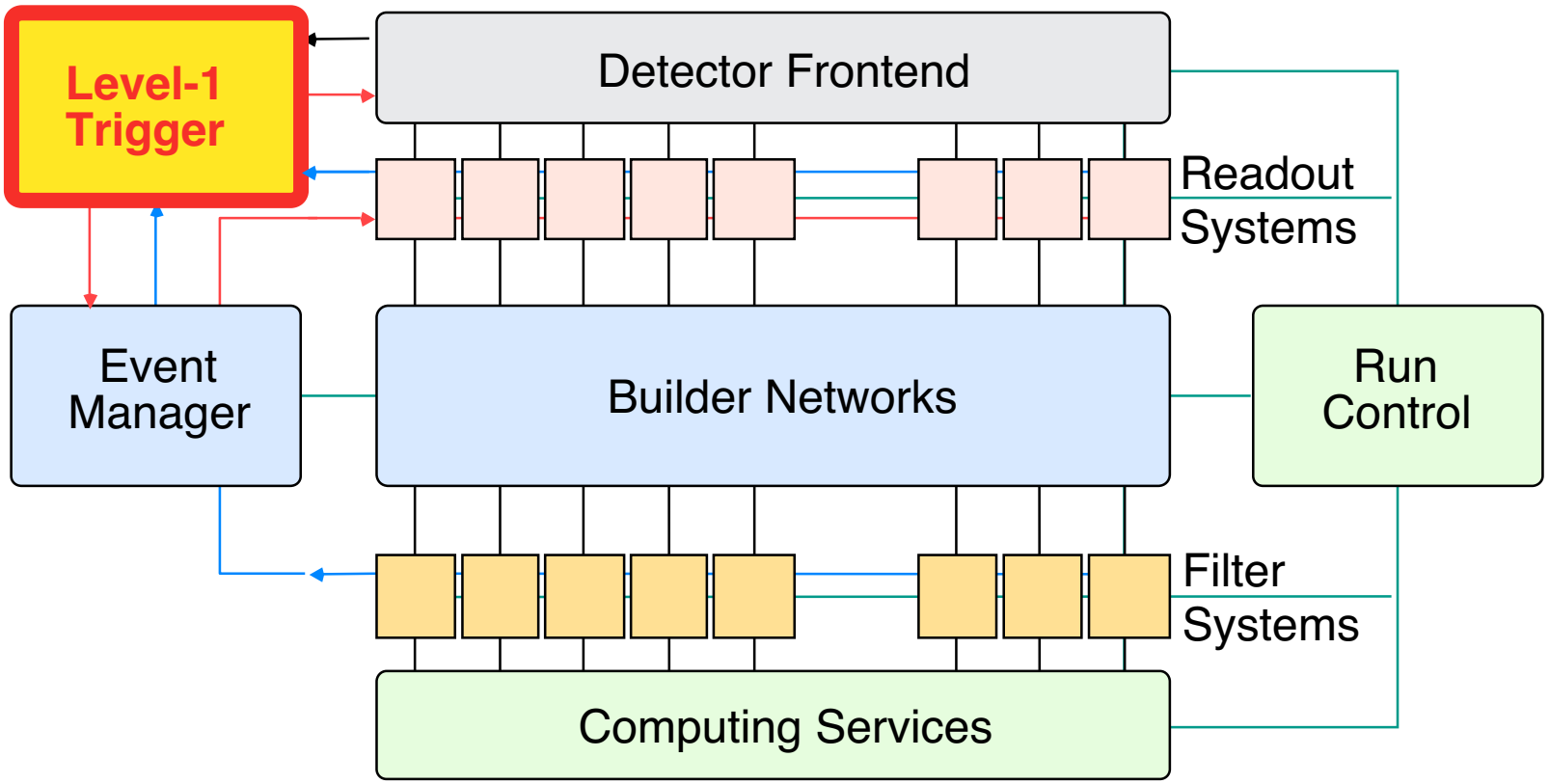
The pdf file of this talk is available at:
http://cmsdoc.cern.ch/~wsmith/LECC02_wsmith.pdf
See also CMS Level 1 Trigger Home page at
http://cmsdoc.cern.ch/ftp/afscms/TRIDAS/html/level1.html

Trigger & DAQ Systems

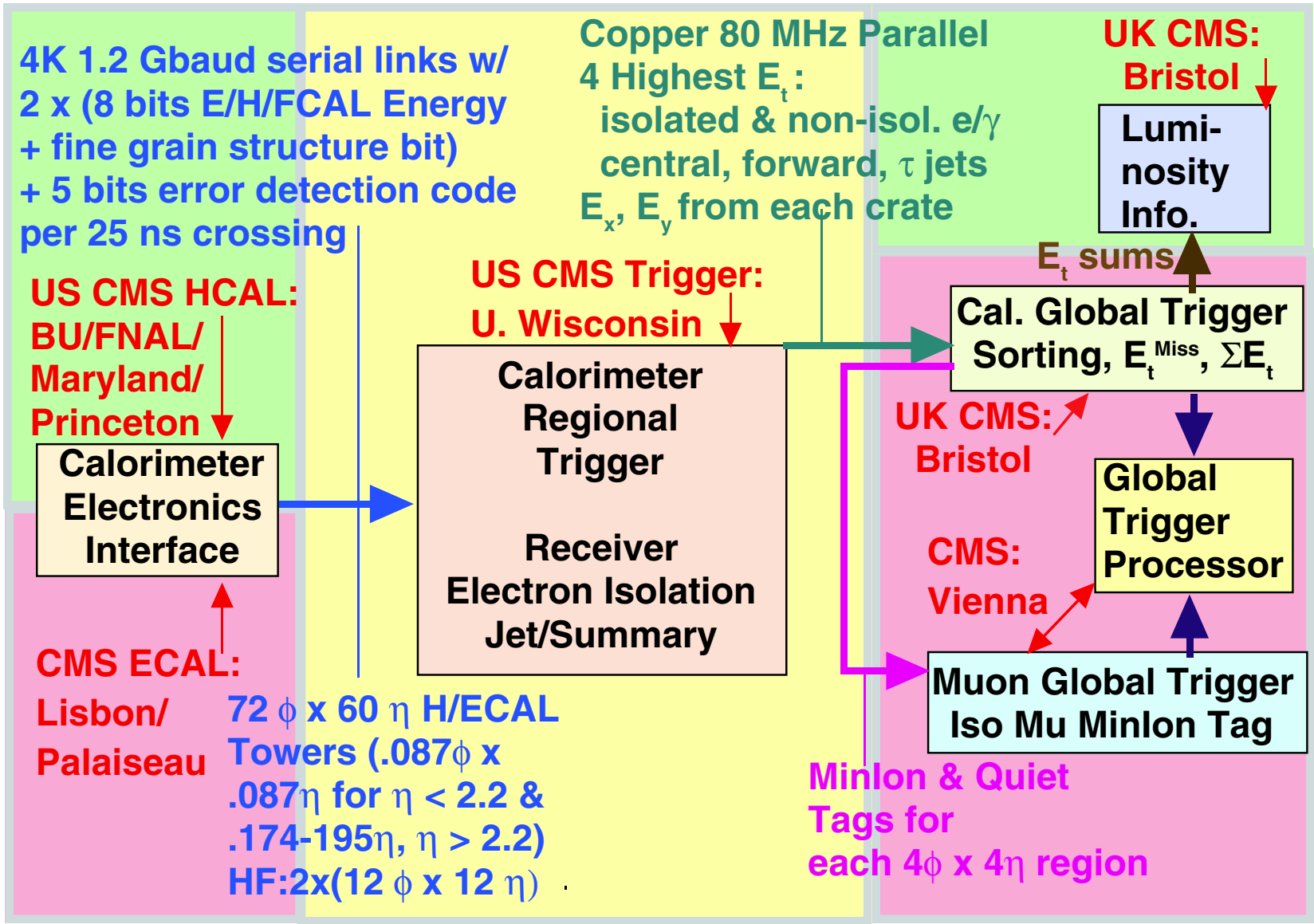


Level-1 Trigger Requirements:

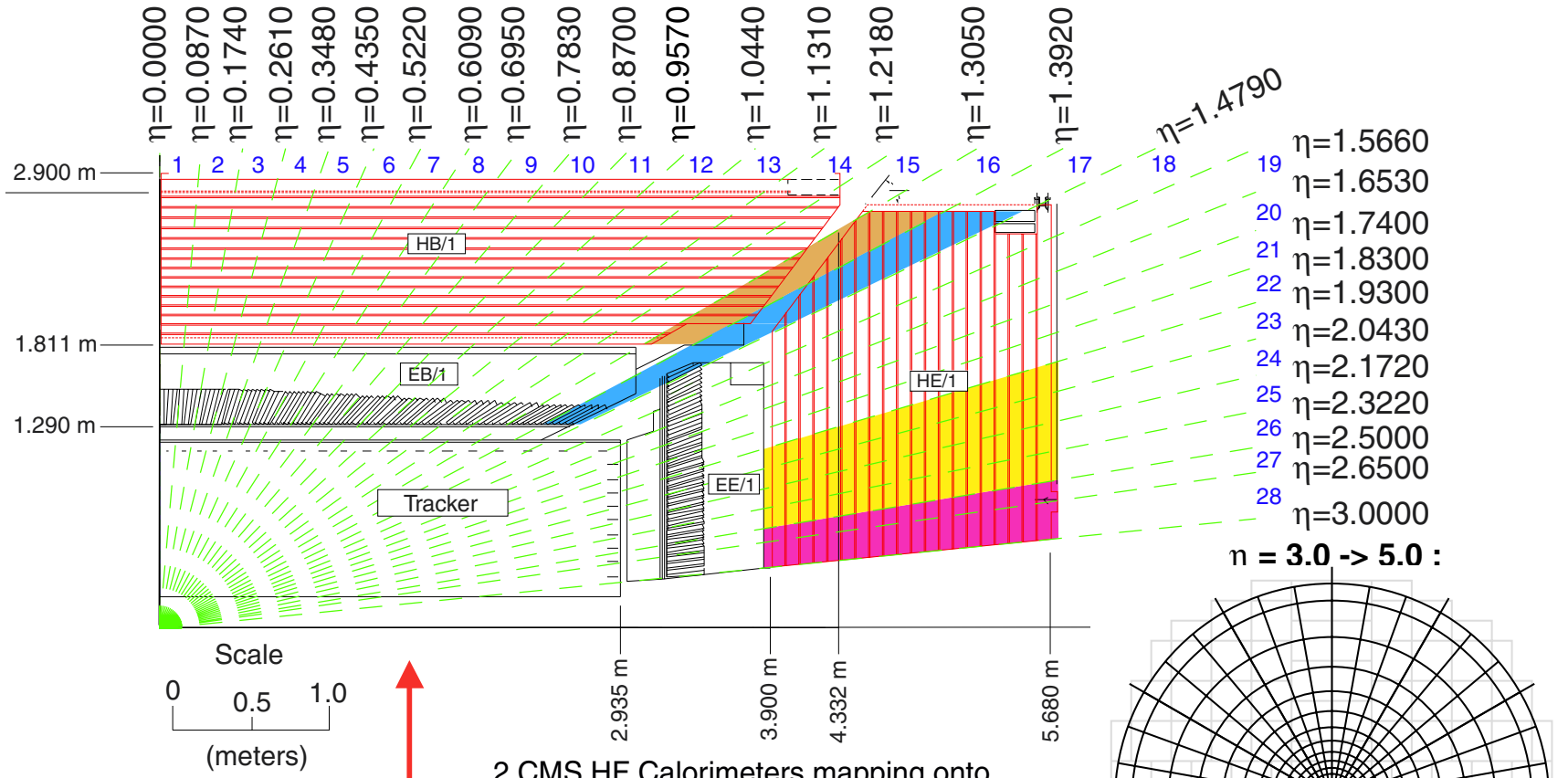
- **Input: 10^9 events/sec at 40 MHz at full $\mathcal{L} = 10^{34}$**
- **Output: 100 kHz (50 kHz for initial running)**
- **Latency: 3 μsec for collection, decision, propagation**

Calorimeter Trig.Overview

(located in underground counting room)



Calorimeter Geometry



EB, EE, HB, HE map to 18 RCT crates

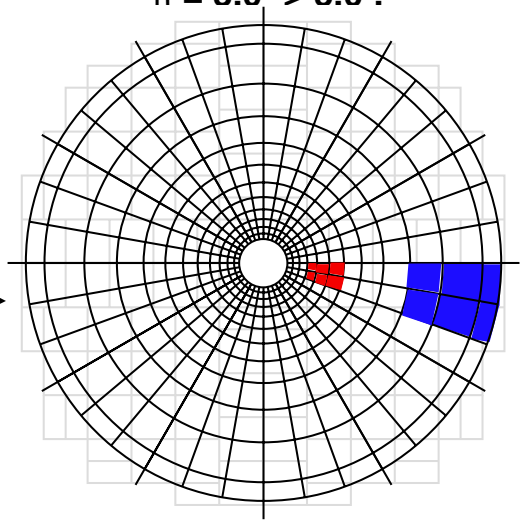
Provide e/γ and jet, τ, E_T triggers

2 CMS HF Calorimeters mapping onto Trigger System HF Crate

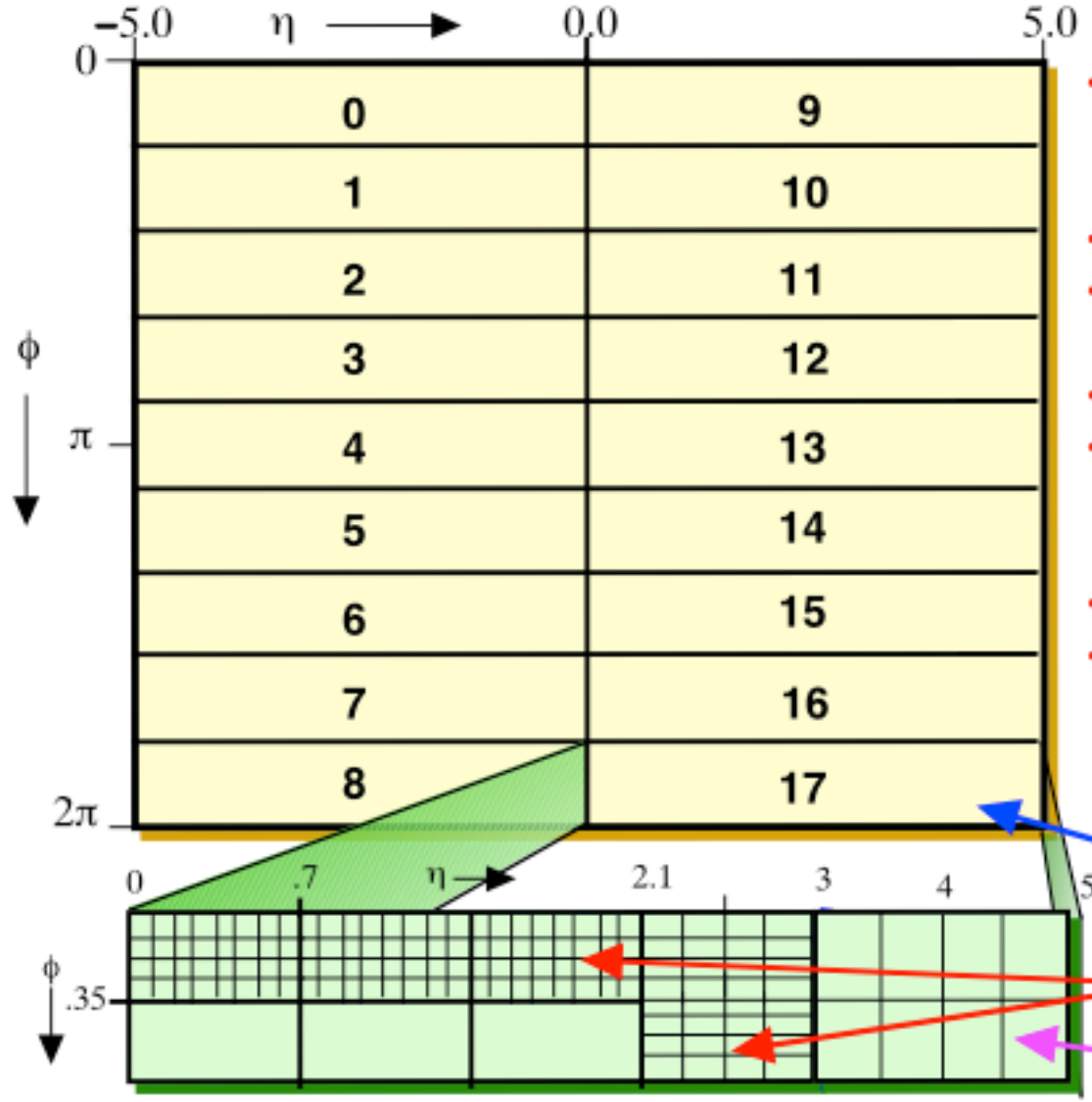
Readout segmentation: 36ϕ × 12η × 2z × 2F/B

Trigger Tower segmentation: 18ϕ × 4η × 2F/B

η = 3.0 -> 5.0 :



Trigger Mapping



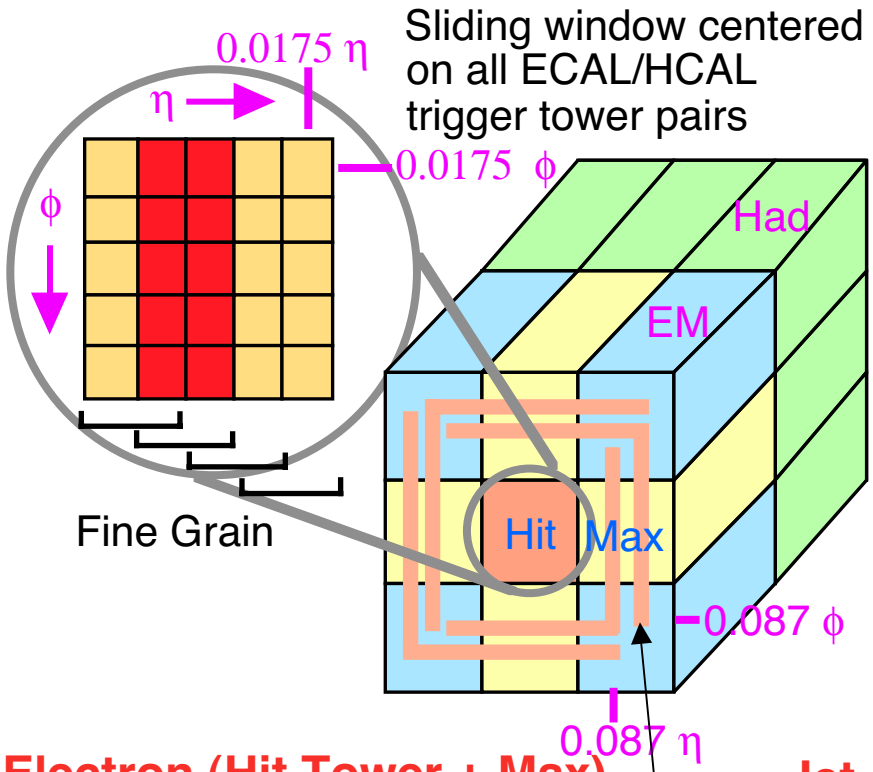
- 18 crates handle all of the CMS calorimeters seamlessly
- Each crate processes a 0.7 ϕ x 5.0 η region.
- Each Receiver/Electron ID card pair typically covers a .35 ϕ x 0.7 η region
- Single Jet/Summary card handles full crate

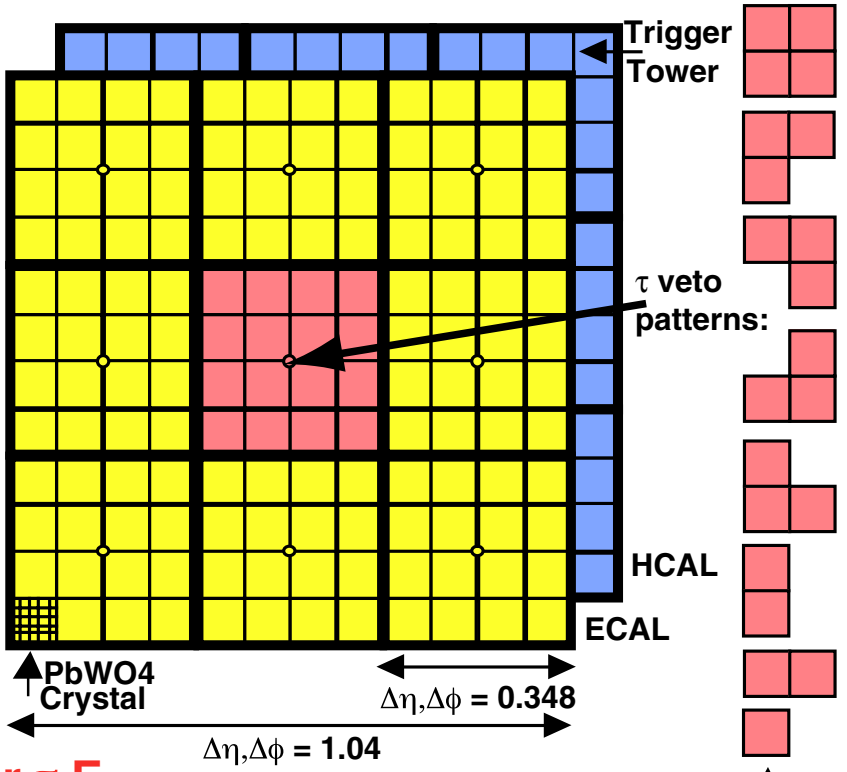
Calorimeter Regional Trigger Crate (18x)

Receiver Cards (x7/crate)

(New) Jet/Summary Card processes HF data (3<η<5)

Calorimeter Trig. Algorithms





Electron (Hit Tower + Max)

- 2-tower ΣE_T + Hit tower H/E
- Hit tower 2x5-crystal strips >90% E_T in 5x5 (Fine Grain)

Isolated Electron (3x3 Tower)

- Quiet neighbors: all towers pass Fine Grain & H/E
- One group of 5 EM E_T < Thr.

Jet or τ E_T

- 12x12 trig. tower ΣE_T sliding in 4x4 steps w/central 4x4 E_T > others

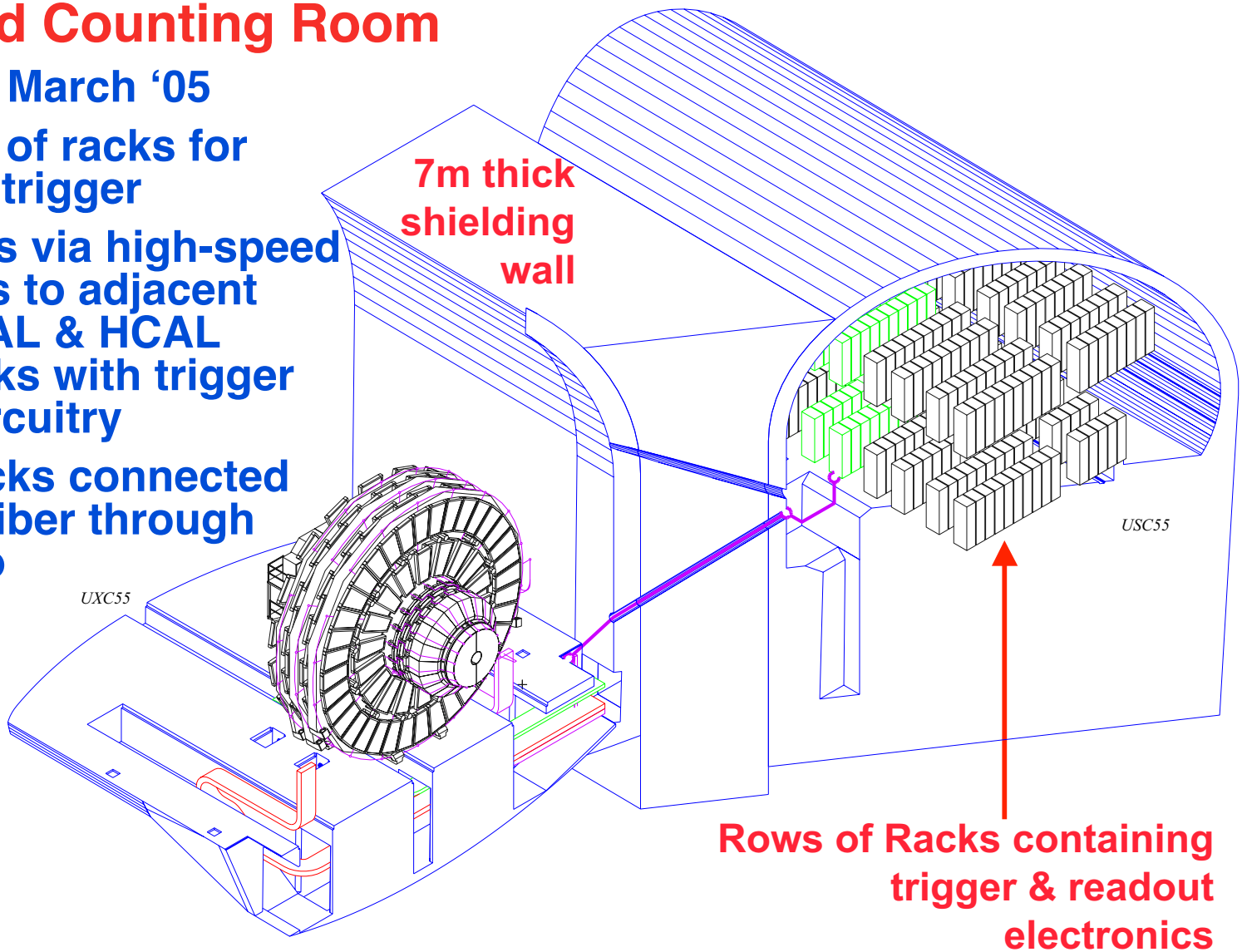
τ: isolated narrow energy deposits

- Energy spread outside τ veto pattern sets veto
- Jet ≡ τ if all 9 4x4 region τ vetoes off

Cal. Regional Trigger Location

Underground Counting Room

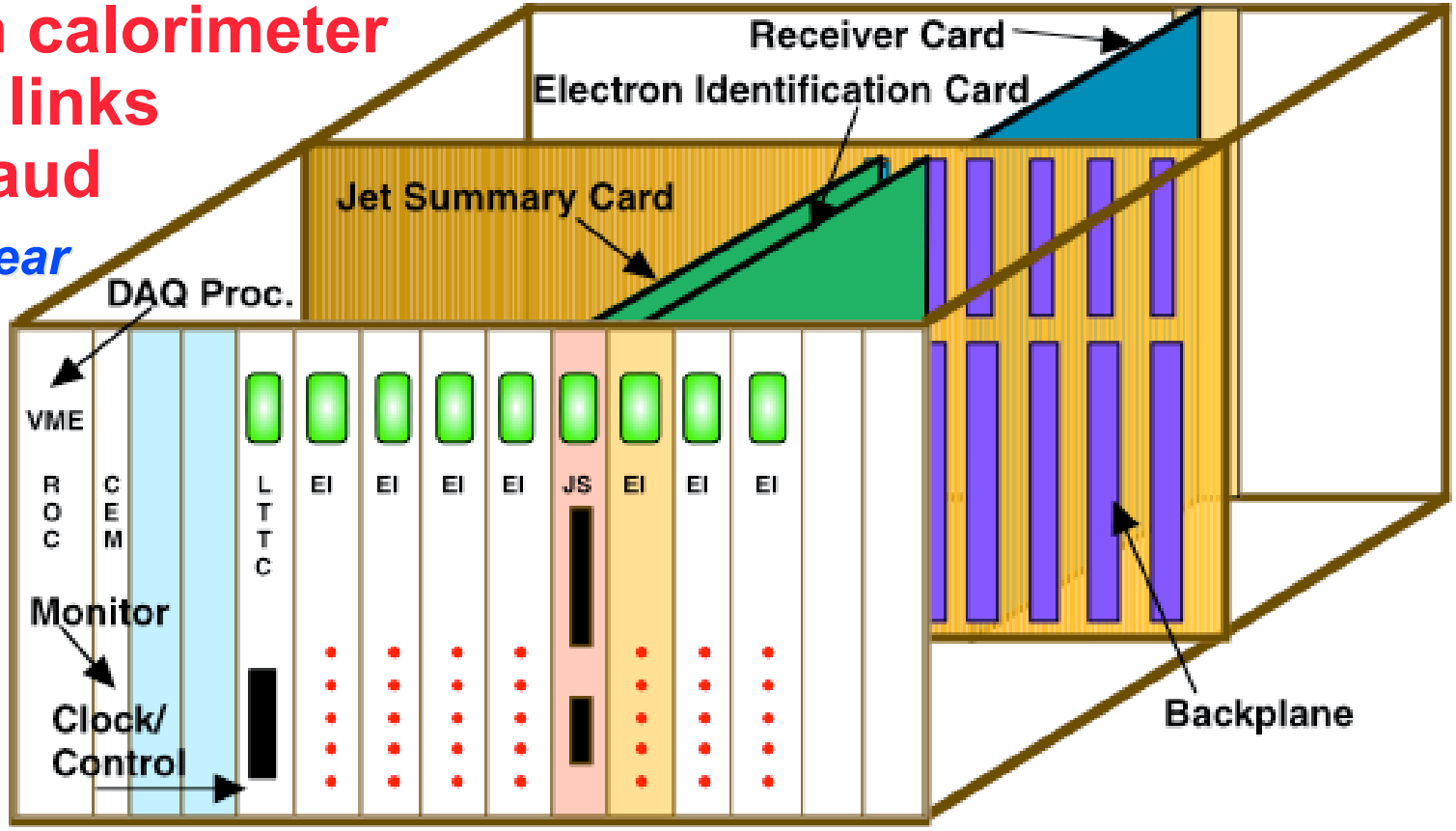
- Planned for March '05
- Central row of racks for calorimeter trigger
- Connections via high-speed copper links to adjacent rows of ECAL & HCAL readout racks with trigger primitive circuitry
- Readout racks connected via optical fiber through "tunnels" to detector (~90m fiber lengths)



Calorimeter Trigger Crate

Data from calorimeter FE on Cu links @ 1.2 Gbaud

- *Into 126* rear Receiver Cards*
- *Prototype tested w/ ASICs*



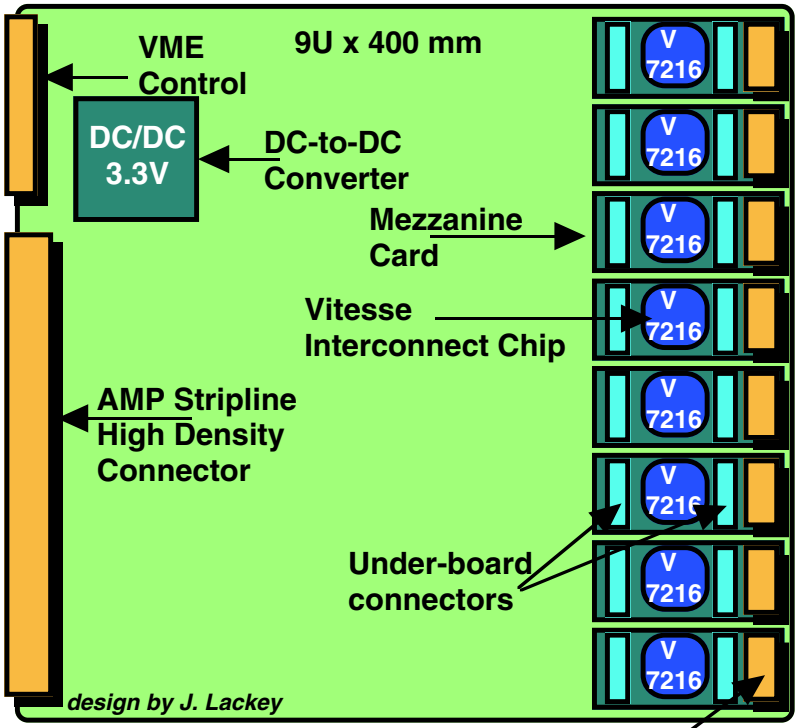
160 MHz point to point backplane (proto. tstd.)

- **18 Clock&Control (proto. tstd.), 126 Electron ID (proto. tstd.), 18 Jet/Summary Cards -- all cards operate @ 160 MHz**
- **Use 5 Custom Gate-Array 160 MHz GaAs Vitesse Digital ASICs**
  - Phase, Adder, Boundary Scan, Electron Isolation, Sort (manufactured)

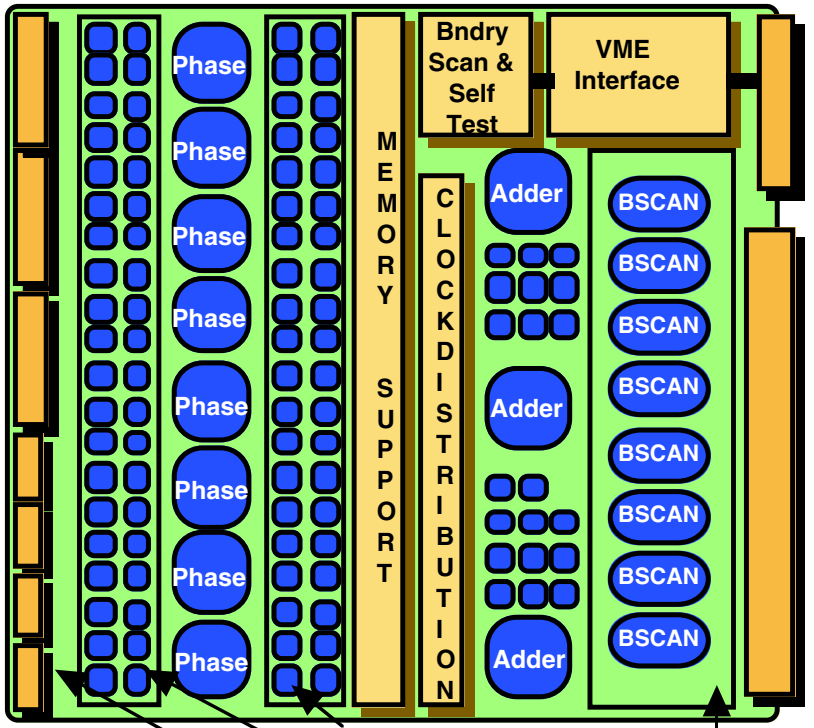
**Spares not included*

Receiver Card

Receiver Card Rear



Receiver Card Front

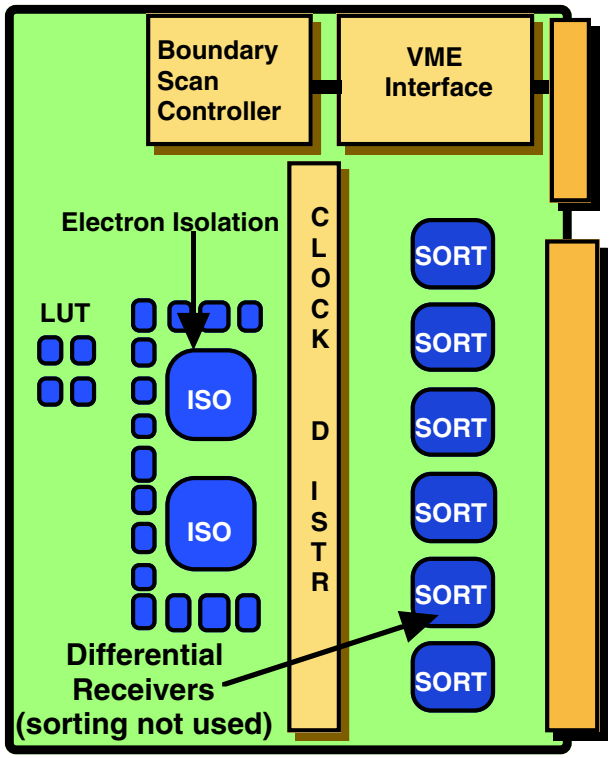


32 Channels =
4 Ch. x 8 mezzanine cards
1.2 GBaud copper rcvrs
18 bit (2x9) data + 5 bit error
Vitesse 4-channel deserializer

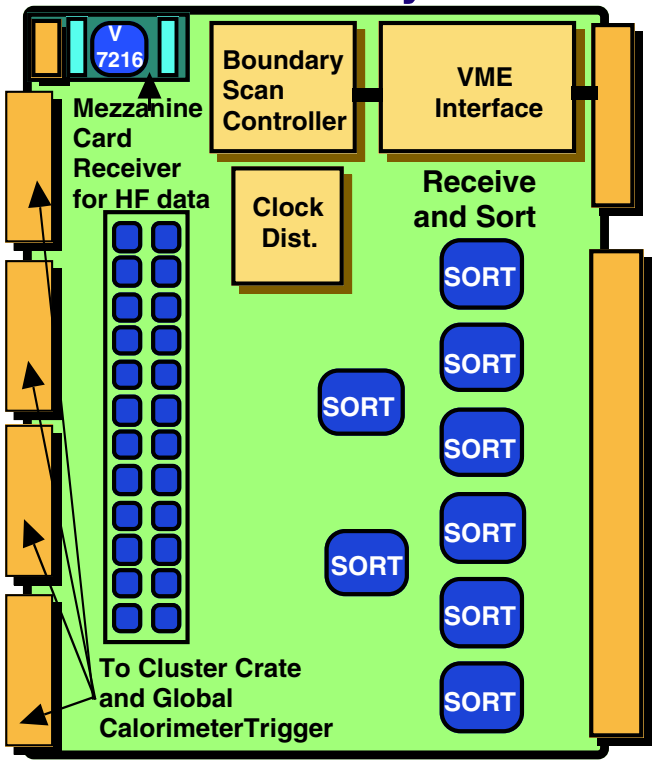
Data from Rear @ 120 MHz TTL
Phase ASIC: Deskew,Mux @ 160MHz
Error bit for each 4x4, Test Vectors
Memory LUT @ 160 MHz
Adder ASIC: 8 inputs @ 160 MHz in 25 ns.
Differential Output@160 MHz

Electron Isolation & Jet/Sumary Cards

Electron Isolation Card



Jet/Summary Card



NEW:

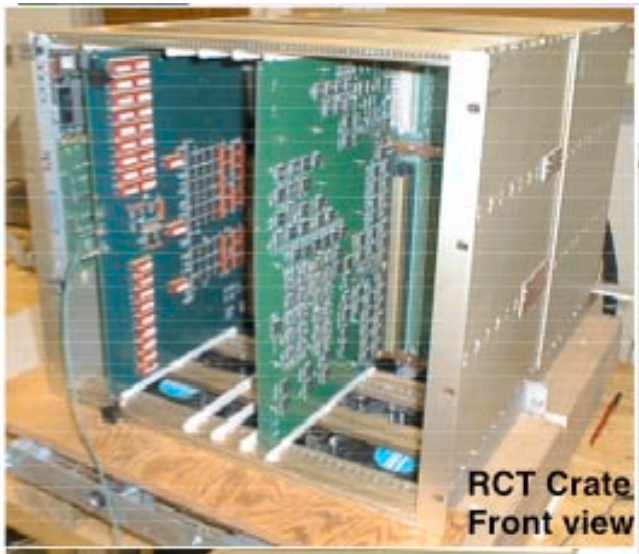
Sends top 4 central forward & tau jets (12 total)

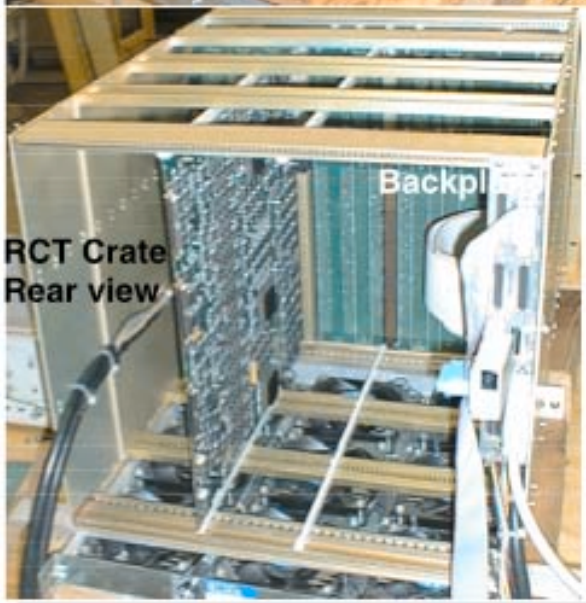
Reads in HF data directly for inclusion in output (extra HF crate gone)

Processes 4x8 region @ 160 MHz
Electron isolation on ASIC
Lookup tables for ranking
Takes Max in each 4x4

Summarizes full crate:
Sorts 32 e's, 4x4 Et → top 4 e's, jets
LUTs: Ex & Ey from Et for 4x4 area
Adder tree for Et, Ex and Ey sums
Quiet/MinI bits for each 4x4 region

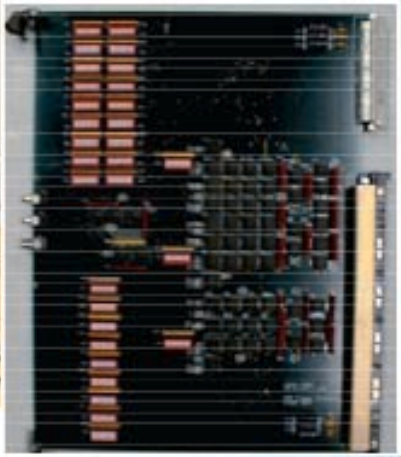
First Generation Prototypes

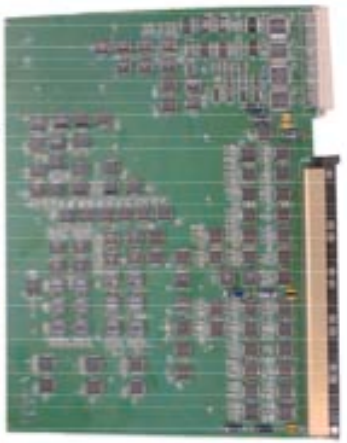




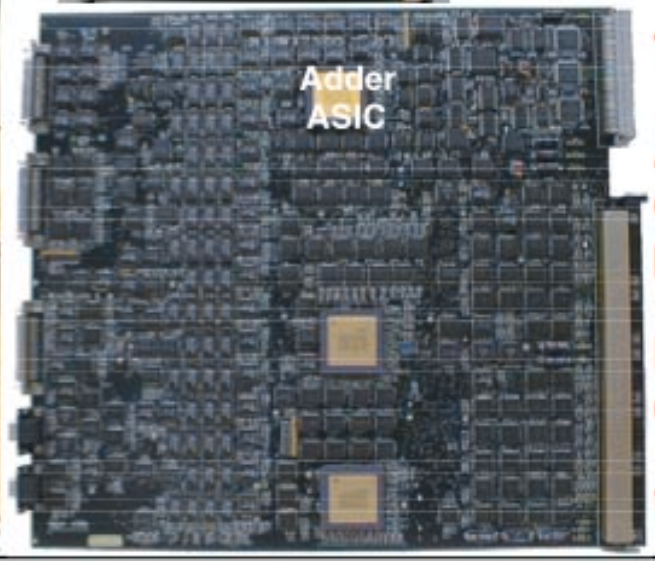
Electron ID Card→

Clock & Control Card





Receiver Card ↓



All Tests Passed

Intercrate sharing checked

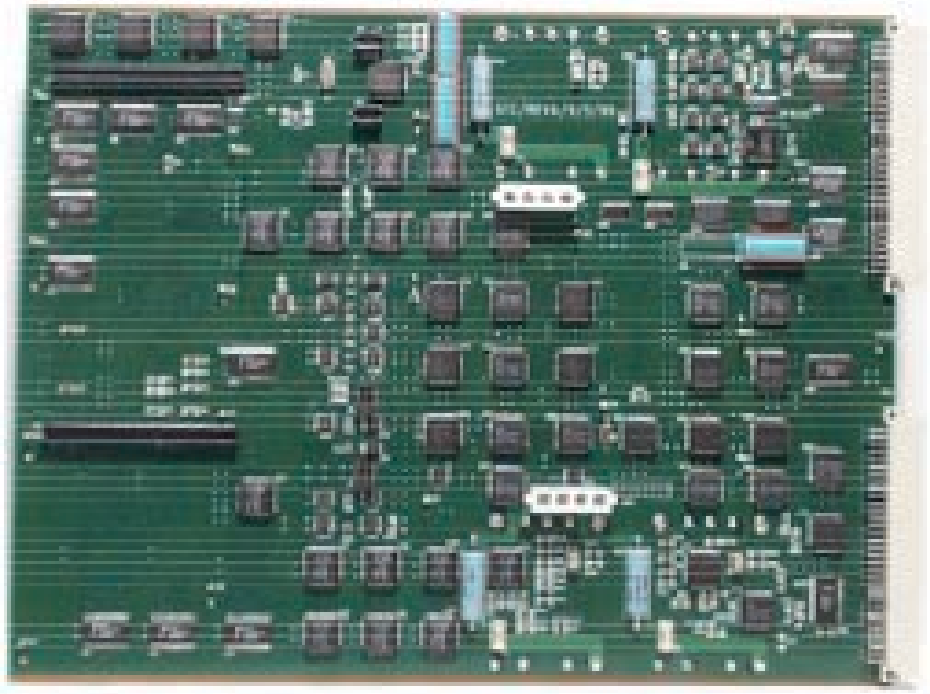
Timing checked

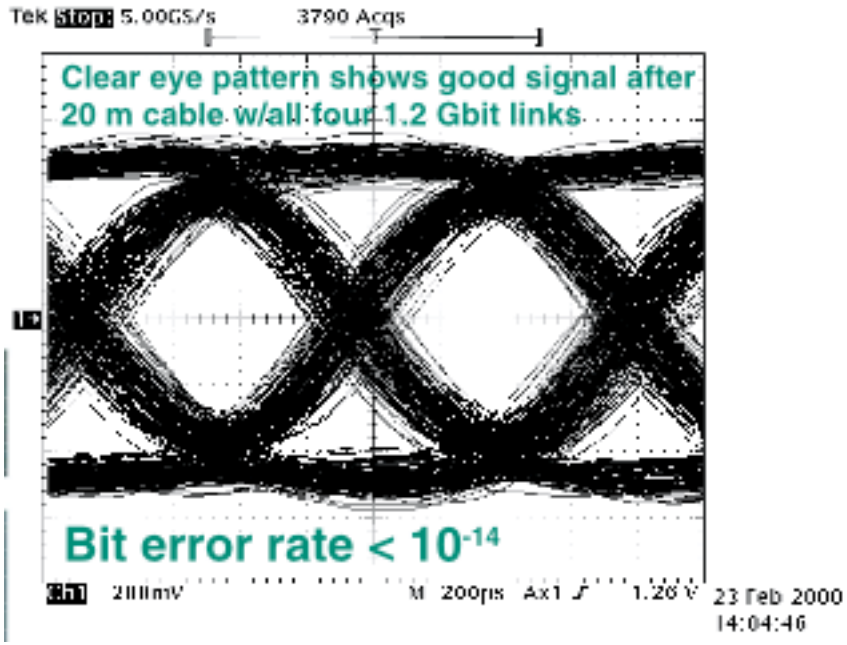
Adder ASIC fully qualified for production

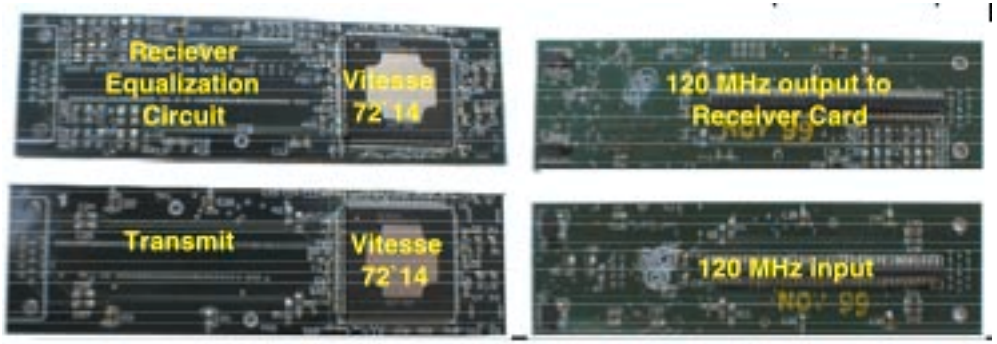
Full 160 MHz dataflow verified

VME checked

First Generation Serial Test Card
Trigger Link Test

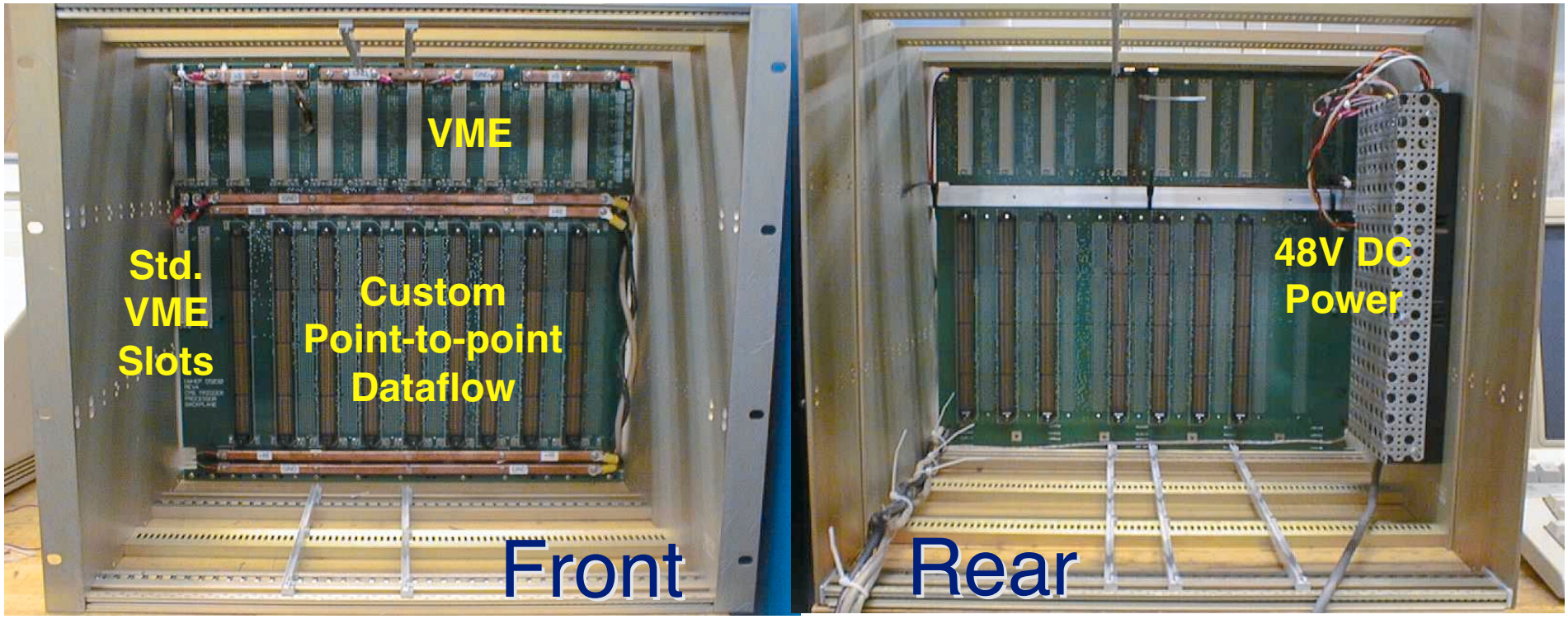






4 x 1.2 Gbaud Cu link between ECAL/HCAL and trigger systems validated with 20 m cable, BER < 10^{-14} Hz

2nd Gen. Crate & Backplane



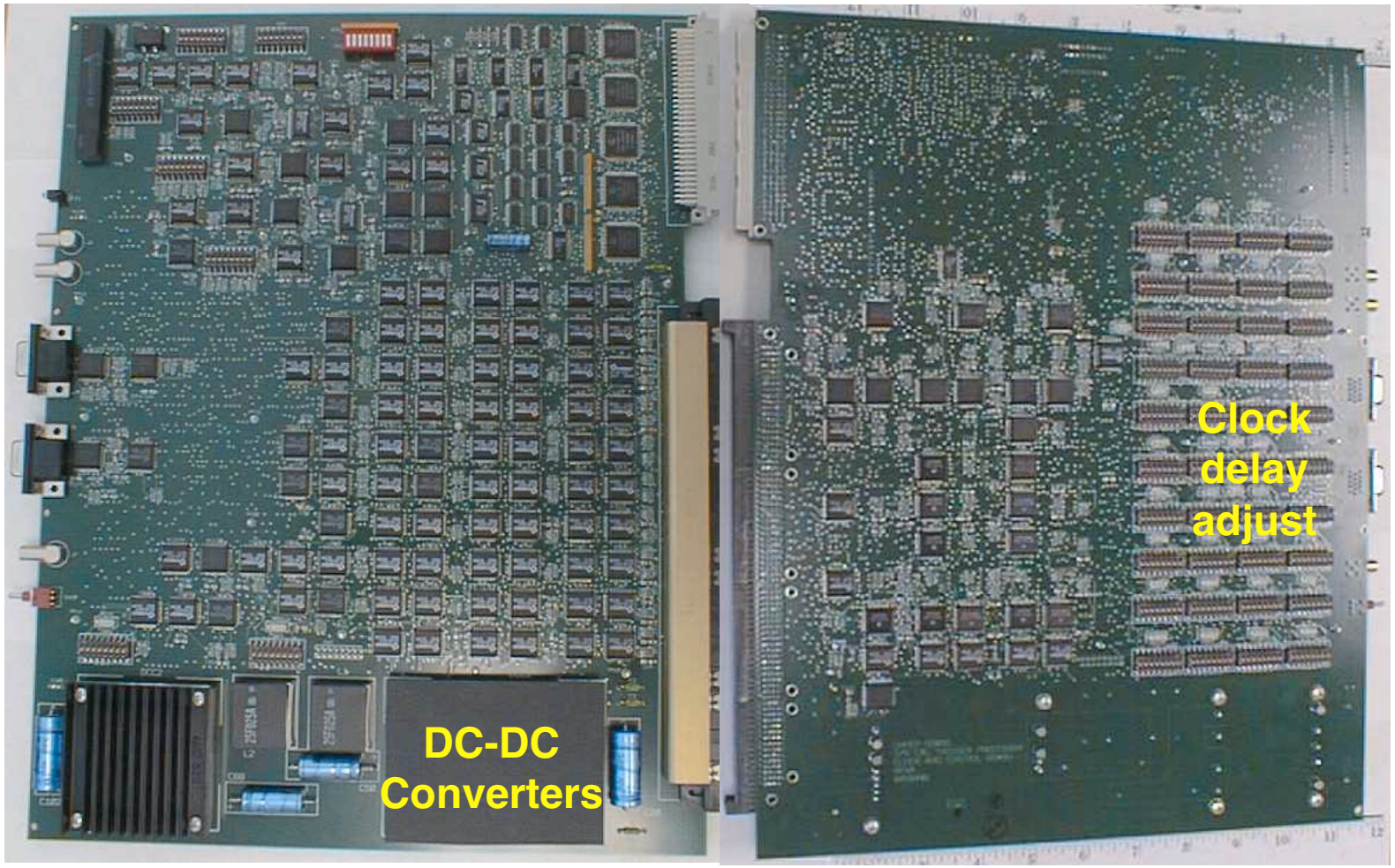
160 MHz with 0.4 Tbit/sec dataflow

- **Initial tests indicate good signal quality**

Designed to incorporate algorithm changes

- **New Non-Isolated Electron, Tau & Jet Triggers**

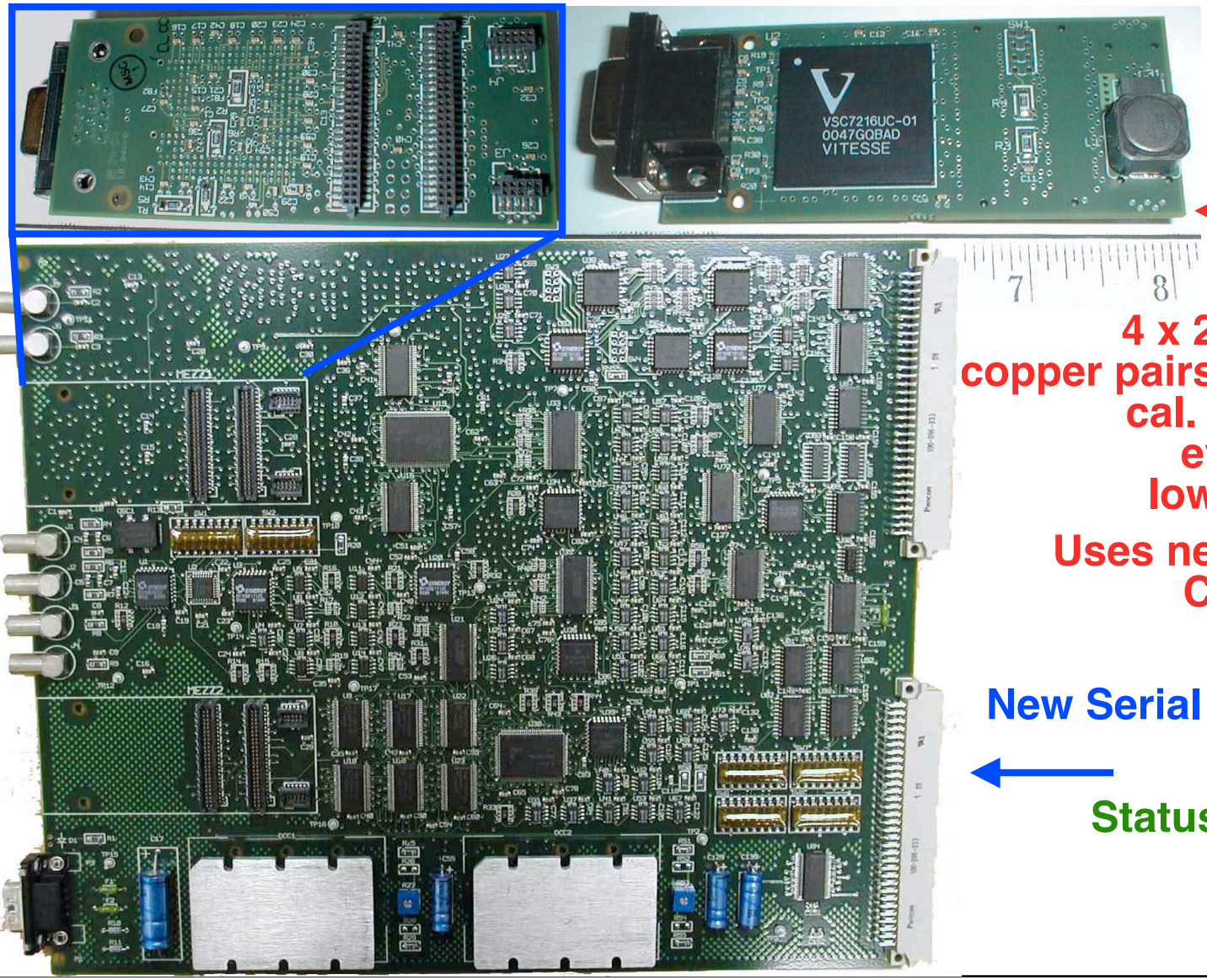
2nd Gen. Clock & Control Card



Fans out 160 MHz clock & adjusts phase to all boards

50% of functionality tested successfully

New Cal. Trig. 4 Gbaud Copper Link Cards & Serial Test Card



8 Compact Mezzanine Cards for each Receiver Card accept 4 x 20 m 1.2-Gbaud copper pairs transmitting 2 cal. tower energies every 25 ns with low cost & power.

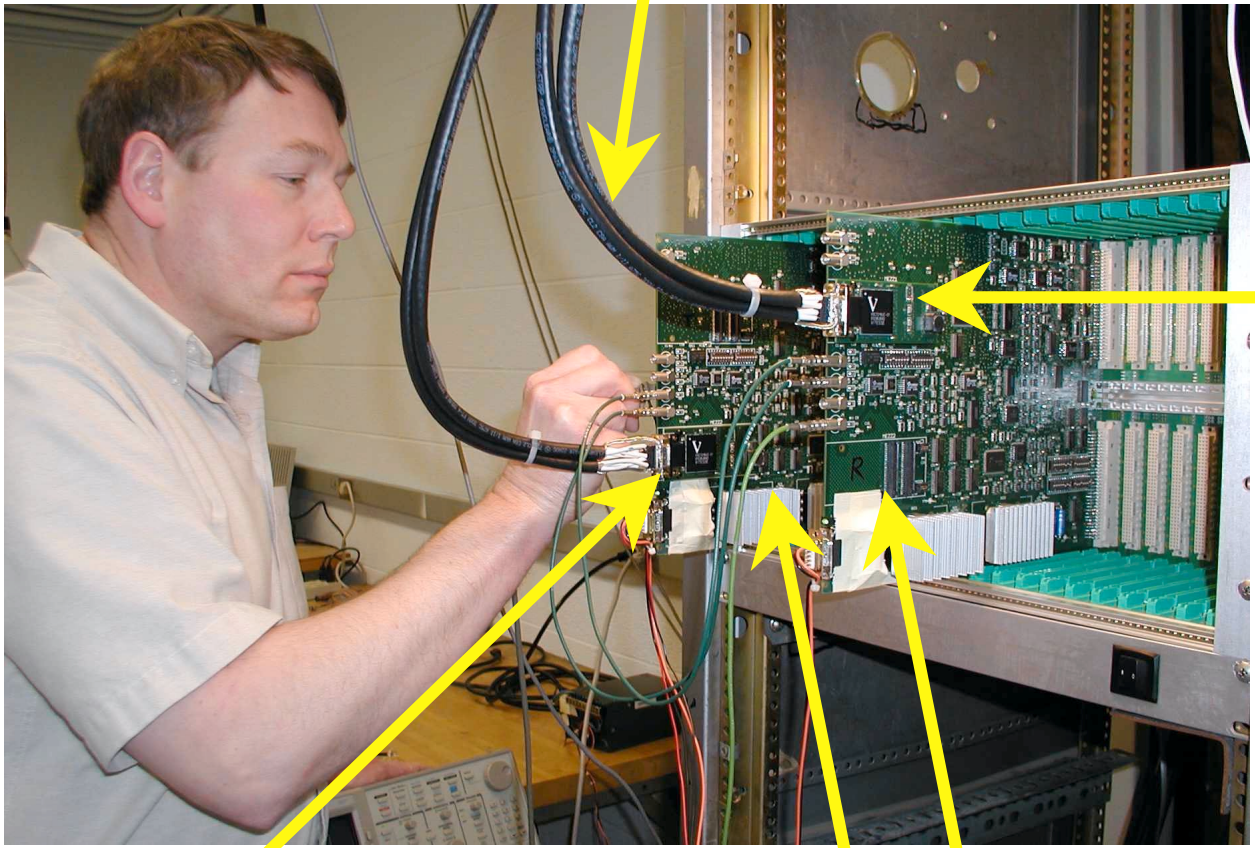
Uses new Vitesse Link Chips (7216-01).

New Serial Link Test Card

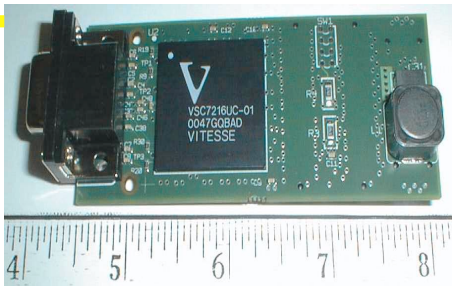
Status: tested and in production

4 x 1.2 Gbaud Copper Link Test Setup

20 m Cu Cable, VGA Connector



Receiver mezzanine card:



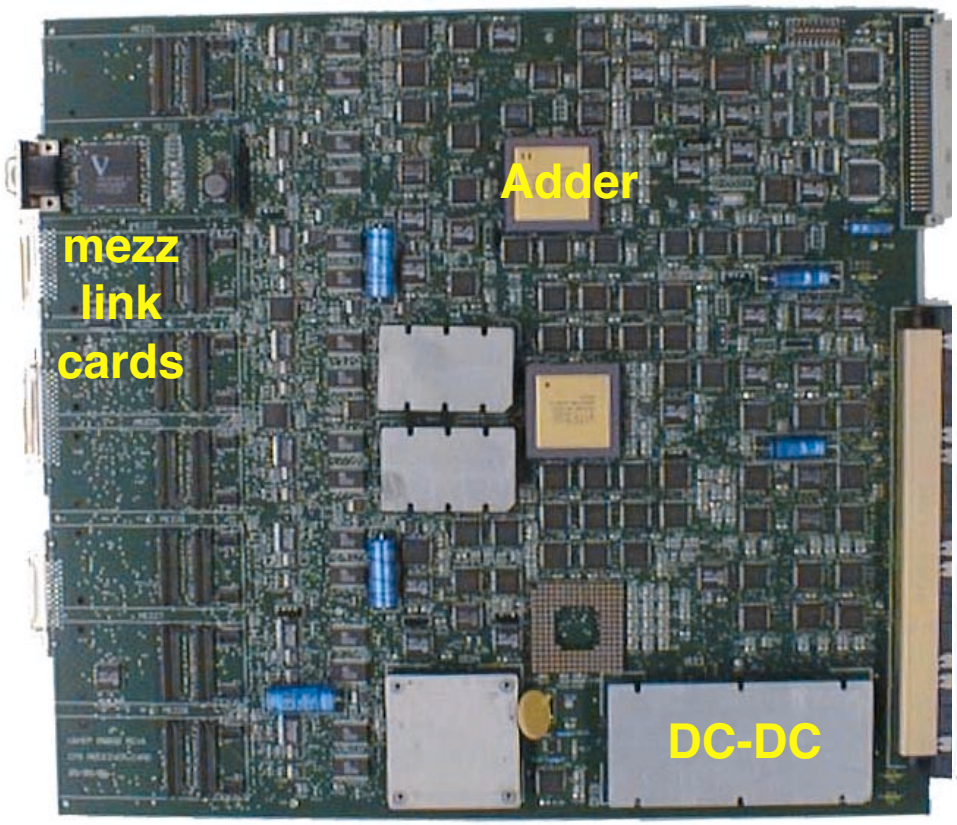
Results:
Bit Error rate < 10^{-15}

Test Transmit mezzanine card

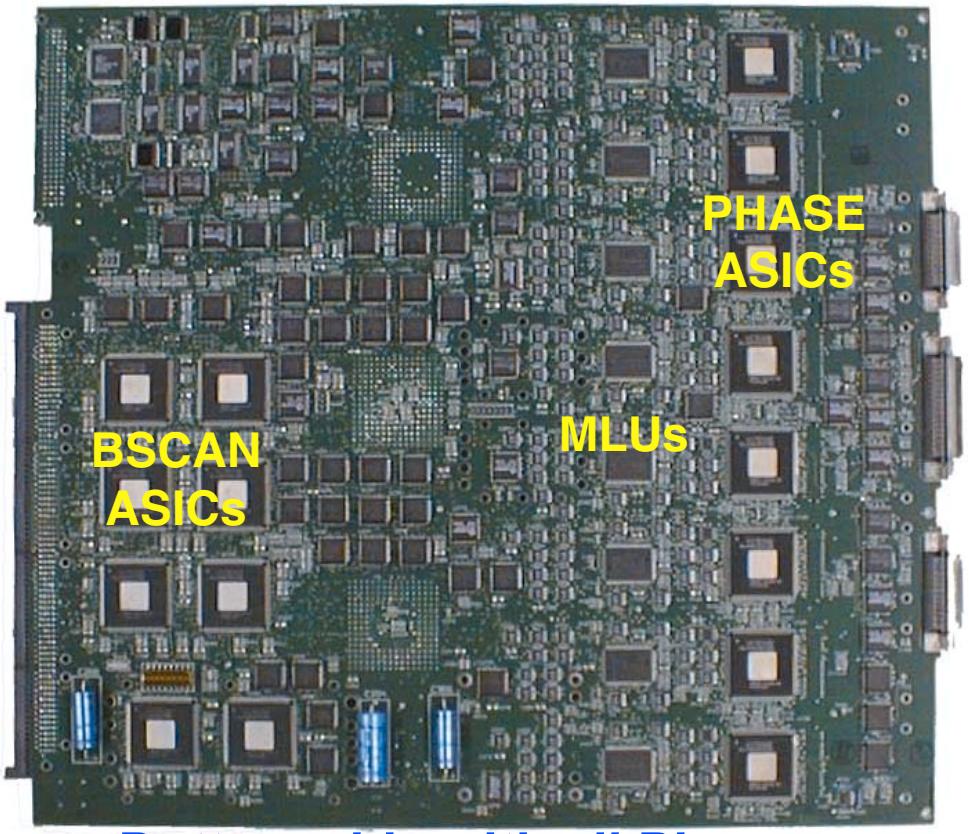
Serial Link Test Cards

2nd Gen. Calorimeter Trigger Receiver Card

Full featured final prototype board in test - initial results are good.
Continue to test on-board ASICs & copper link mezzanine cards

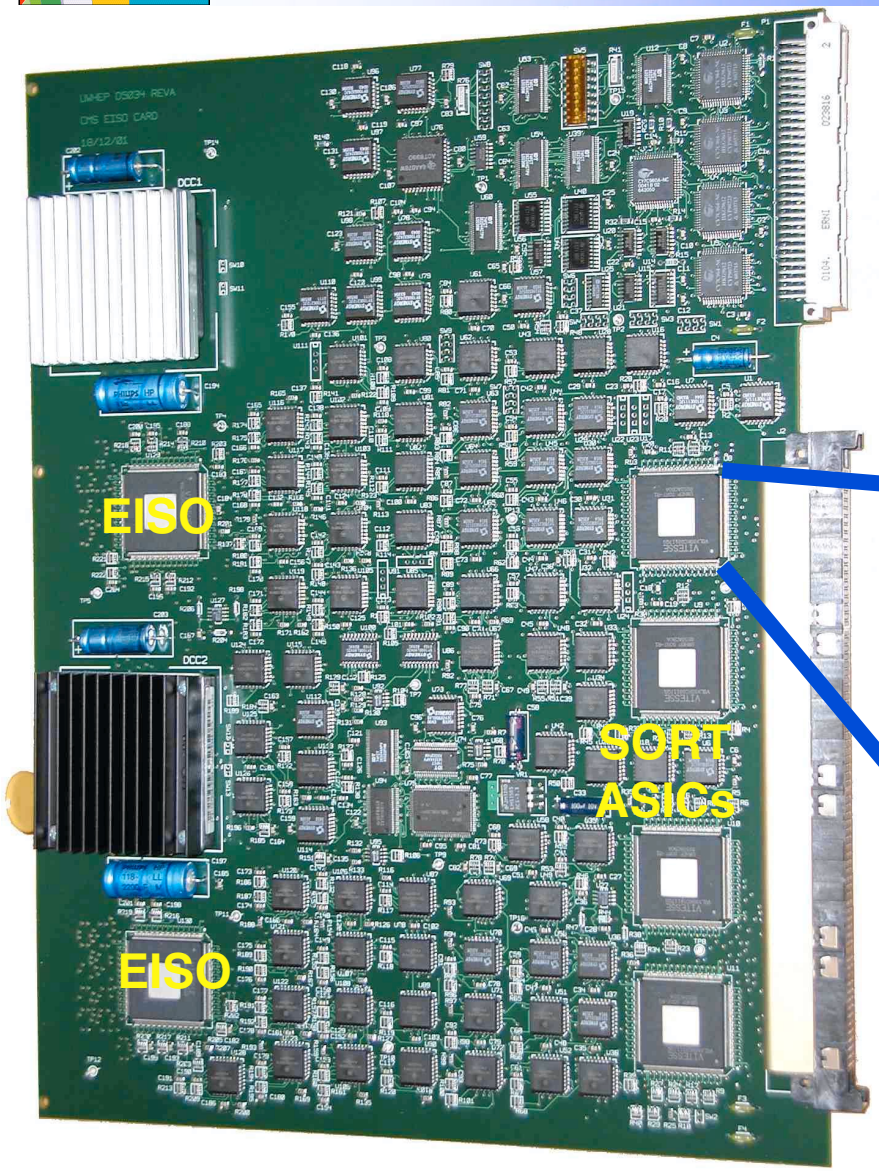


Top side with 1 of 8 mezzanine cards & 2 of 3 Adder ASICs



Bottom side with all Phase & Boundary Scan ASICs

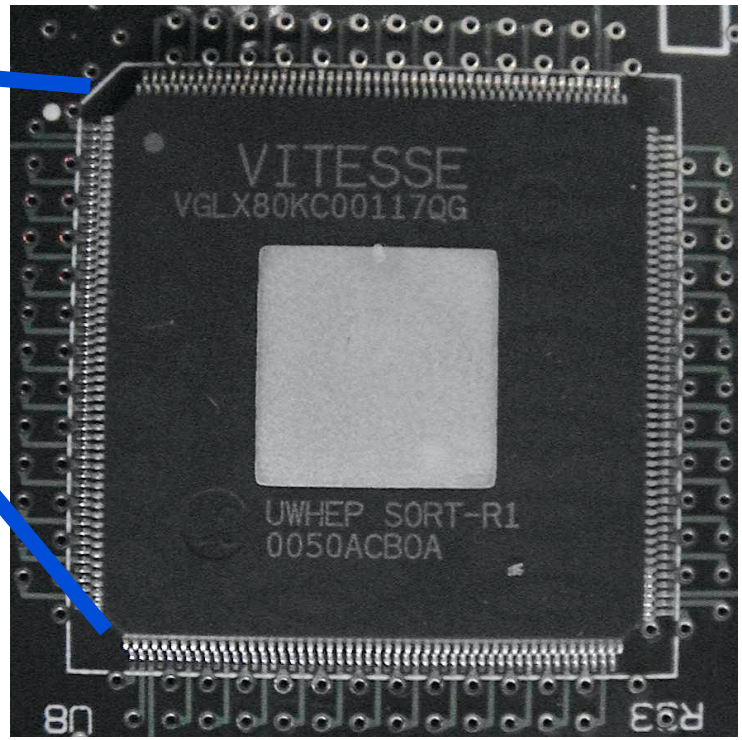
Second Generation Electron Isolation Card



Full featured final prototype board is finished & under test.

Electron ID & Sort ASICs tested by Vitesse before delivery

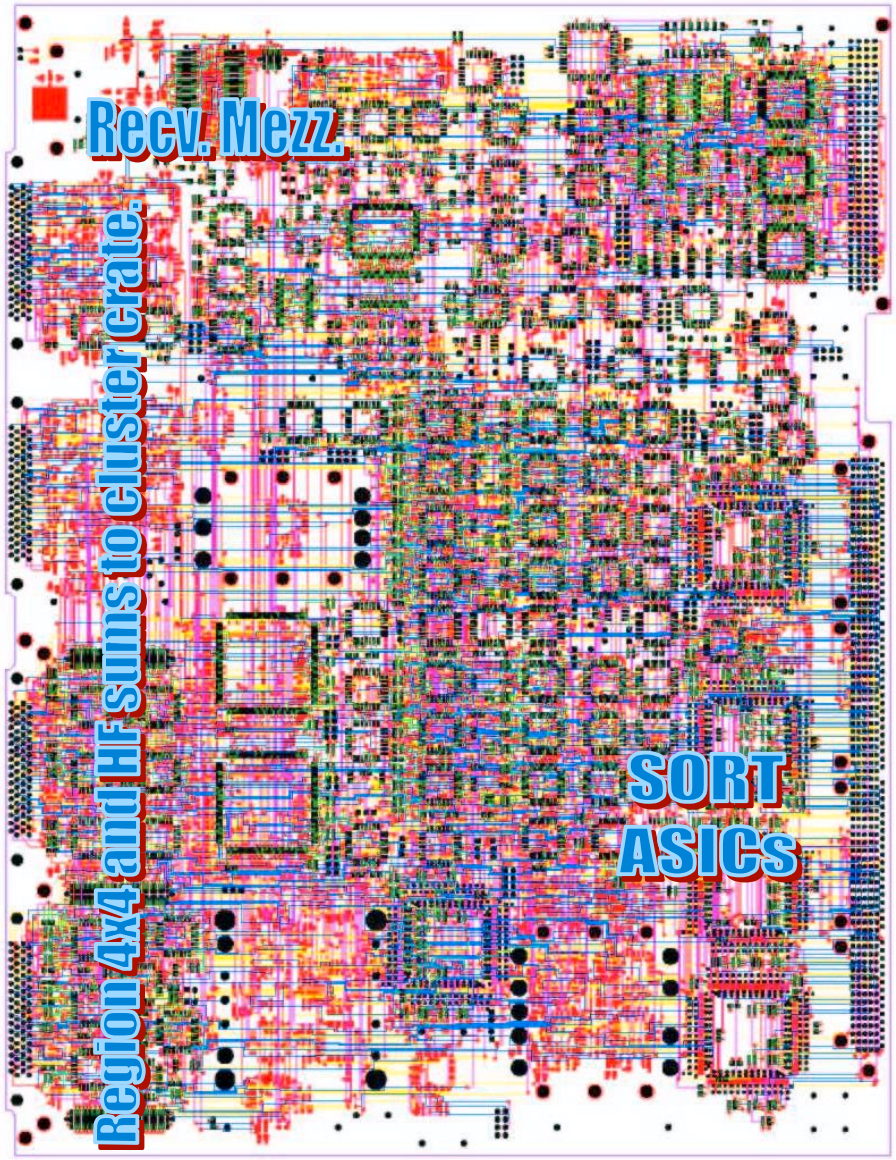
Make further ASIC on-board tests



Jet-Summary Card

Being Manufactured

- **Electron/photon/muon info.**
  - SORT ASICs to find top four electron/photons
  - Threshold for muon bits
  - To GCT
- **Region energies**
  - To cluster crate
- **Absorbs HF functionality**
  - Reuses Receiver Mezzanine Card
  - To cluster crate



Pre-production Prototype Testing

Hand probing of boards

- Timing of signals/clocks checked
- Data paths checked

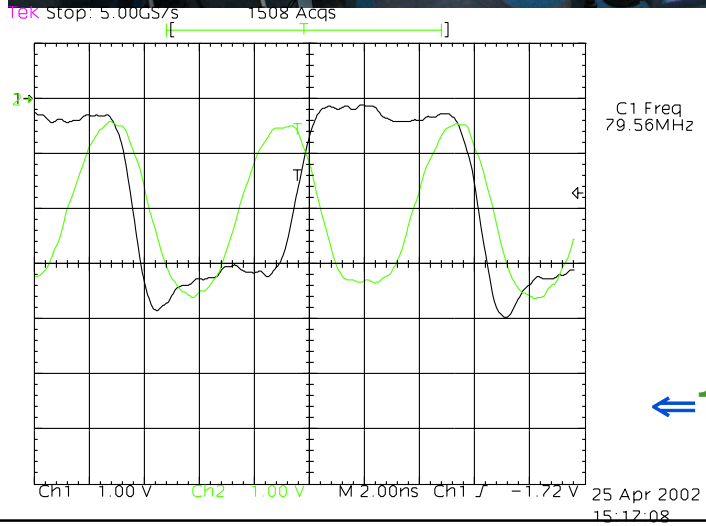
Inject known data from Serial Link Test Card

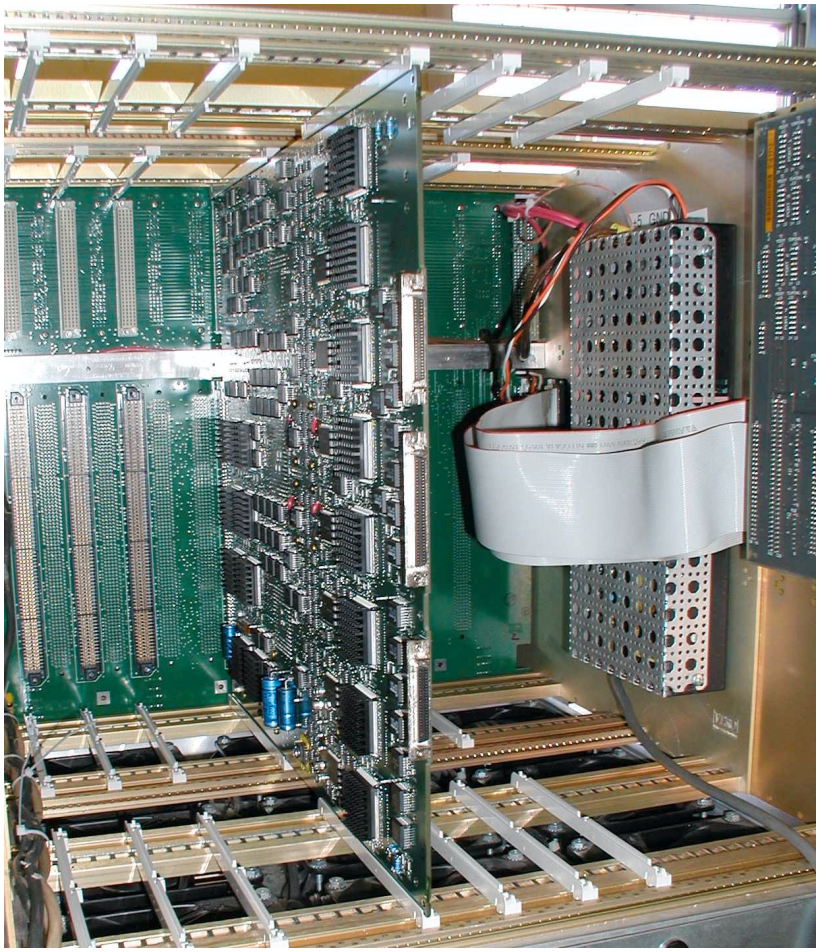
- Receiver Card memories loaded & known data sent out in "test" mode

Detailed use of JTAG to check data paths on board

- Fully implemented on all boards and ASICs
  - Access JTAG through VME interface
- Use to check ASIC to ASIC data paths in detail
  - Easier to spot loose connections, bad solder joints
- Building fault library for Receiver & Electron Isolation Cards for production testing
  - Programs for uniform testing of cards

Testing New Receiver & Clock Cards, Crate, Backplane





⇐160 MHz TTL clock with data into 200 MHz Memories (2 ns scale)

Conclusions

Conducting second generation prototype tests

- **Crate, Backplane, CCC, RC, Receiver Mezzanine Card, Phase & Boundary Scan ASICs under test -- results good**
  - Phase ASIC validated & production complete
  - Adder ASIC already validated & production complete
- **Serial Link Test Card & Transmitter MC tested & in production**
- **Electron Isolation Card & EISO & SORT ASICs under test**
  - Sort ASIC Validated & production complete

Goals for 2002/3

- **Completion of prototype tests, validate last two ASICs**
- **Integrate Serial Links w/ECAL, HCAL front-ends**
- **Prototype Jet/Summary card manufacture**
  - Ready for manufacture -- waiting for other board tests
  - Integrated HF into this card -- no need for separate HF crate
- **Begin System Production & Test**