CMS Level 1 Trigger

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CMS

Overview & Recent Progress:

- Calorimeter Trigger
- Muon Trigger
- Global Trigger

Organization, Cost, Schedule

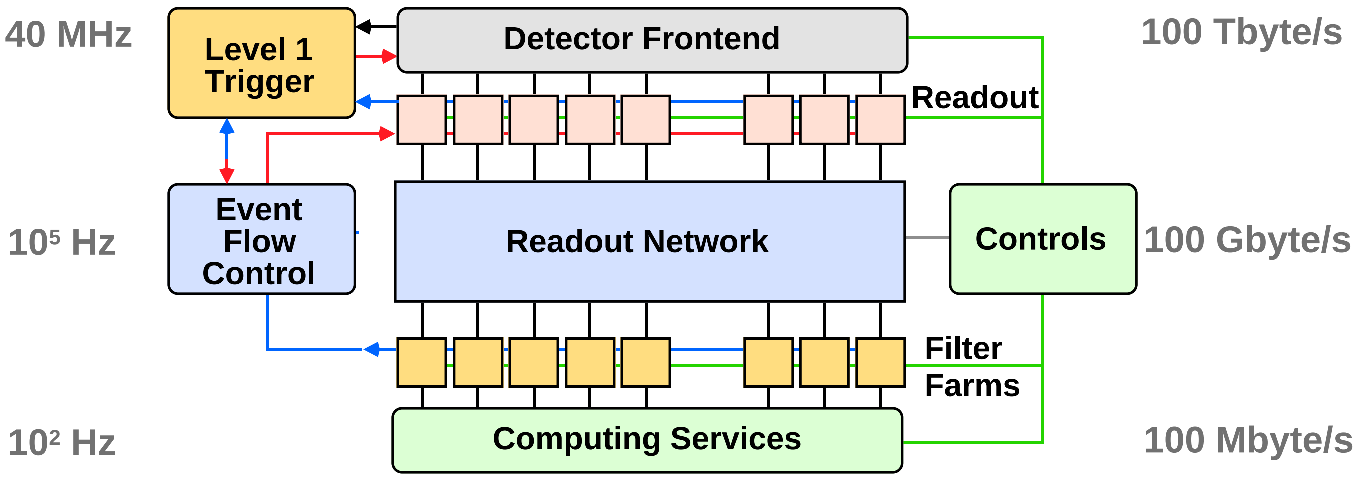
The pdf file of this talk is available at:

http://cmsdoc.cern.ch/~wsmith/LHCC_Jan99.pdf

See also CMS Level 1 Trigger Home page at

http://cmsdoc.cern.ch/ftp/afscms/TRIDAS/html/level1.html

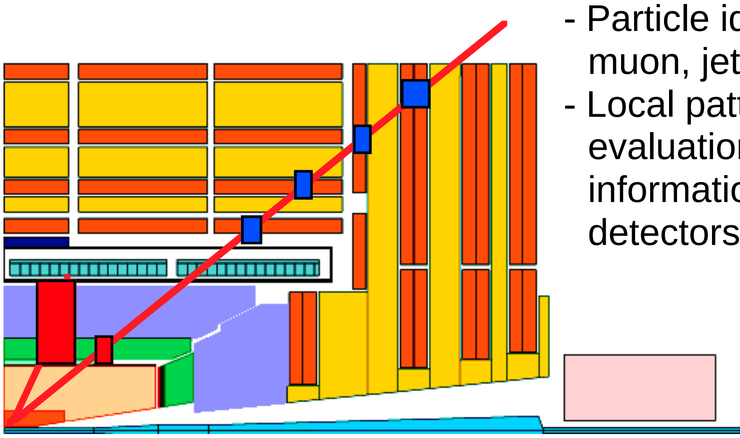
Basic Structure



Collision rate		40 MHz
Level-1 Maximum trigger rate		100 kHz
Average event size	≈	1 Mbyte
No. of In-Out units (200-5000 byte/event)		1000
Readout network (512-512 switch) bandwidth	≈	500 Gbit/s
Event filter computing power	≈	5 10^6 MIPS
Data production	≈	Tbyte/day
No. of readout crates	≈	250
No. of electronics boards	≈	10000

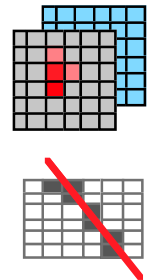
CMS Trigger Levels

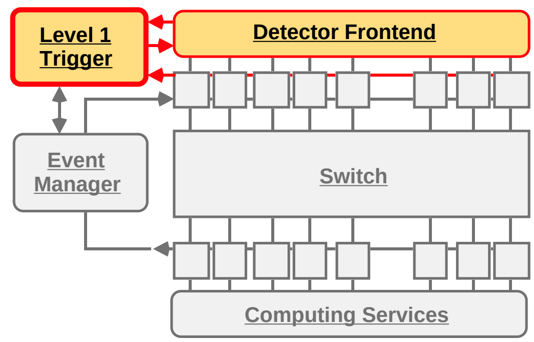
40 MHz



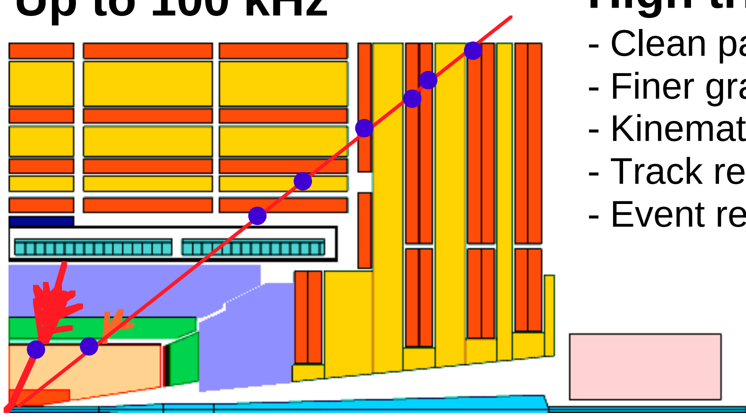
Level-1. Specialized processors

- Particle identification: high p_T electron, muon, jets, missing E_T
- Local pattern recognition and energy evaluation on prompt macro-granular information from calorimeter and muon detectors



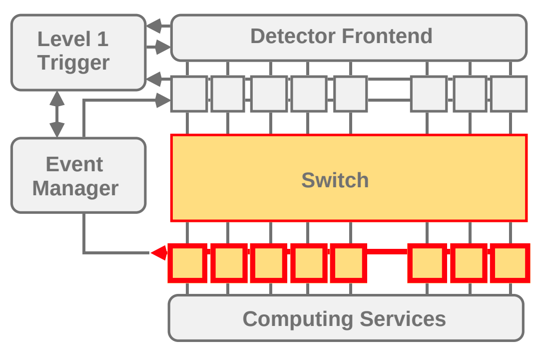


Up to 100 kHz

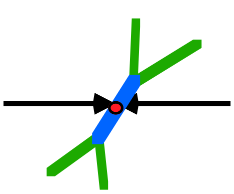


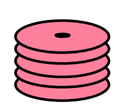
High trigger levels. Network and CPU farms

- Clean particle signature
- Finer granularity precise measurement
- Kinematics. effective mass cuts and event topology
- Track reconstruction and detector matching
- Event reconstruction and analysis



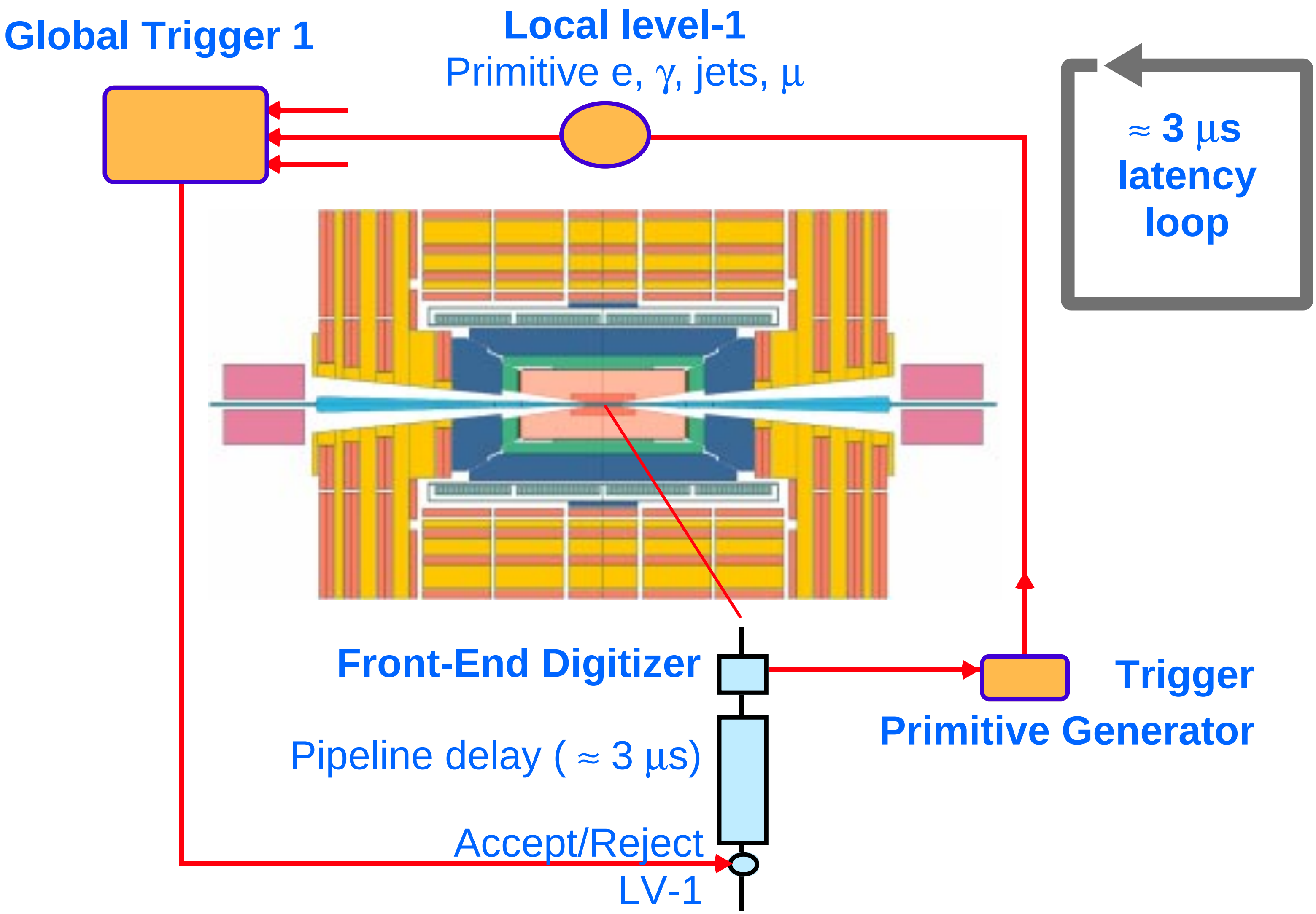
≈ 100 Hz





Level-1 trigger system

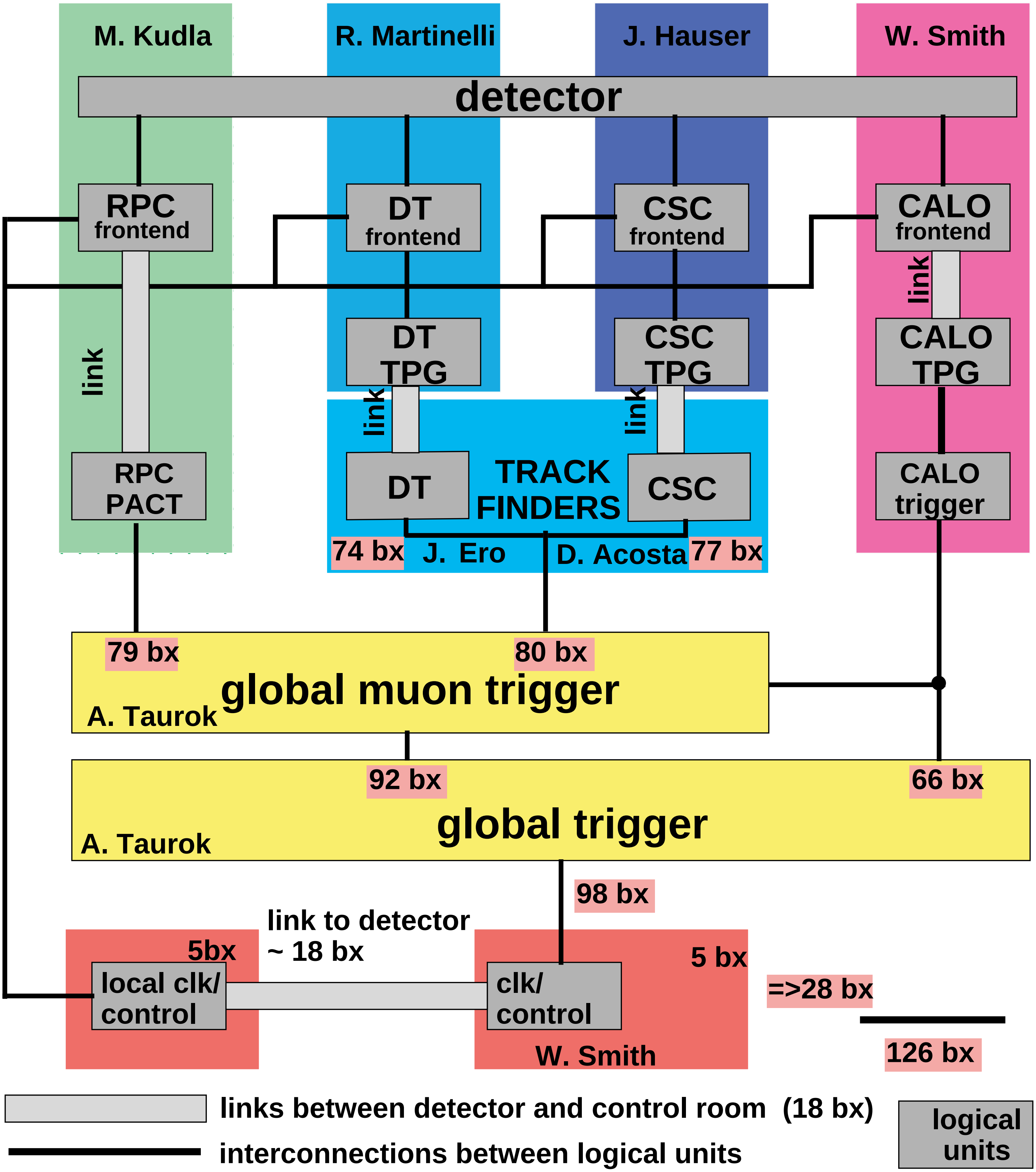
Communication Loop:



Synchronous 40 MHz digital system

- **160 MHz internal pipeline**
- **Readout and processing latency < 1μs**
- **Signal distribution latency ≈ 2 μs**

Level 1 Latency



CMS/LHC Trigger Physics

Standard model Higgs (high luminosity)

- H (80 GeV) $\rightarrow \gamma\gamma$
- H (120 GeV) $\rightarrow$ Z Z* (4 leptons)
- H (>500 GeV) $\rightarrow$ leptons (+ ν's)
- H (< $2M_w$ Associated t or W or Z) $\rightarrow$ b b (lepton + X)

SUSY Higgs (low luminosity)

- (standard model Higgs like channels)
- h, H, A $\rightarrow \tau\tau$ (lepton + X) or $\rightarrow \mu\mu$
- A $\rightarrow$ Z h ; h $\rightarrow$ bb (lepton + X)
- p p $\rightarrow$ t t X; t $\rightarrow H^+$ b; $H^+ \rightarrow \tau\nu$; t $\rightarrow$ lepton + X; $\tau \rightarrow$ X

SUSY sparticle searches (low luminosity)

- MSSM sparticle $\rightarrow$ LSP (Missing E_t) + n jets
- MSSM sparticle $\rightarrow$ Same sign dileptons + X

Other new particles

- Z' $\rightarrow$ dileptons
- Leptoquarks: dileptons

Top physics (low luminosity)

- t $\rightarrow$ lepton + X
- t $\rightarrow$ multijets

Bottom physics (low luminosity)

- b $\rightarrow$ lepton + X
- b $\rightarrow \psi k_s$ (leptons + X)

QCD

- Low luminosity 100 GeV jets
- High luminosity 200 GeV jets

$\Rightarrow$ Trigger candidate requirements:

- High luminosity: lepton/γ (30 GeV), dileptons/$\gamma\gamma$ (15 GeV) missing E_t (100 GeV), jets (200 GeV)
- Low luminosity: lepton/γ (15 GeV), dileptons/$\gamma\gamma$ (10 GeV) missing E_t (50 GeV), jets (100 GeV)

Cal. Trigger requirements

Input

- **ECAL trigger towers, 0.087ϕ x 0.087η**
- **Matching HCAL towers**
- **Data every 25ns - including any corrections for time development of calorimeter signal**
  - 8 bit transverse energy
  - 1 bit finegrain charecterization of energy deposit
- **Data presynchronized across all channels, ECAL and HCAL**

Output

- **Top 4 nonisolated electrons/photons (E_t and location)**
- **Top 4 isolated electrons/photons (E_t and location)**
- **Top 6 jets (E_t and location) & no. above threshold**
- **Total and missing transverse energy (E_t, E_x, E_y)**
- **Minimimum ionization ID and isolation bits for use with muon trigger**

Outut rate

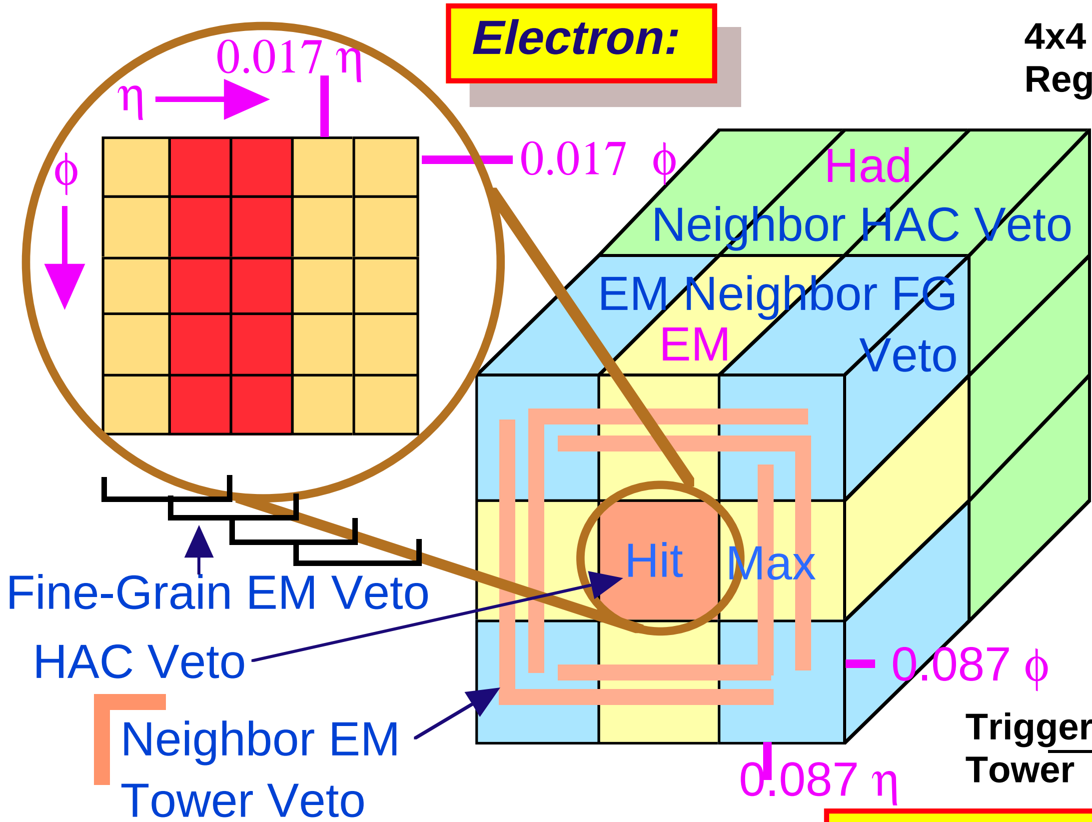
- **75/2=37.5 kHz maximum for calorimeter trigger**
- **Simulations should indicate significant safety margin - i.e., ~15 kHz rate from calorimeter trigger simulation**

Efficiency

- **Trigger should contribute no more than a few percent inefficiency for any physics channel compared to other offline analysis cuts.**
- **Trigger efficiencies should be measurable**

Calorimeter Triggers

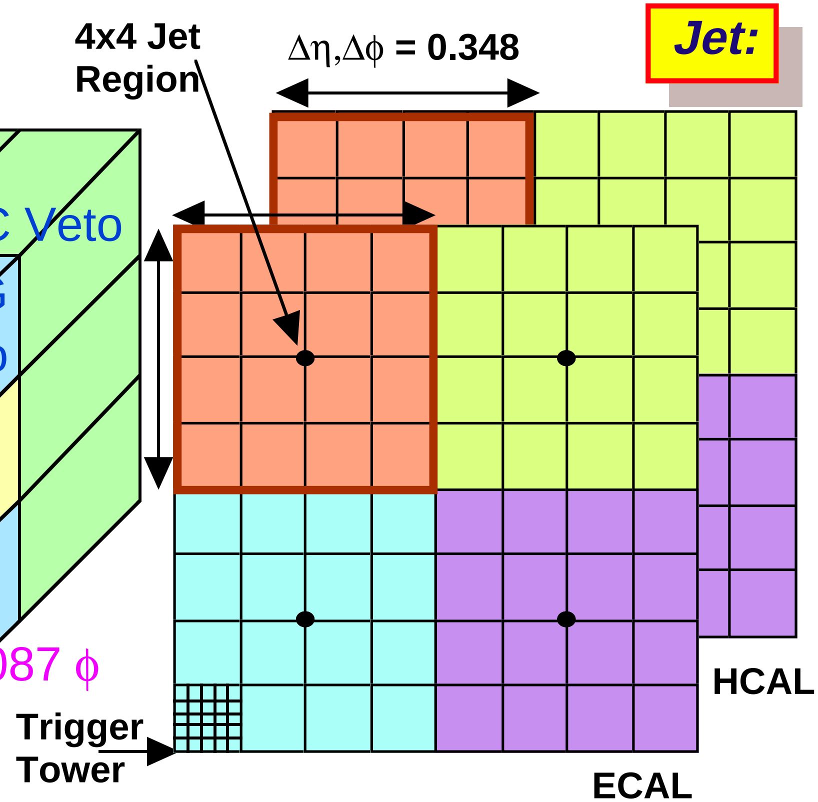
Electron:



3 x 3 sliding window centered on ECAL/HCAL trigger tower pairs

Tower count = $72\phi \times 60\eta \times 2 = 8640$

Jet:



Jet E_t from sum of ECAL& HCAL trigger tower E_t in non-overlapping 4x4 regions (also used for E_x, E_y, E_t, E_t^{Miss})

Use multijet triggers

Jet candidates are sorted to find highest energy jets

High Luminosity Cal Trigger

Luminosity = 10^{34} cm^{-2} s^{-1}

Trigger Type	Nominal		Reduced Rate	
	Trigger Et Cutoff (GeV)	Incremental Rate (kHz)	Trigger Et Cutoff (GeV)	Incremental Rate (kHz)
Sum Et	400	0.3	400	0.3
Missing Et	80	0.9	80	0.9
Electron	25	9.3	30	2.5
DiElectron	12	1.8	15	1.2
Single jet	100	1.0	100	1.0
Dijet	60	0.7	65	0.4
Trijet	30	1.3	45	0.1
Quadjet	20	1.1	25	0.5
Jet+Elctrn	50 & 12	0.3	50 & 10	0.5
Cumulative Rate (kHz)	16.7		7.4	

Process	Efficiency (%)	
	Nominal Et Cutoffs	Reduced Rate Et Cutoffs
H (80 GeV) $\rightarrow \gamma\gamma$	93	88
H (120 GeV) $\rightarrow$ Z Z $\rightarrow$ e e $\mu\mu$	76*	70*
H (200 GeV) $\rightarrow$ Z Z $\rightarrow$ e e j j	95	94
p p $\rightarrow$ t t $\rightarrow$ e X	82	77
p p $\rightarrow$ t t $\rightarrow$ H^+ X $\rightarrow$ t X	76	72

QCD Background:

CMSIM results:

Total calorimeter trigger rate at 15 kHz nominal and limited to 7.5 kHz

Signal Efficiency:

High efficiency remains for all channels with electrons and photons.

The difficult-to-trigger top decay events keep high efficiency, enabling studies of associated Higgs production.

*Inclusion of muon trigger gives full efficiency

Low luminosity Cal. Trigger

(Luminosity = 10^{33} cm^{-2} s^{-1})

Trigger Type	Nominal		Reduced Rate	
	Trigger Et Cutoff (GeV)	Incremental Rate (kHz)	Trigger Et Cutoff (GeV)	Incremental Rate (kHz)
Sum Et	150	1.0	150	1.0
Missing Et	40	1.7	50	0.7
Electron	12	9.1	20	3.4
DiElectron	7	1.9	10	1.3
Single jet	50	0.3	50	0.4
Dijet	30	0.3	35	0.1
Trijet	20	0.1	20	0.2
Quadjet	15	0.04	15	0.1
Jet+Elctrn	15 & 9	3.4	30 & 10	0.3
Cumulative Rate (kHz)	17.8		7.6	

Process	Efficiency (%)	
	Nominal Et Cutoffs	Reduced Rate Et Cutoffs
$p\,p \to t\,t \to e\,X$	98	97
$p\,p \to t\,t \to H+\,X \to t\,X$	94	94
SUSY CMS TP Scenario A (M_{LSP} = 45, M_{spart} ~ 300 GeV)	82	77
SUSY Neutral Higgs (Range of tan b and M_H values)	40 - 96	30 - 95

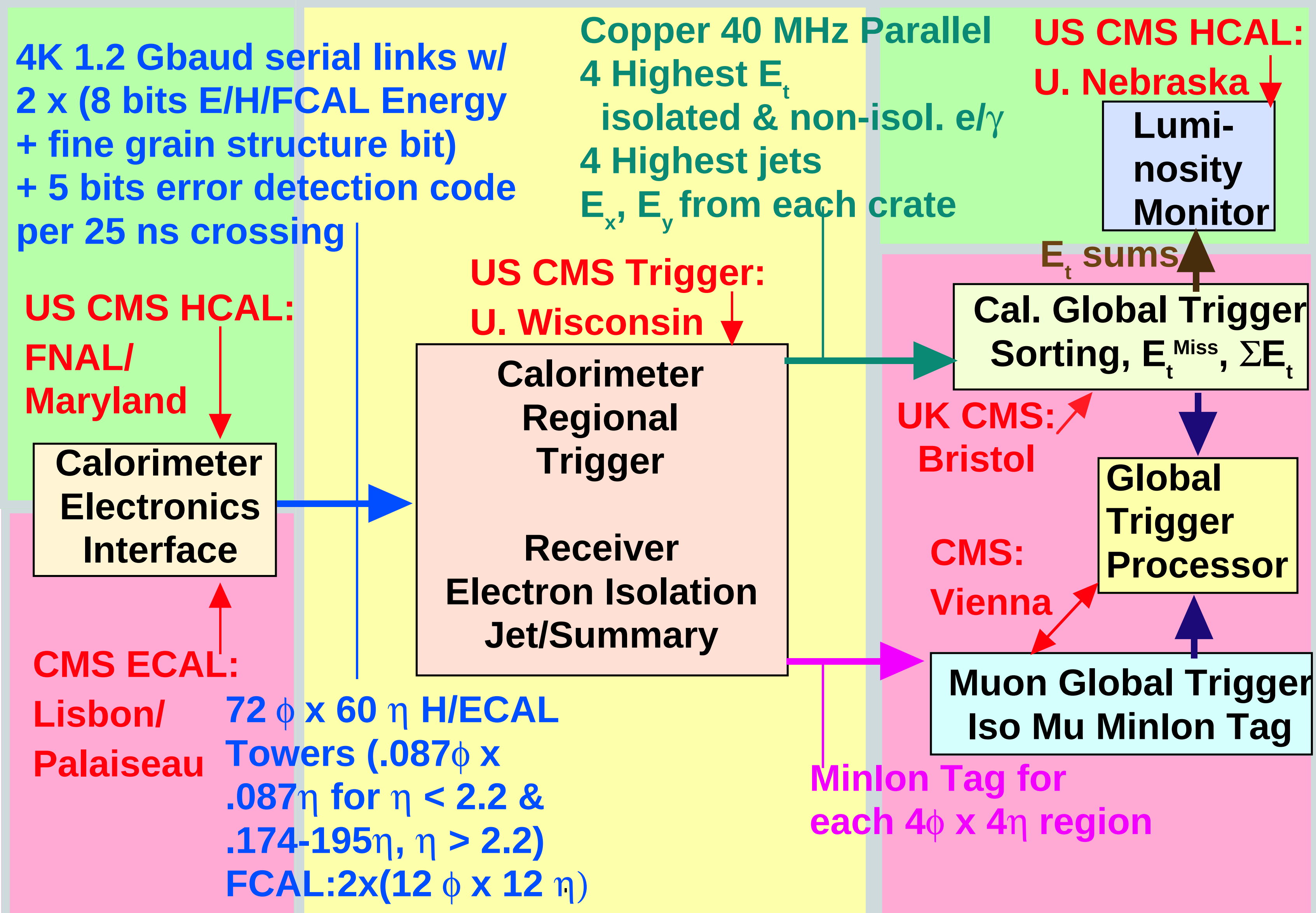
QCD Background:

CMSIM results:
Total calorimeter trigger rate at 15 kHz nominal and limited to 7.5 kHz

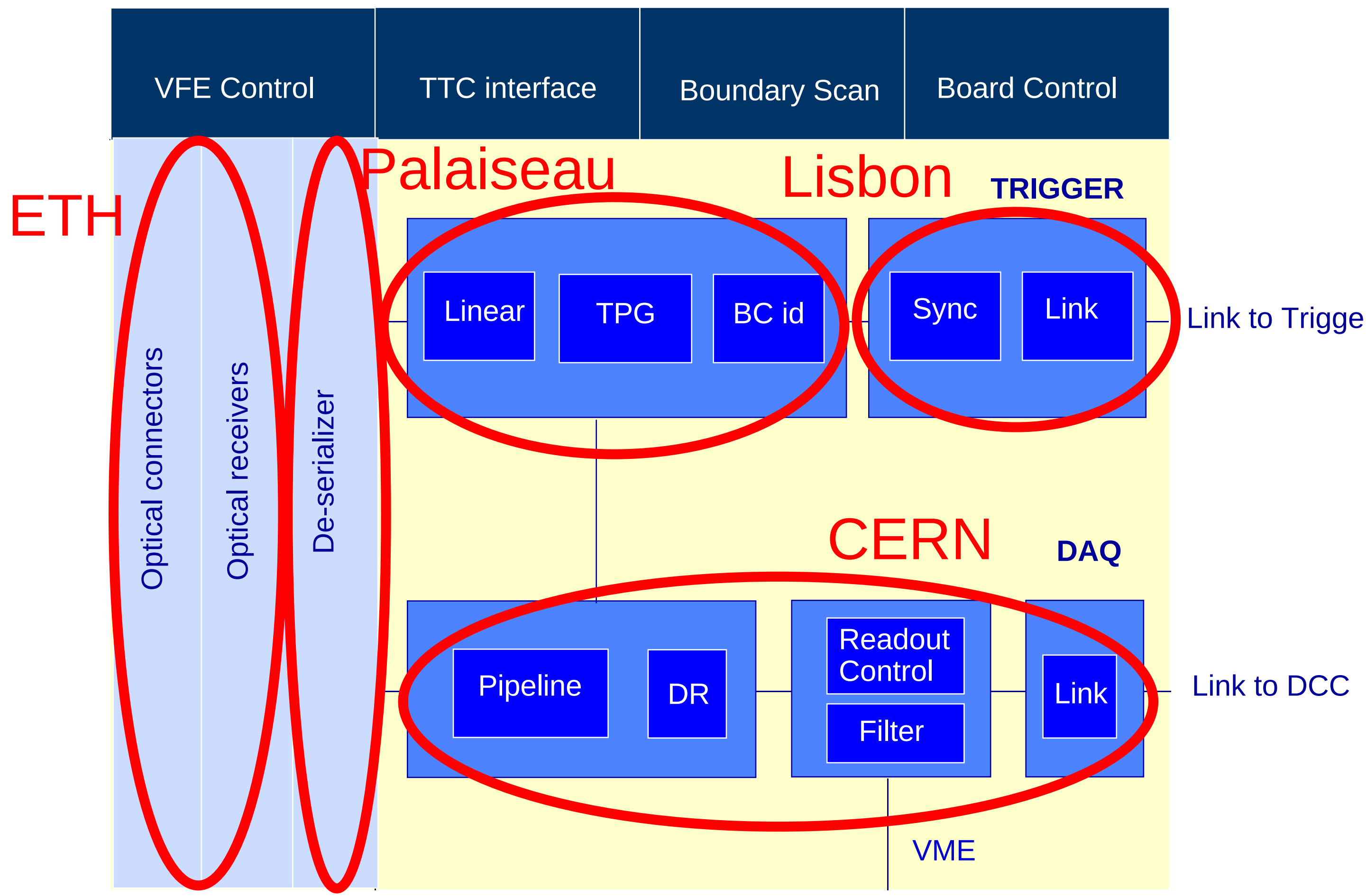
Signal efficiency
High efficiency remains for the benchmark processes involving top decays and SUSY sparticles.

Note:
There is also high rate of B signal in level-1 sample.

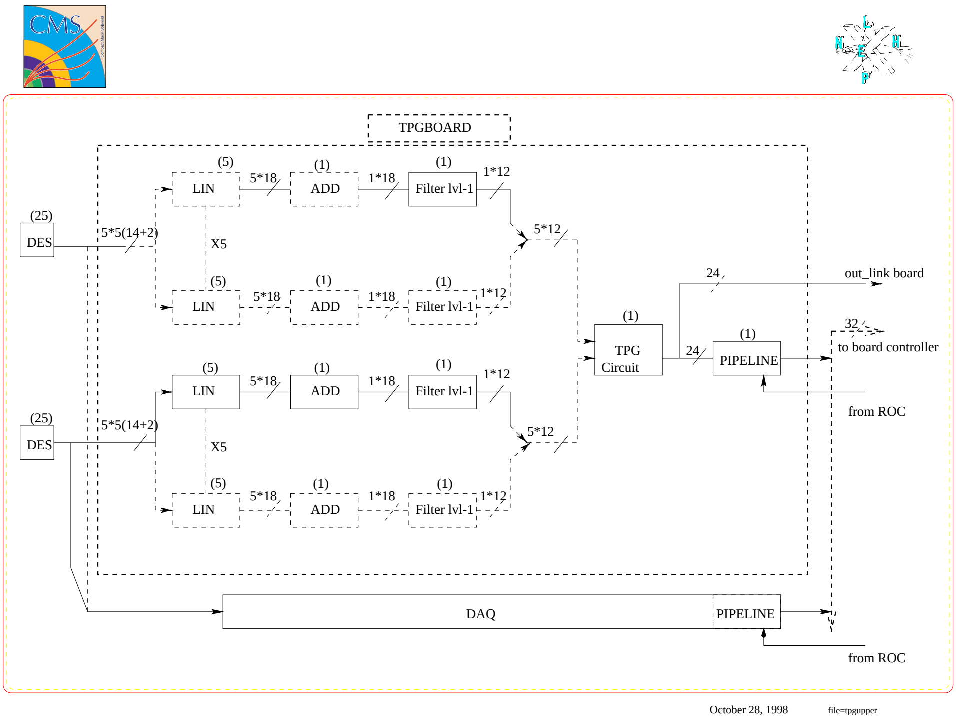
Calorimeter Trigger Overview



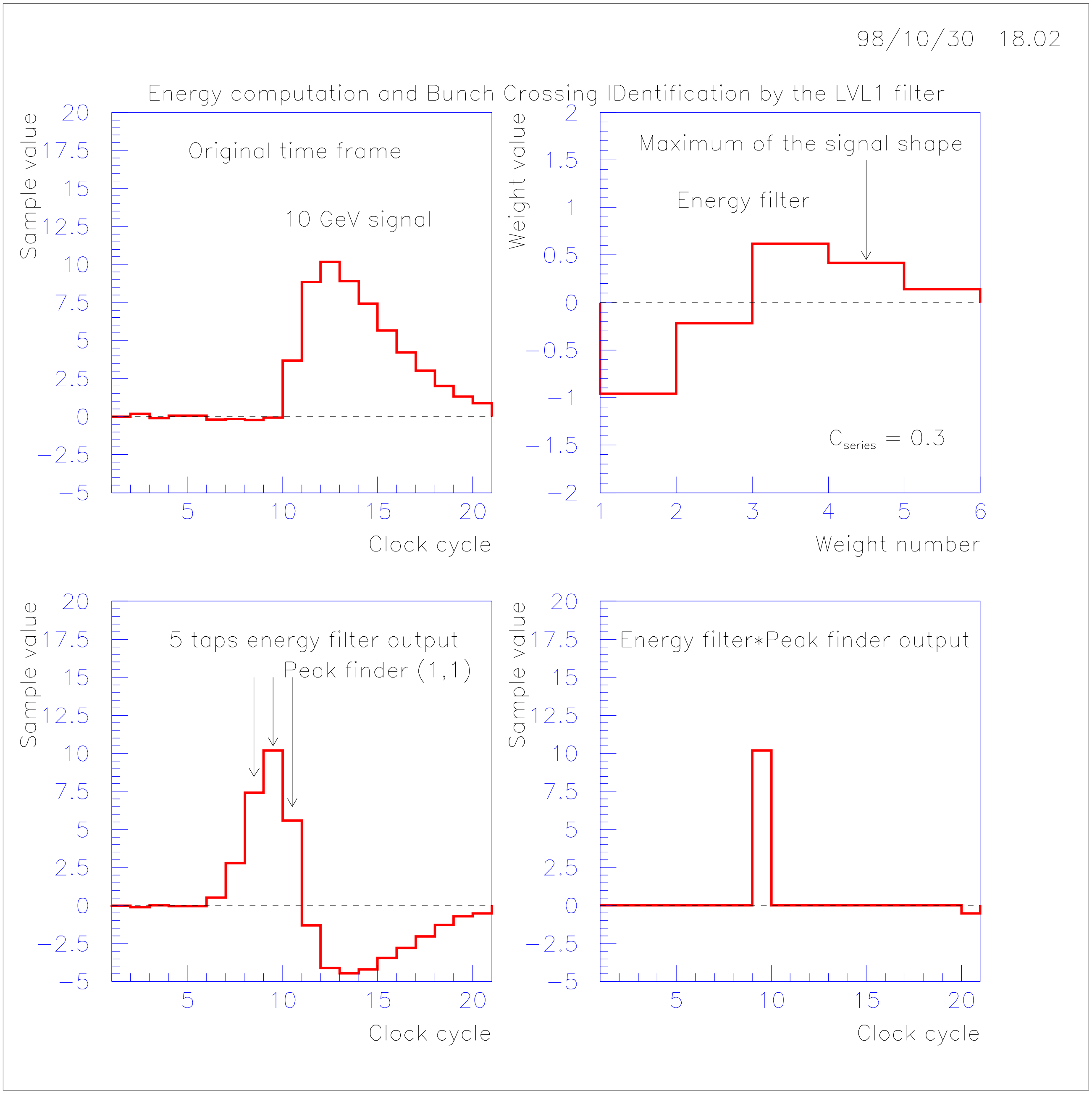
ECAL ULR&T CARD



The TPG Board Architecture



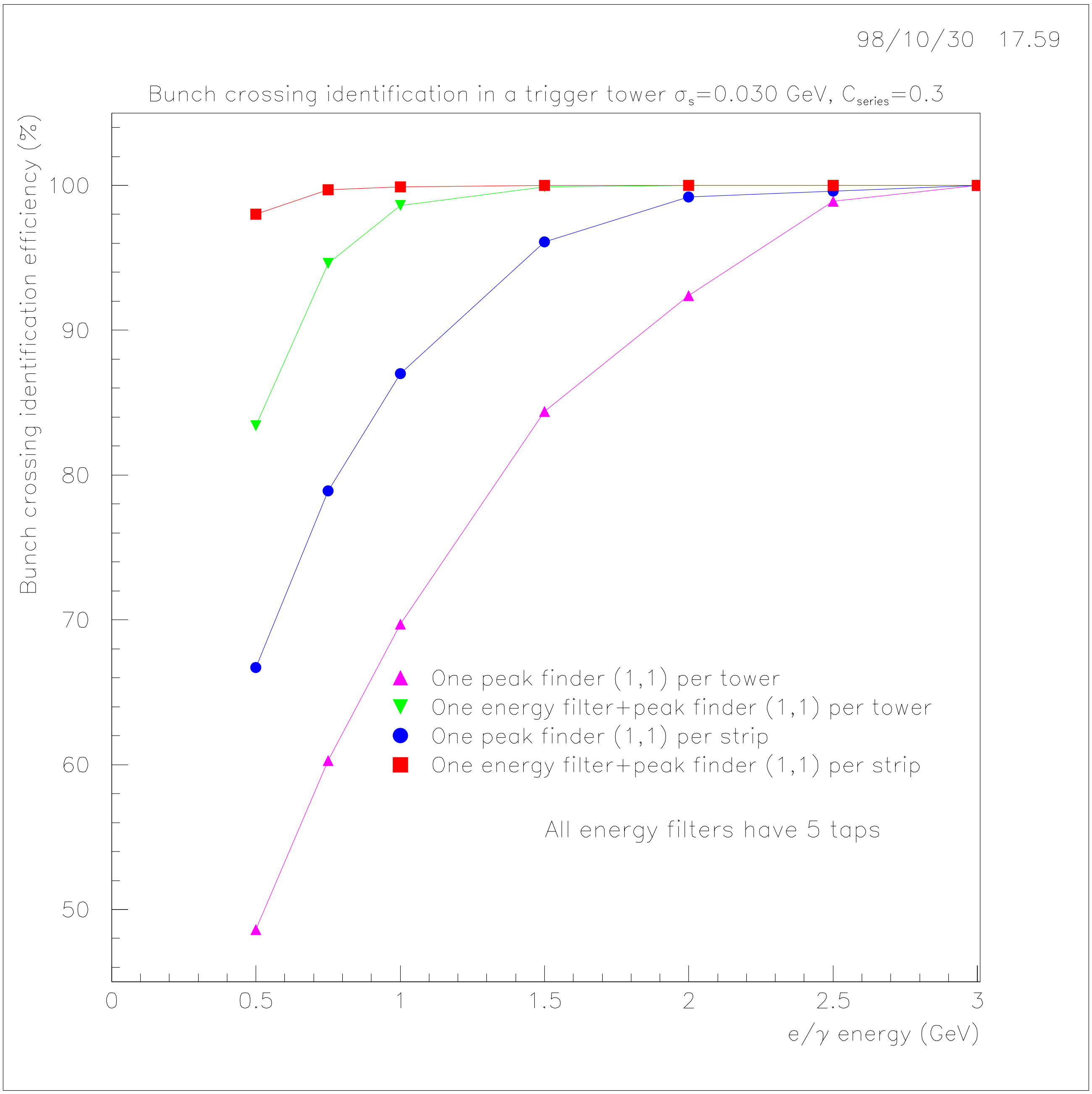
- LINEARIZER: transform non linear scale from VFE to transverse energy scale
- ADDER: build strip signals
- LVL1 filter: perform the LVL1 filter computations on each strip signal
- TPG: extract the trigger primitives (E_T^{tot} and CSB) for each trigger tower
- PIPELINE: store the trigger primitives for DAQ



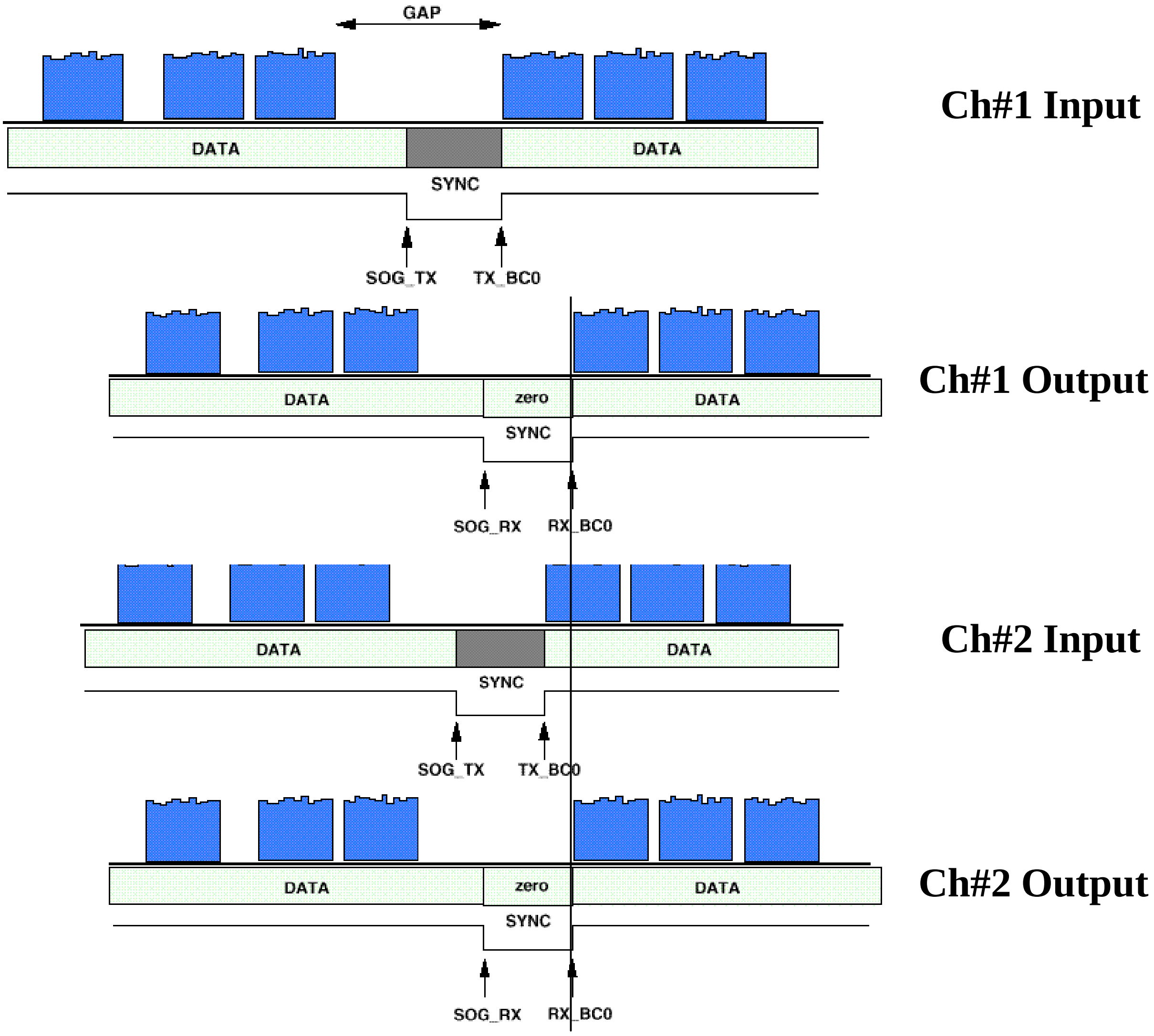
98/10/30 18.02
Energy computation and Bunch Crossing IDentification by the LVL1 filter
Original time frame
10 GeV signal
Sample value
Clock cycle
Maximum of the signal shape
Energy filter
$C_{series} = 0.3$
Weight value
Weight number
5 taps energy filter output
Peak finder (1,1)
Sample value
Clock cycle
Energy filter*Peak finder output
Sample value
Clock cycle

BCID for benchmark e/γ showers

$$\epsilon^{BCID} = \frac{Nb\ of\ events\ with\ a\ peak\ for\ the\ right\ BC\ in\ a\ strip}{Nb\ of\ events}$$

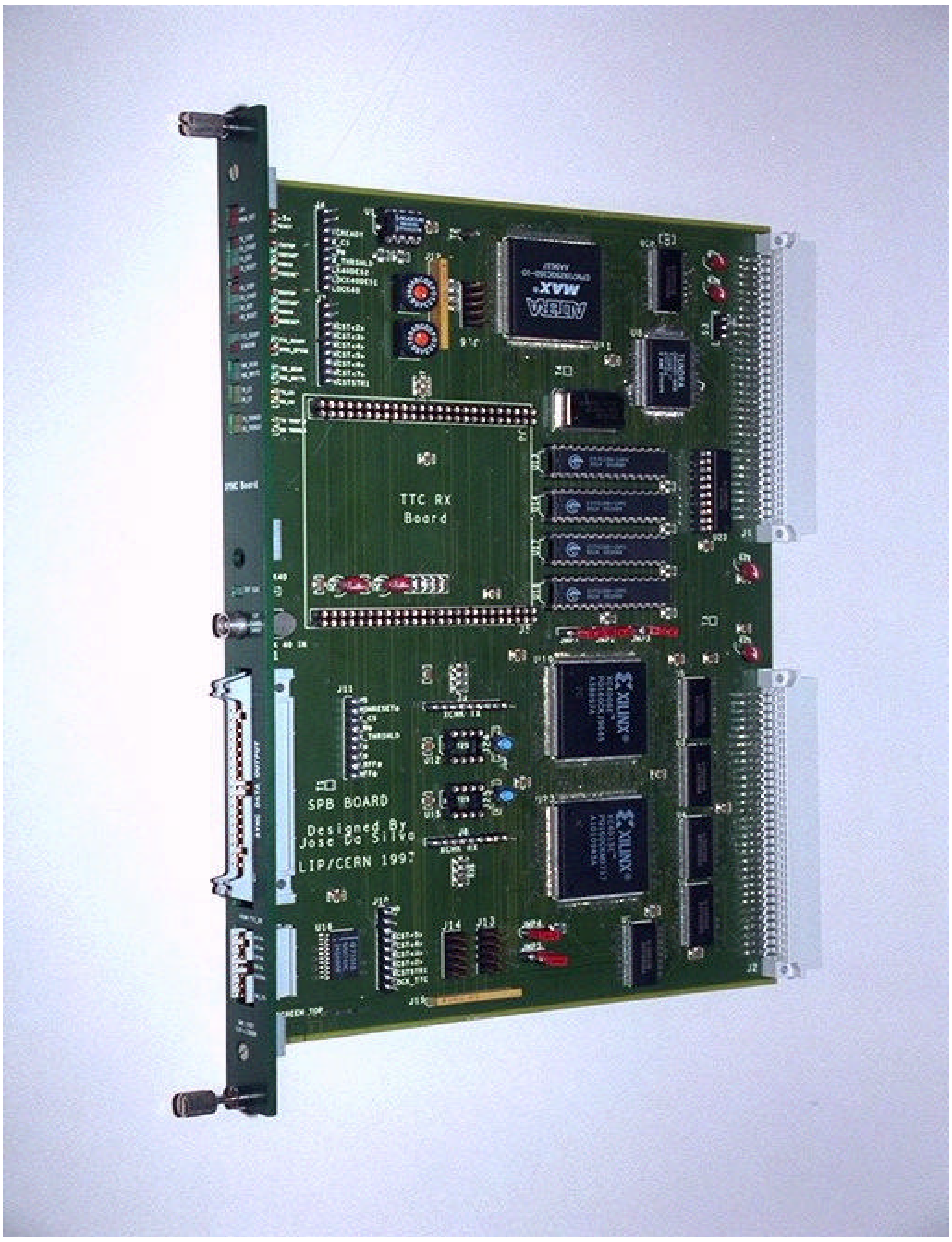


Sync FIFO

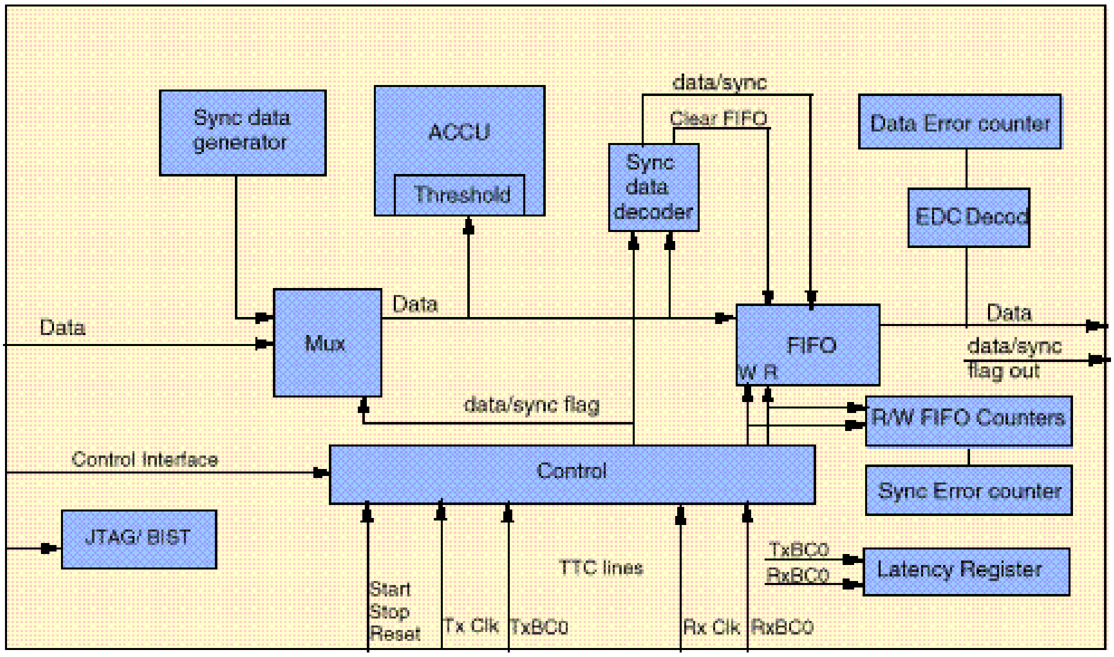


- **2 Input Channels with time difference and same Output Timing**

Sync Tester Board



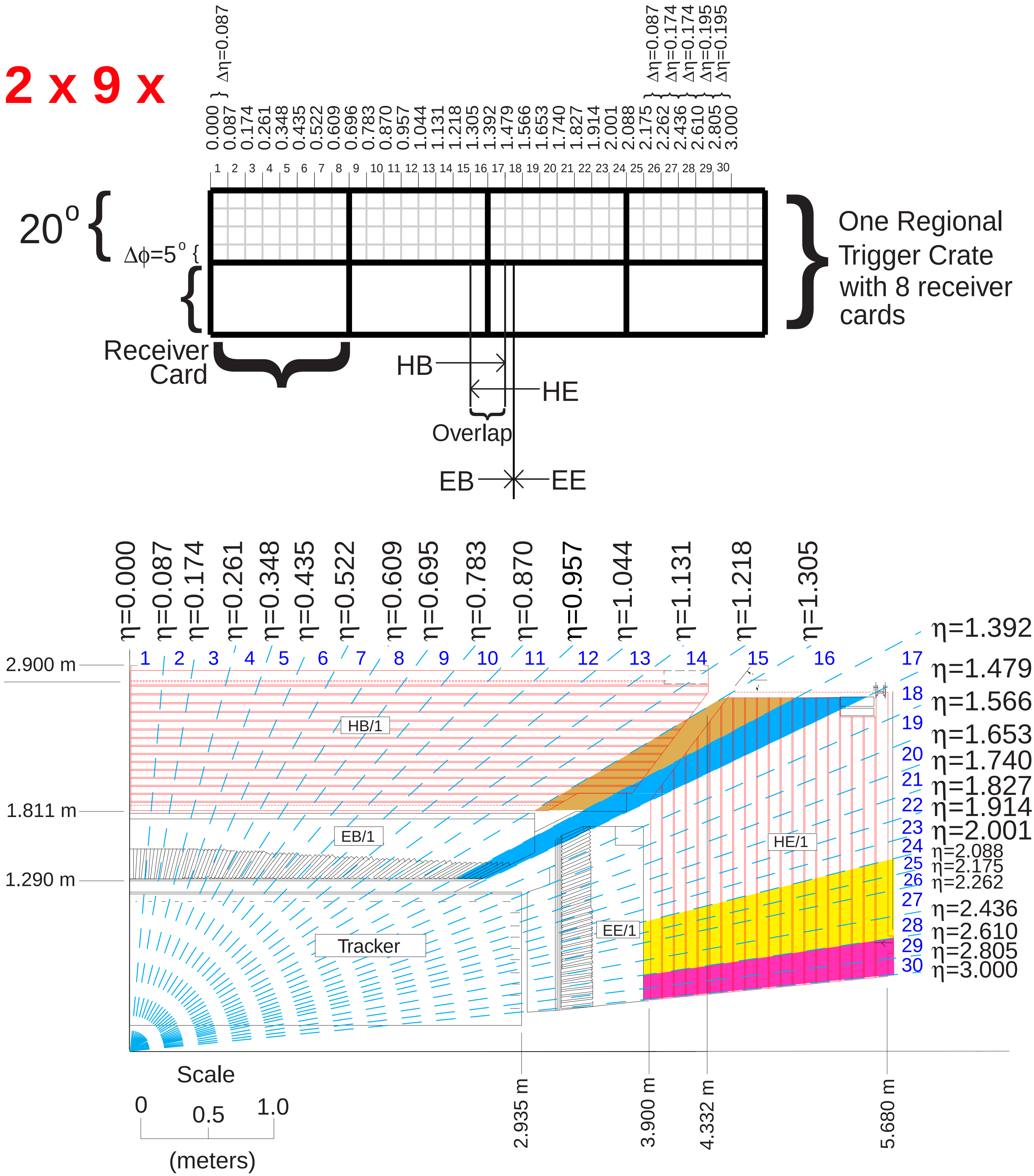
Sync Block Diagram



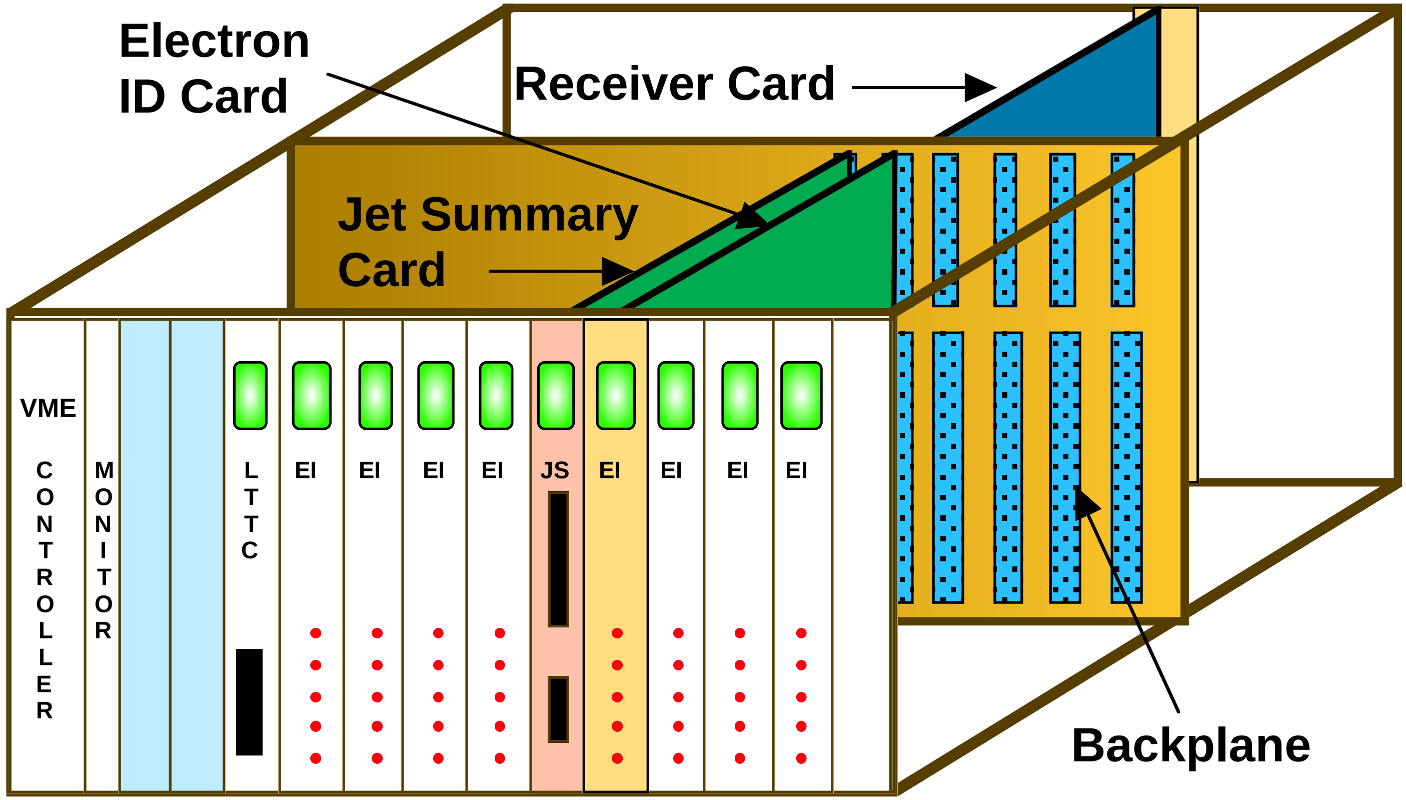
Differences from previous design:

- Merge of the 2 circuits.
- TTC Control Signals decoded on the BC.
- Internal Accumulator.
- FIFO Transparent Mode with programmable depth.
- Latency Register (Tx_BC0 > Rx_BC0 distance).
- BIST.

Calorimeter Trigger Towers



Regional Calorimeter Crate



19 X
(18 E/HCAL +1 FCAL)

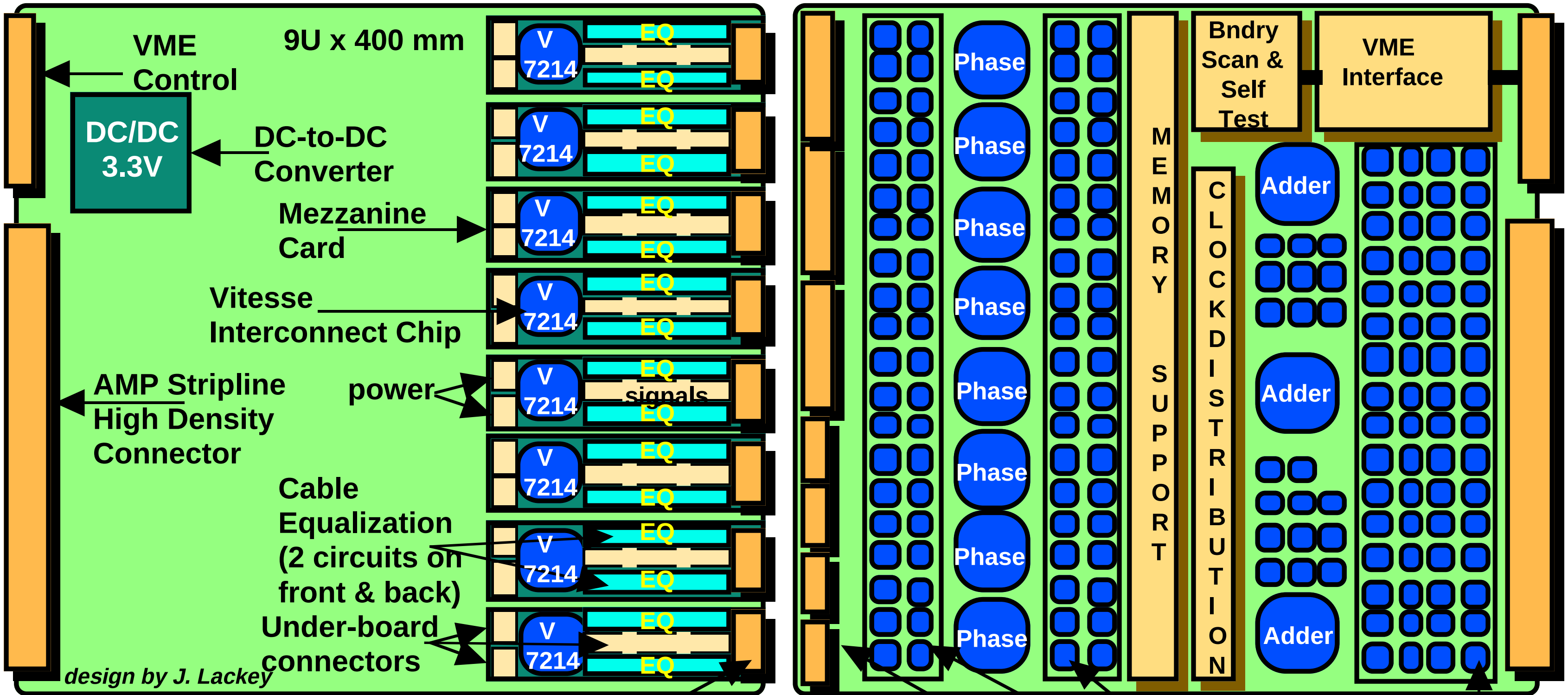
Data from calorimeter FE on Cu links @ 1.2 Gbaud

- Into 152 rear-mounted Receiver Cards

160 MHz point to point backplane

- 19 Clock&Control, 152 Electron Identification, 19 Jet/Summary, Receiver Cards operate @ 160 MHz

Receiver Card



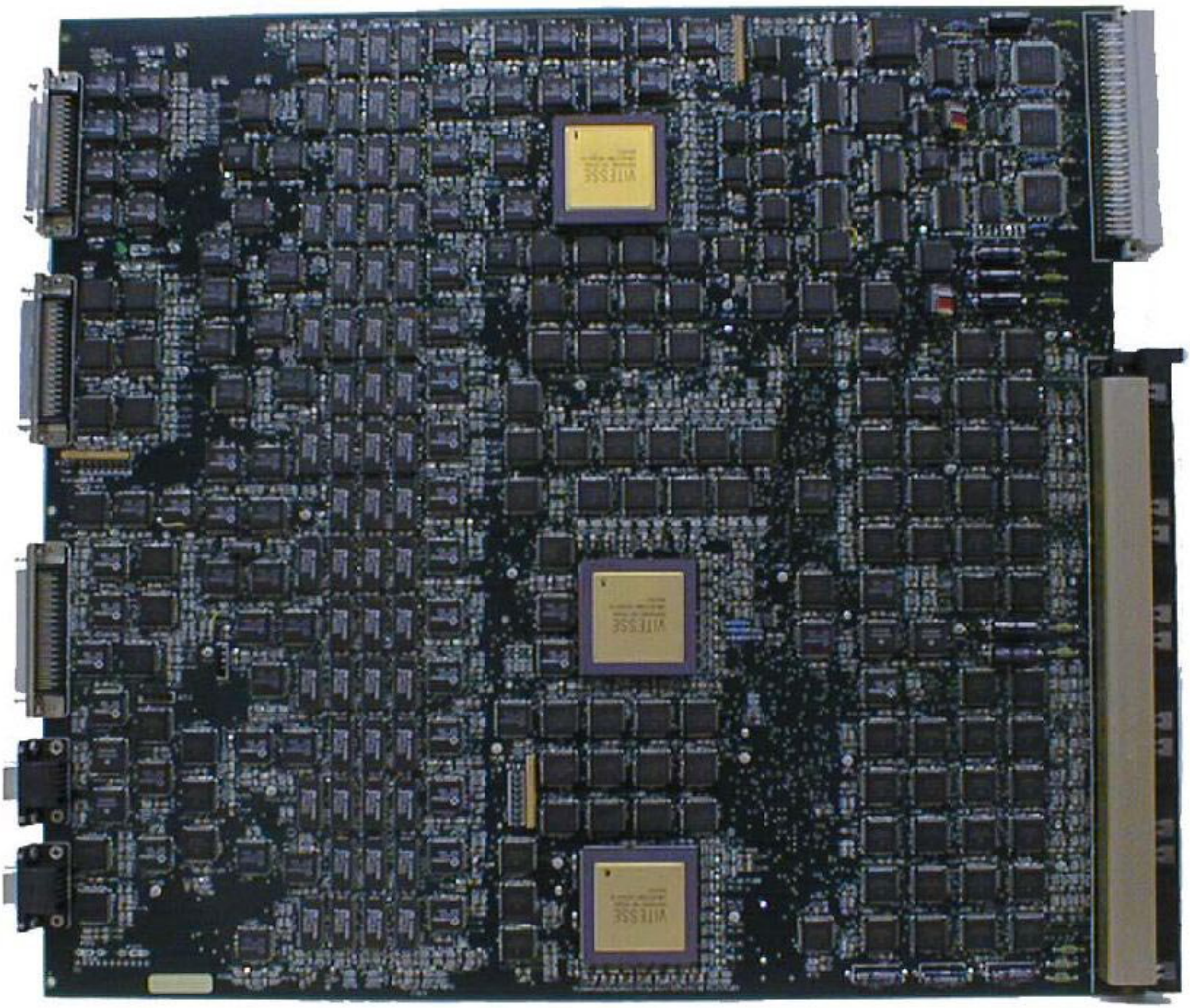
Rear:
32 Channels =
4 Ch. x 8 mezzanine cards
1.2 GBaud copper rcvrs
18 bit (2x9) data + 5 bit error
Vitesse Chip:
Converts Serial to Parallel

Front: Data from Rear @ 120 MHz TTL
Phase ASIC: Deskew,Mux @ 160MHz
Error bit for each 4x4, Test Vectors
Memory LUT @ 160 MHz
Adder ASIC:
8 inputs @ 160 MHz in 25 ns.
Differential Output@160 MHz

Receiver Card Prototype

160 MHz Prototype Card Under Test:

- VME Interface working
- Adder ASIC's functioning
- Detailed timing under study



8 x 13-bit 160 MHz Adder ASIC

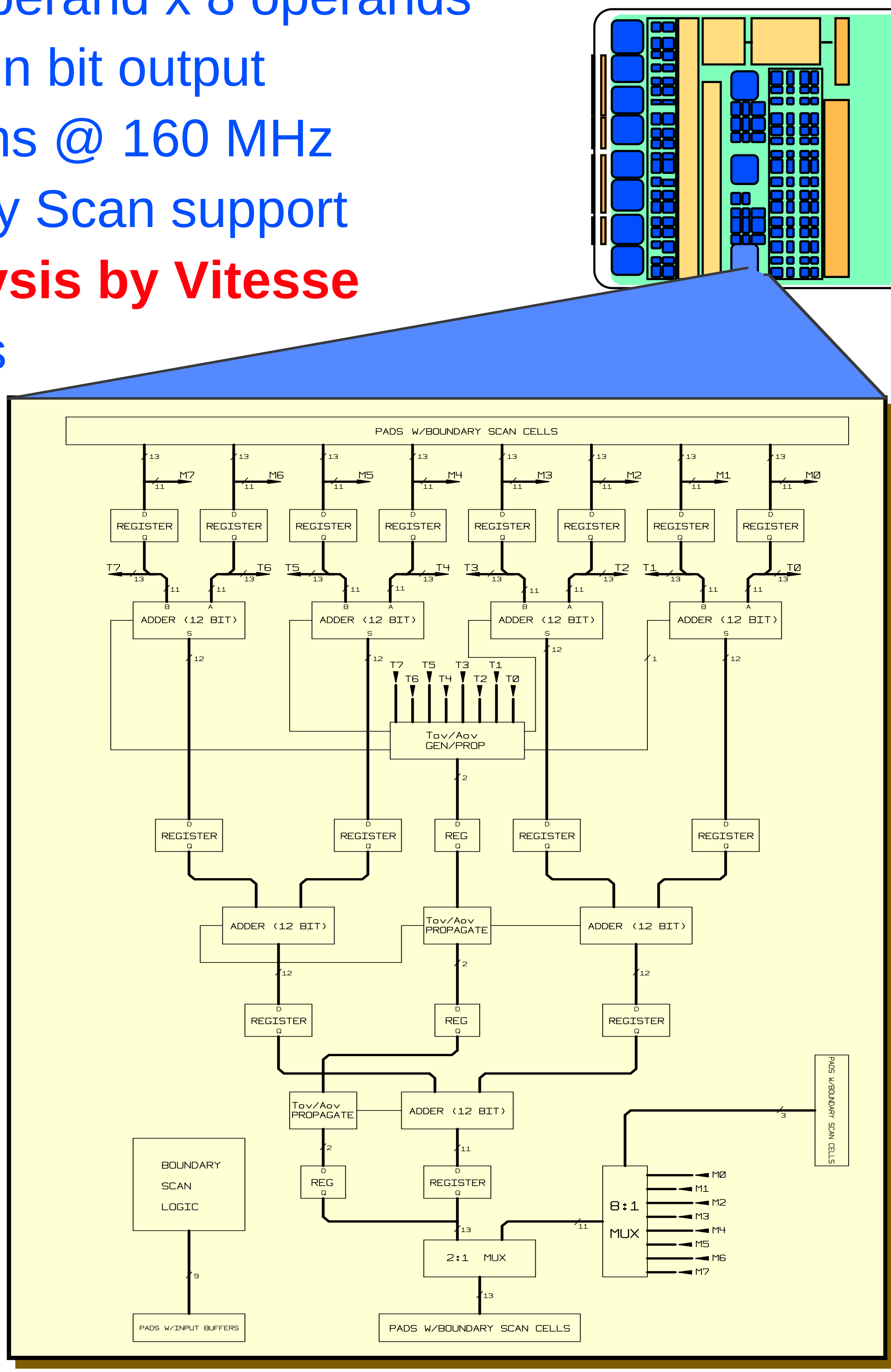
Vitesse 0.6µ H-GaAs Process: ECL I/O

- 13 bits per operand x 8 operands
- Single thirteen bit output
- Latency: 25 ns @ 160 MHz
- Full Boundary Scan support

Technical analysis by Vitesse

- ~11,000 cells
- 4 Watts
- 308 MHz

Receiver Card:



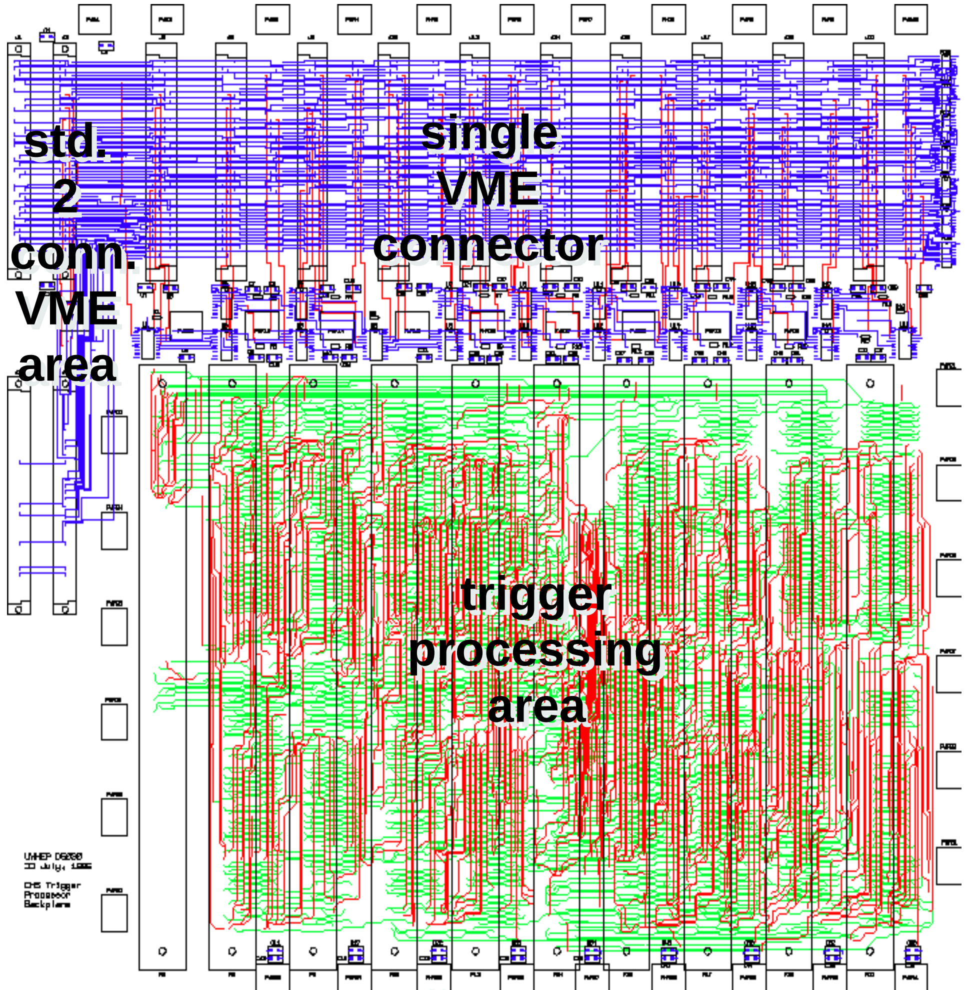
Status:

- 5 tested devices delivered
- select nets exceed simulation speed by 10%

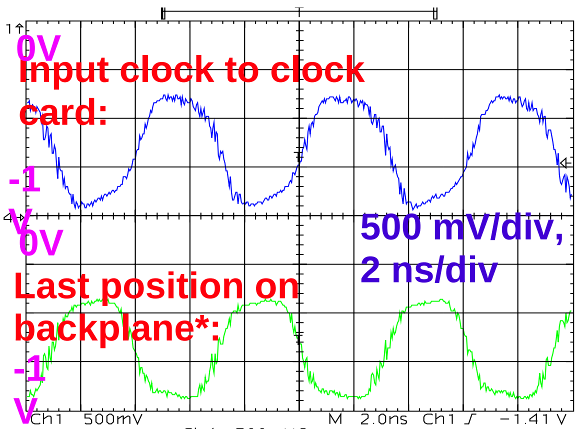
- J. Lackey

160 MHz Backplane

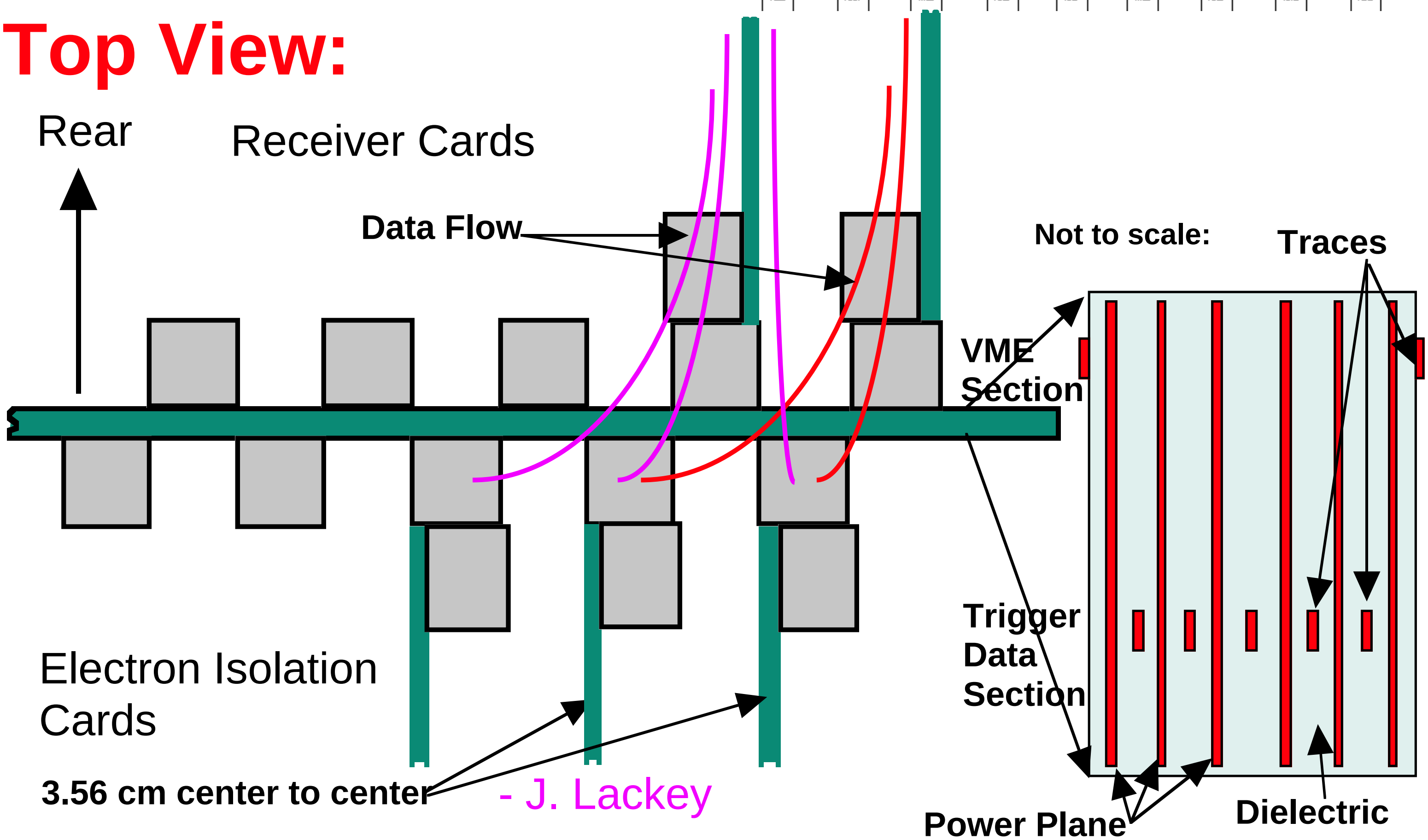
Display 3 of 6 signal layers:



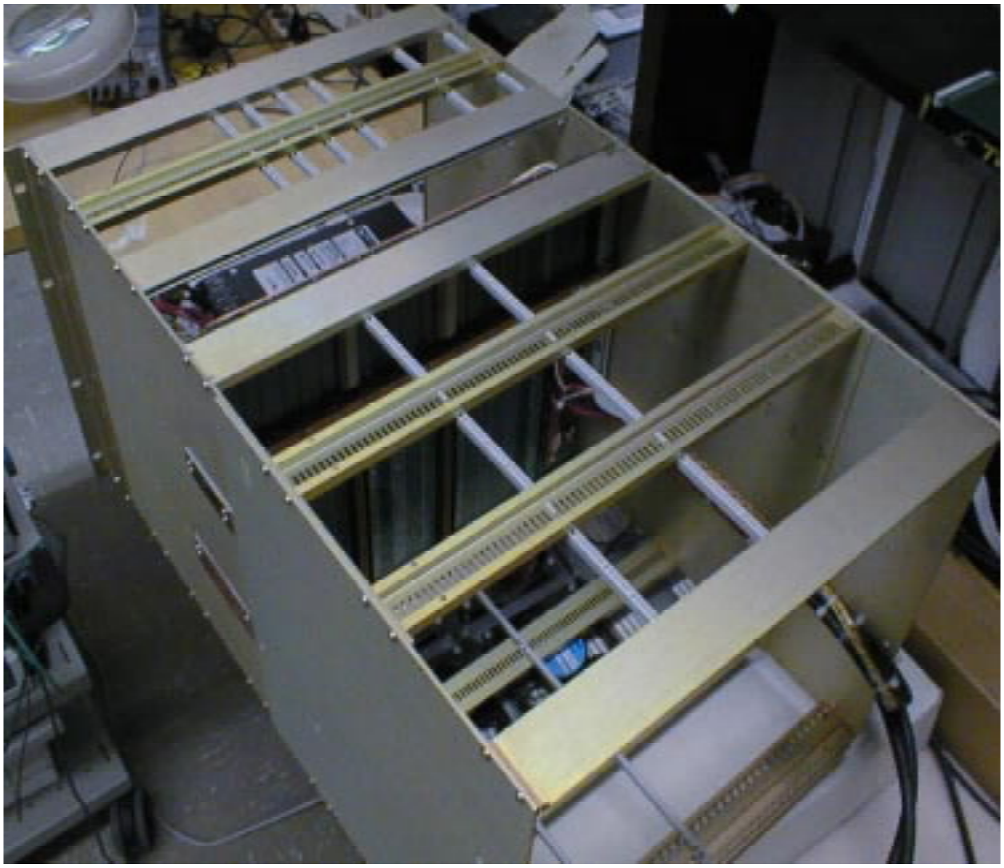
Signal performance: rise < 1 ns:



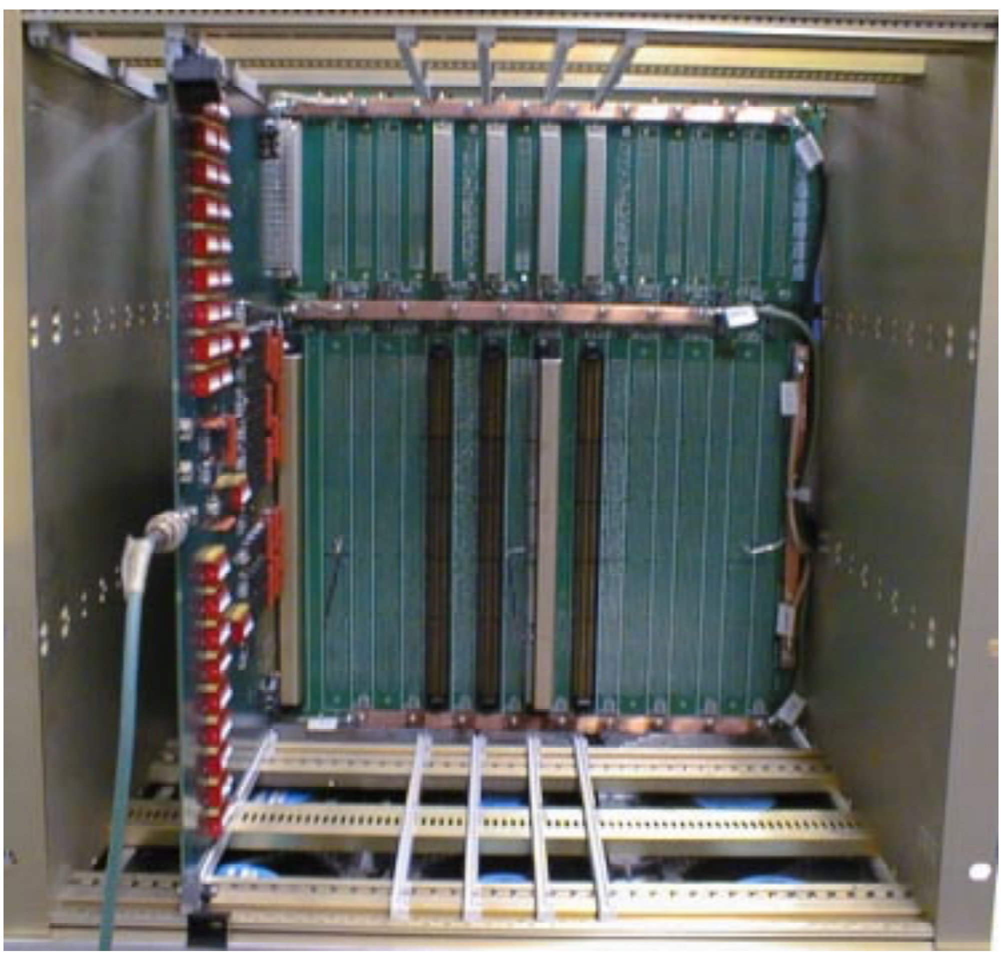
Top View:



Backplane Test Setup

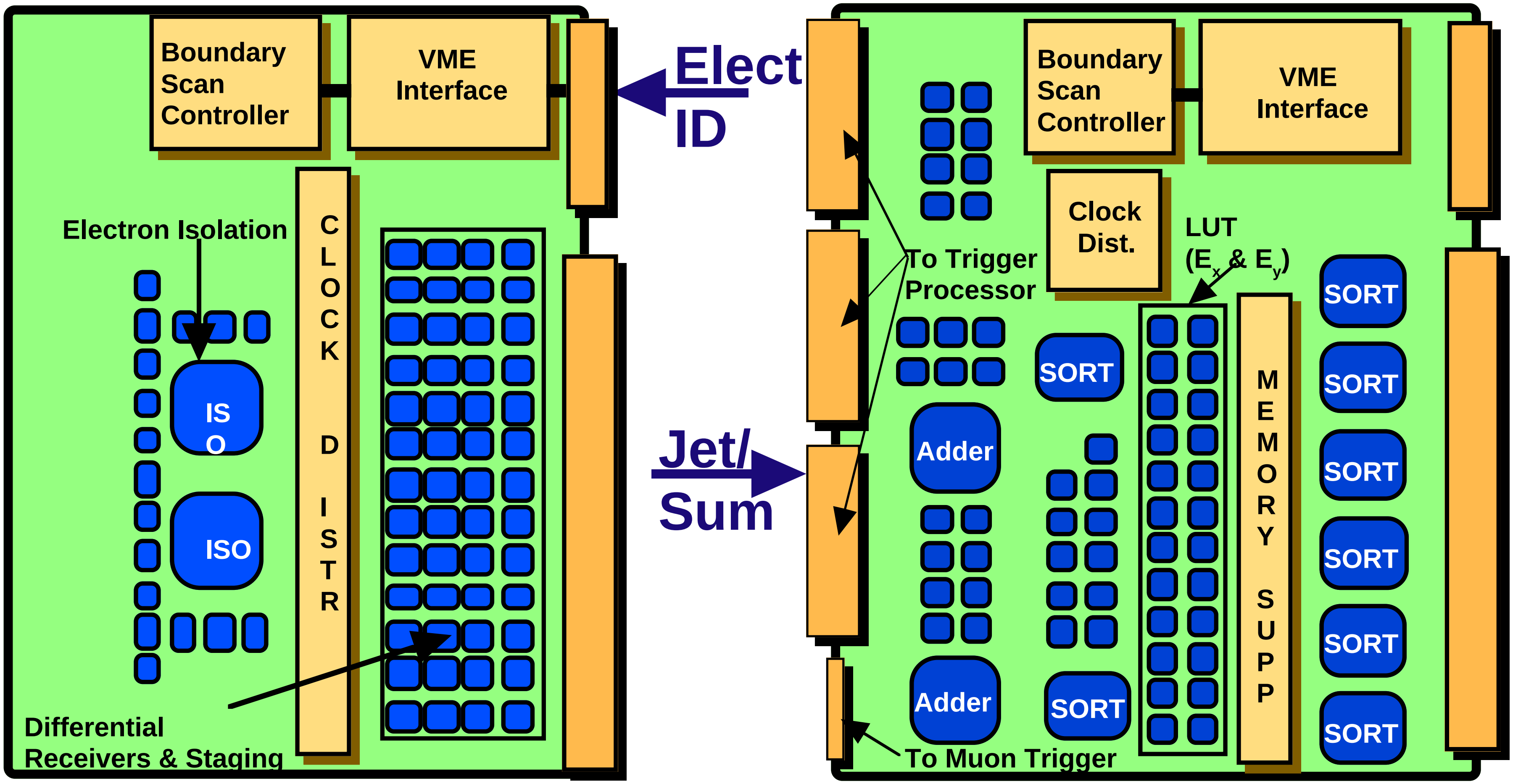


Top rear view of crate & backplane with power supplies



Front view of crate & backplane with clock board installed

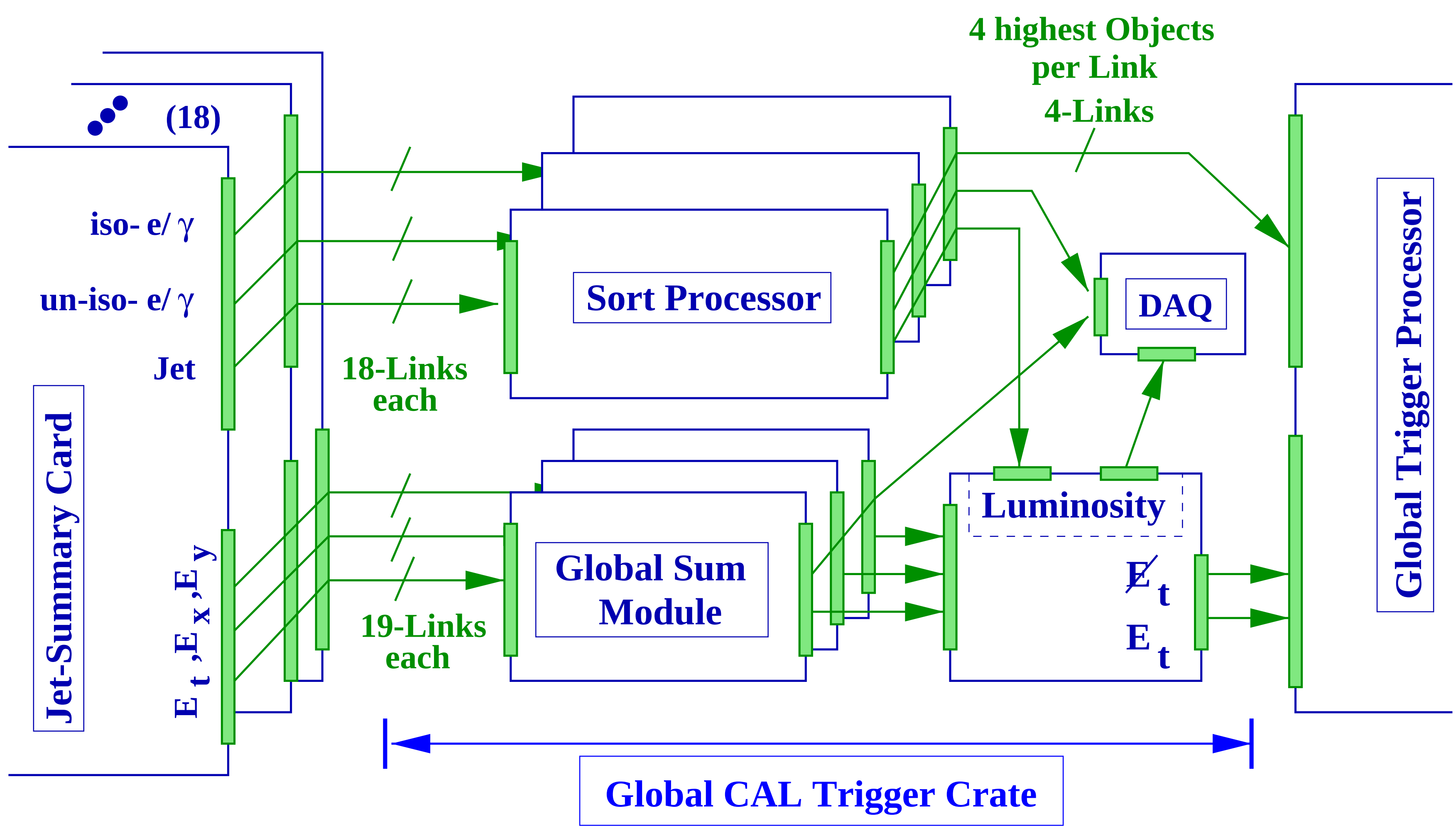
Electron ID & Jet/Summary Cards



Processes 4x8 region @ 160 MHz
Electron isolation on ASIC
Lookup tables for ranking
Takes Max in each 4x4

Summarizes full crate:
Sorts 32 e's,4x4 E_t Æ top 4 e's, jets
LUTs: E_x & E_y from E_t for 4x4 area
Adder tree for E_t, E_x and E_y sums
Quiet/MinI bits for each 4x4 region

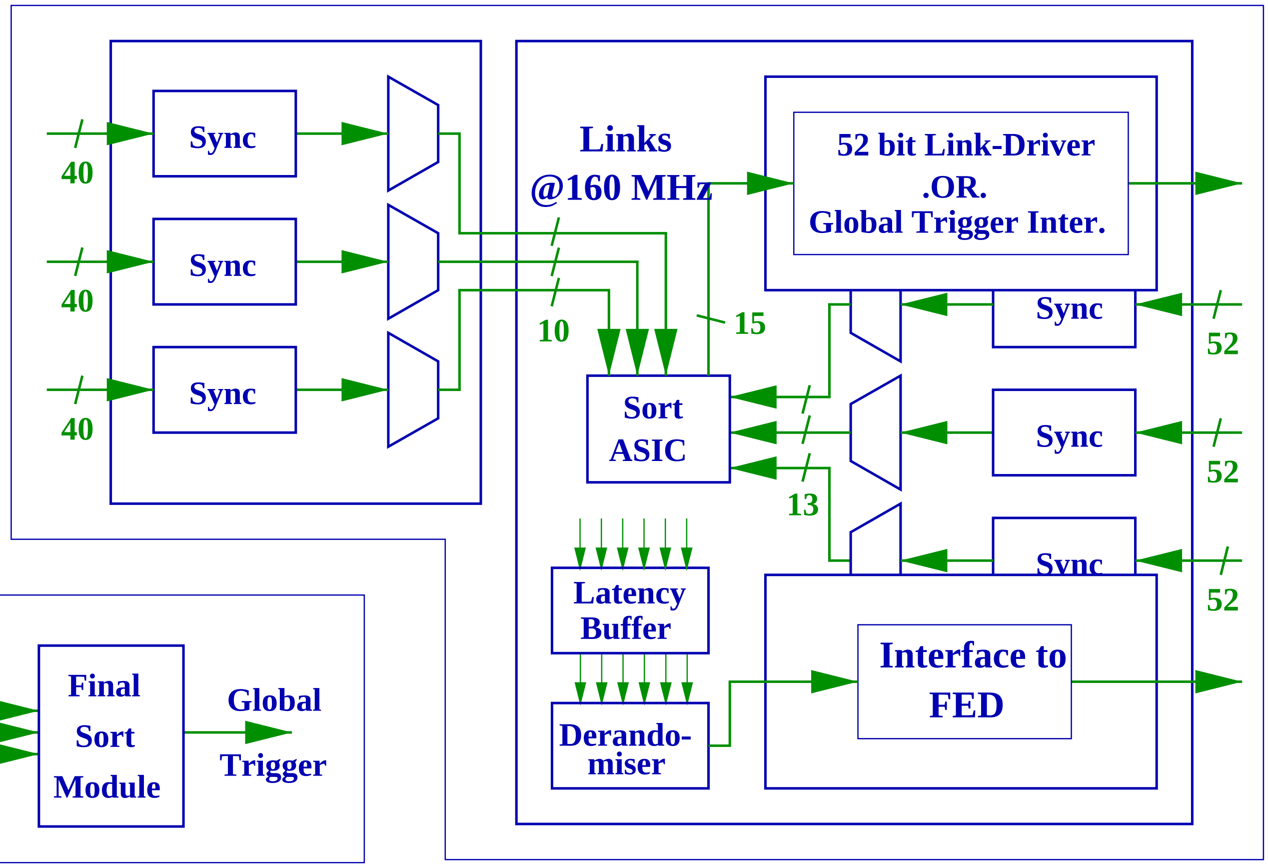
Global Kalorimeter Trigger Blockdiagramm

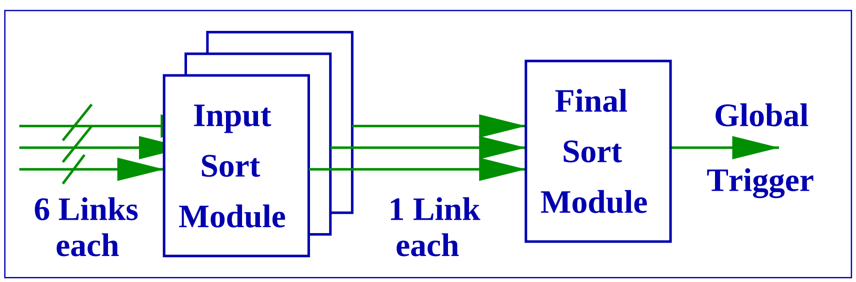


Sort-Processor

- **Rear Receiver Board**

  for Input Sort Module
- **use Mezzanine Cards**
  - **Input Sort to Final Sort**
  - **Final Sort to Global Tr.**
  - **Sort to FED**
- **Readout of all input data**





The Sort-ASIC

- use SORT ASIC on all sort levels

  Configurable: (6 bit rank)

  a) 4 Links; unsorted no location Id

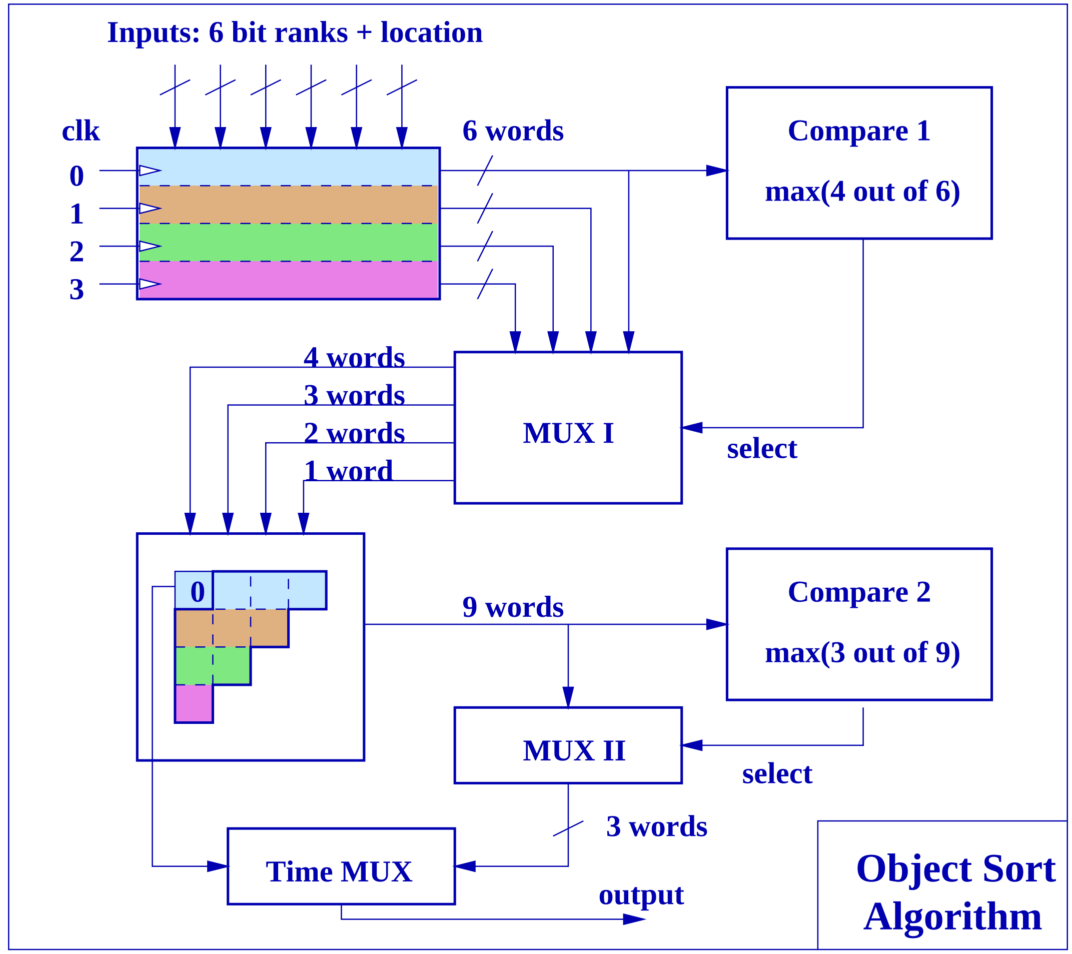
  b) 6 Links; sorted 4 bit location Id

  c) 3 Links; sorted 7 bit location Id

- Pre Sort for 1. level
- Input/Output data ECL @160MHz
- Boundary Scan
- Latency: 50 nsec (2 BC)

Further Options:

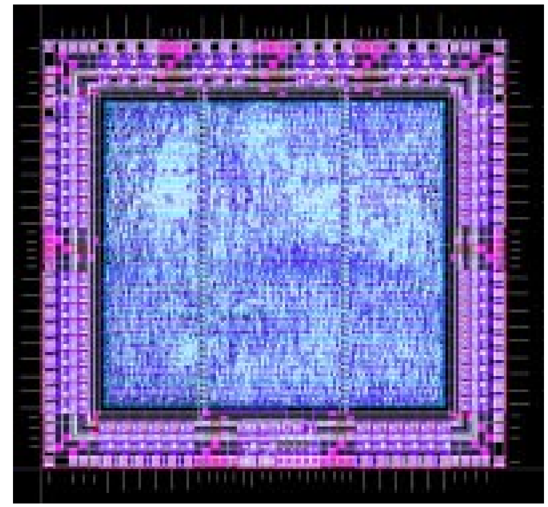
- count objcts above energy threshold
- energy sums above threshold (Jets)



Object Sort Algorithm

GCT Demonstrator Project

- **Design of Prototype Sort ASIC (manufactured 1997)**
  - Object Sort for (32 -> 4)
  - 4 Inputs (8 bit rank, 3 bit location Id) @160MHz
  - ECL I/O (Boundary Scan)
  - Schematic design
  - Funtion successfully tested @50MHz



- **160 MHz Sort ASIC Test System**
  - Sort ASIC Test Module: 4 random pattern generator + Sort Asic
    + (160MHz -> 40MHz) DeMUX + 160MHz clk generator (RAL)
  - 64 bit ECL Data Recorder/Source, Readout via custom fieldbus (Bristol)

All hardware available, Test currently in progress

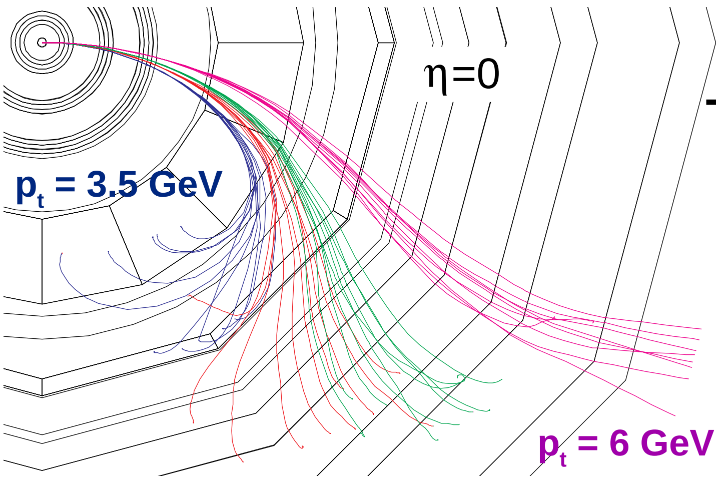
Tasks of the CMS Muon Trigger:

- muon identification
- transverse momentum measurement
- bunch crossing identification

Basic requirements:

- Geometrical coverage: up to $|\eta|=2.4$
- Latency: < 3.2 μs
- Trigger dead time: not allowed
- Maximal output rate: < 15 kHz for luminosities < 10^{34} $s^{-1}cm^{-2}$
- Background rejection: trigger rate due to background should not exceed the rate of prompt muons from heavy quark decays
- Low p_t reach: should be limited only by muon energy loss in the calorimeters
- The highest possible p_t cut: ~50-100 GeV
- Isolation: transverse energy E_t deposited in each calorimeter region of $\Delta\phi \times \Delta\eta = 0.35 \times 0.35$ around a muon is compared with a threshold
- Output to the Global Trigger: up to 4 highest p_t muons in each event

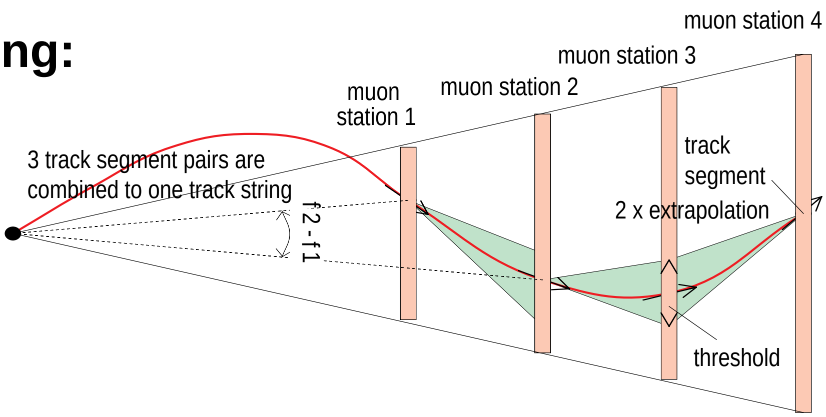
Muon trigger system



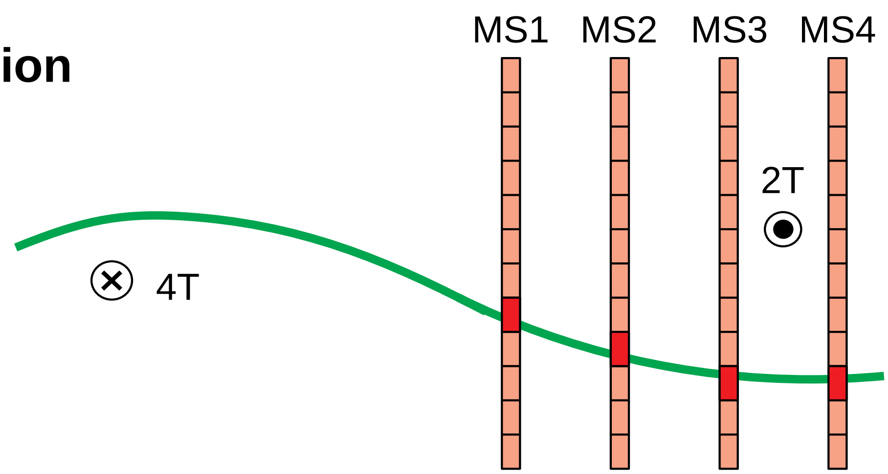
The CMS muon trigger is based on:

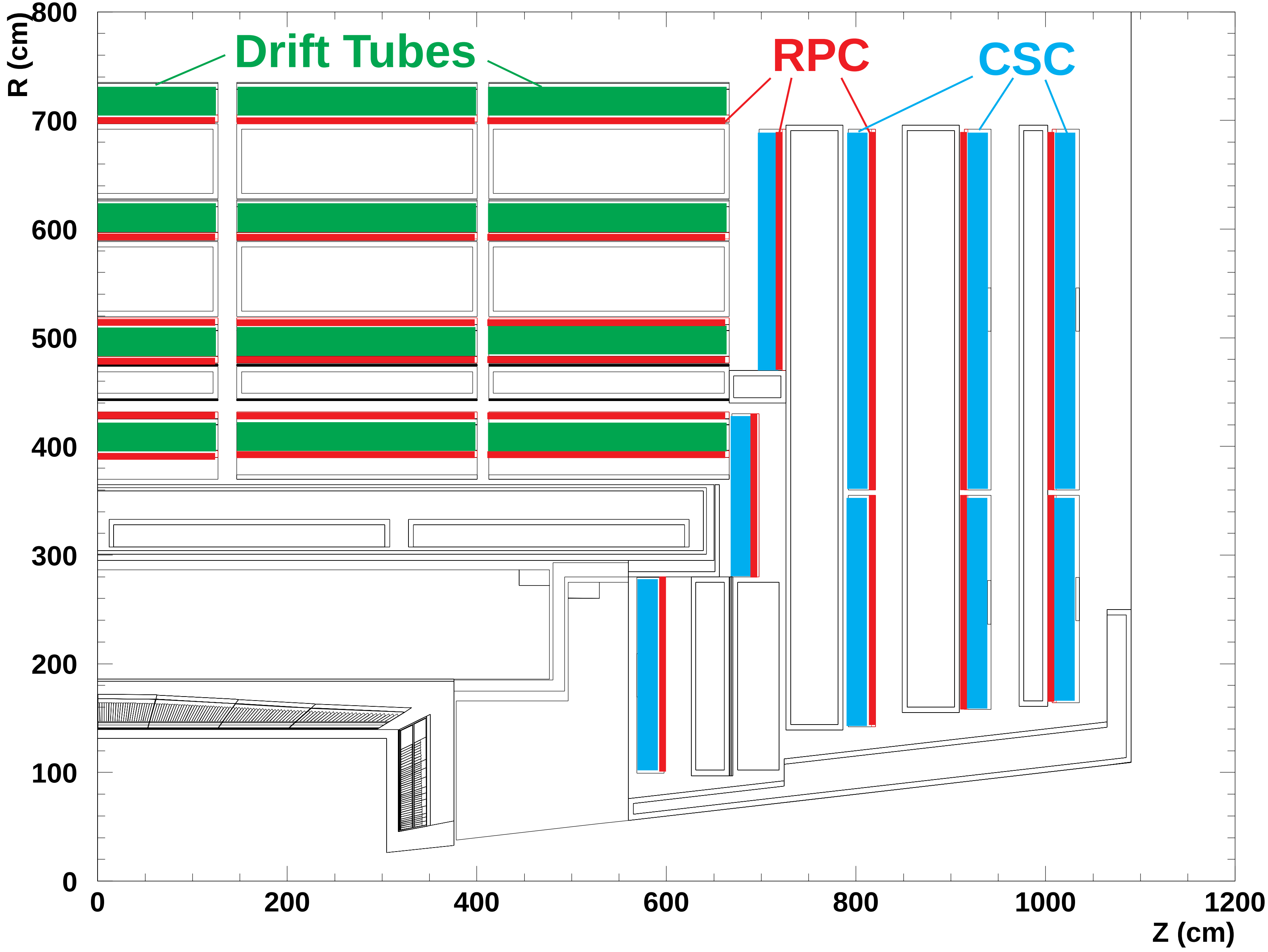
1) Dedicated trigger detector (Resistive Plate Chamber)
2) Muon chambers (Drift Tubes, Cathode Strip Chambers)

DT and CSC track finding:
- combines vectors
- forms a track
- assigns p_t value



RPC pattern recognition
- pattern catalog
- fast logic





Drift Tubes
RPC
CSC
R (cm)
800
700
600
500
400
300
200
100
0
0
200
400
600
800
1000
1200
Z (cm)

Muon Trigger Summary - I

RPCs (barrel & endcap)

- $|\eta| < 2.1$, strips of $\Delta\eta \times \Delta\phi = 0.1 \times 5/16°$
- 4 RPC stations compared to templates for different p_T ranges by Pattern Comparator ASICs
- 144 ϕ segments/ring; 38 ring processors

Drift Tubes (barrel)

- 2 ϕ, 1 z superlayers/stations (no z in station 4)
- 6 rings ($\Delta\eta = 0.35$) of 12 ϕ segments
- Bunch & Track Identifier forms superlayer r-ϕ vectors by solving linear equations
- Track Correlator combines two ϕ superlayers to form a vector for each station
- Trigger Server sorts vectors by quality & p_T and outputs 2 highest p_T segments to Track Finder

CSCs (endcaps)

- 6-layer CSC/station for 3 (upgrade to 4?) stations
- Fast-shaped radial-strip pulses fed to Local Charged Track processor to find coincidence in $\geq$ 4 out of 6 layers inside predefined roads
- Coincidence made with perpendicular anode wires to identify crossing
- Vector from each station sent to Track Finder

Muon Trigger Summary - II

Drift Tube Track Finder

- Accepts DT segments from Trigger Server
- Accepts Segments from CSC Trigger in low $|\eta|$ barrel/endcap overlap region
- Combines track segments into full tracks
- Assigns p_T and quality to each track

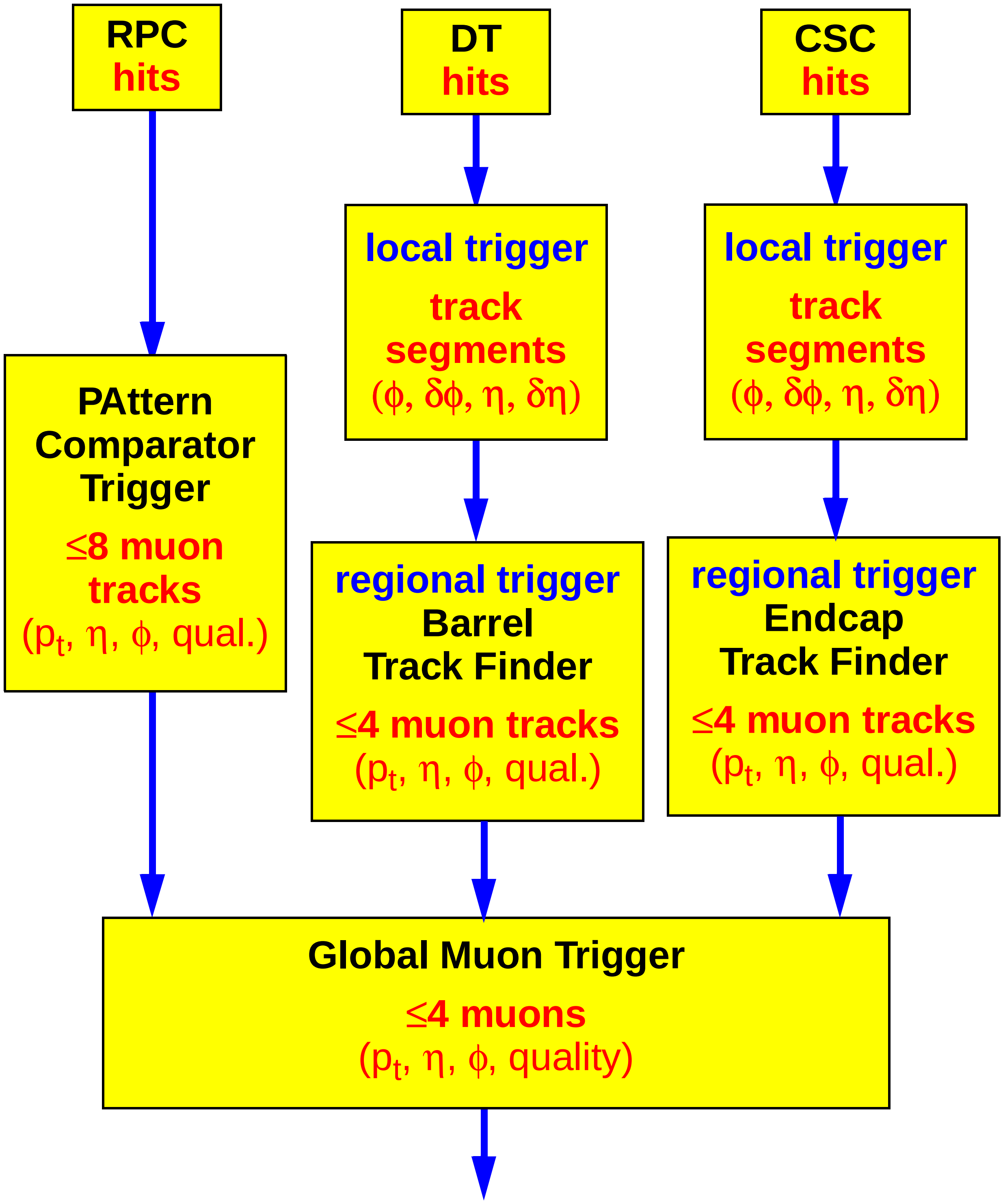
CSC Track Finder

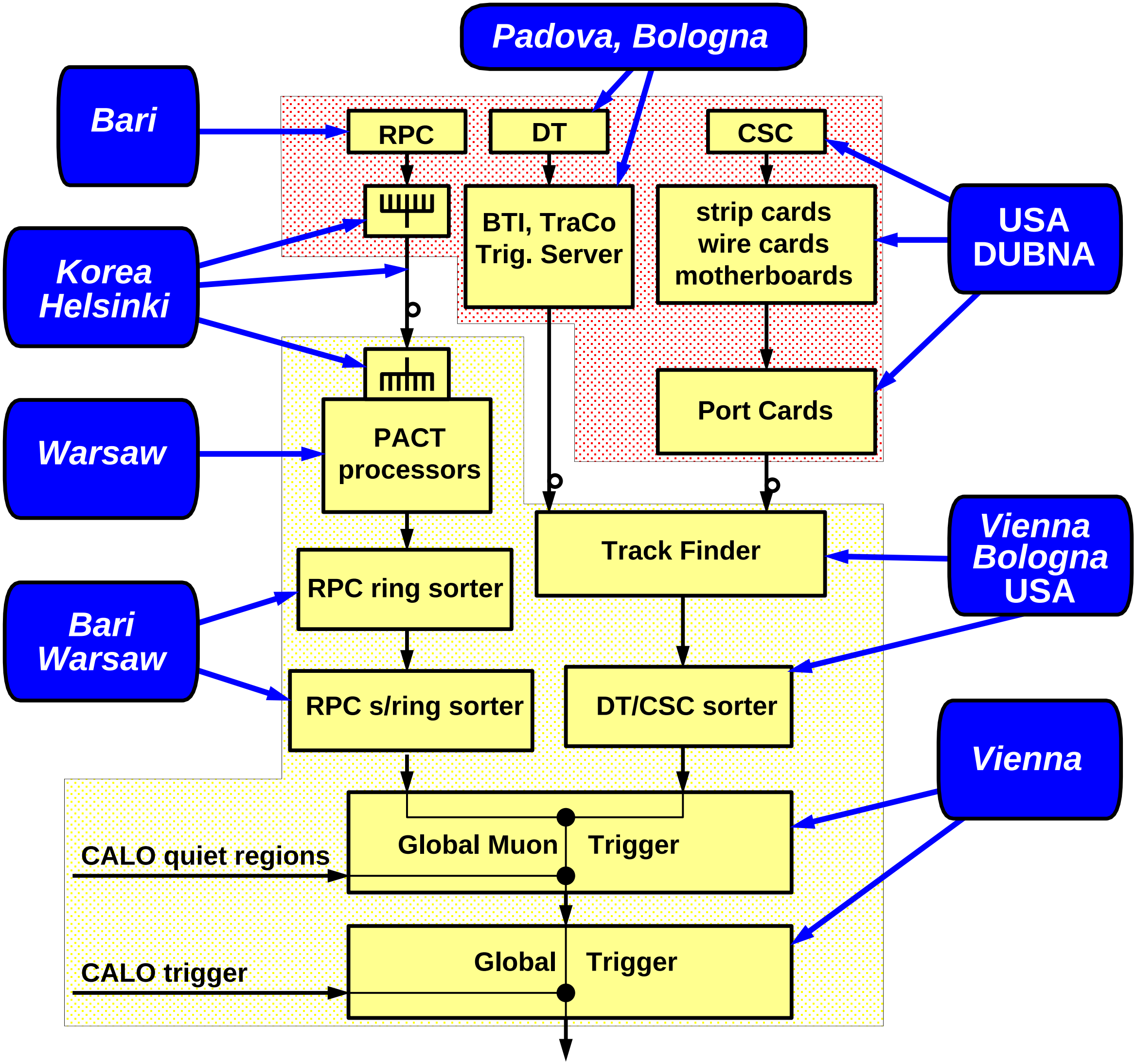
- Accepts CSC vectors from each station
- Accepts Segments from DT Trigger in high $|\eta|$ barrel/endcap overlap region
- Combines track segments into full tracks
- Assigns p_T and quality to each track

Global Muon Trigger

- Separate Sort of 4 highest p_T CSC, DT and 8 highest RPC PACT candidates forms Input
- Examines "quiet bits" from calorimeter to find isolated muons
- Removes Ghosts
- Outputs 4 highest p_T muons to Global Trigger
- Muons identified with $\Delta\eta \times \Delta\phi \sim 0.1 \times 2.5°$
- p_T coded as 5 bits nonlinear; sign; quality

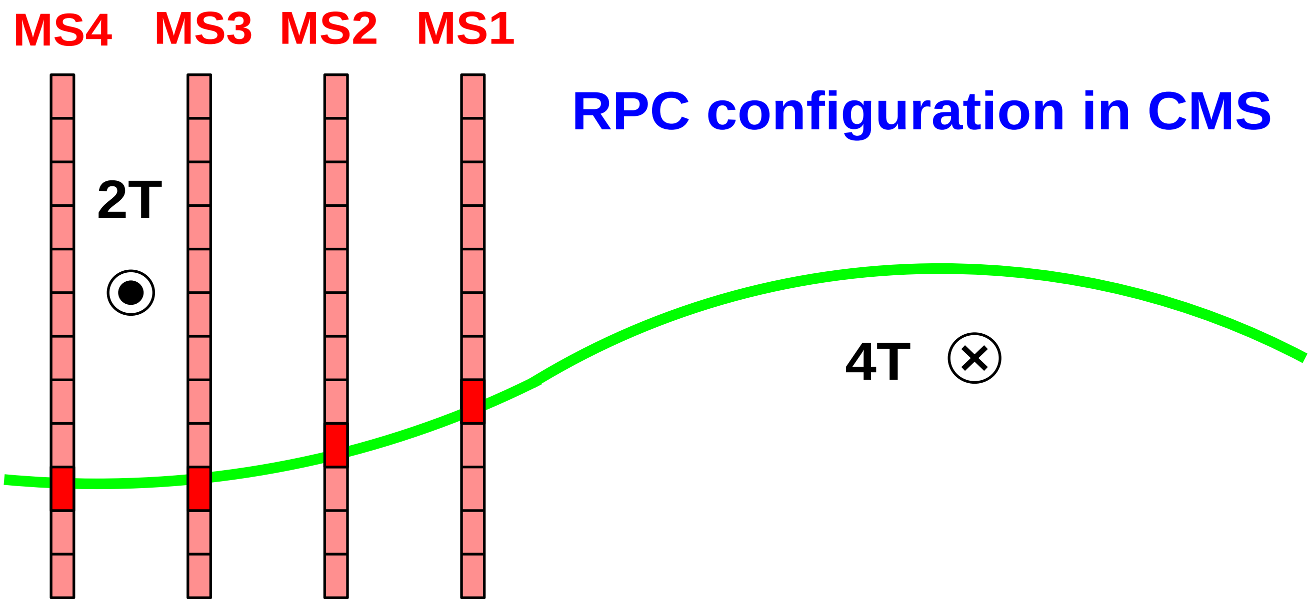
Muon Trigger structure



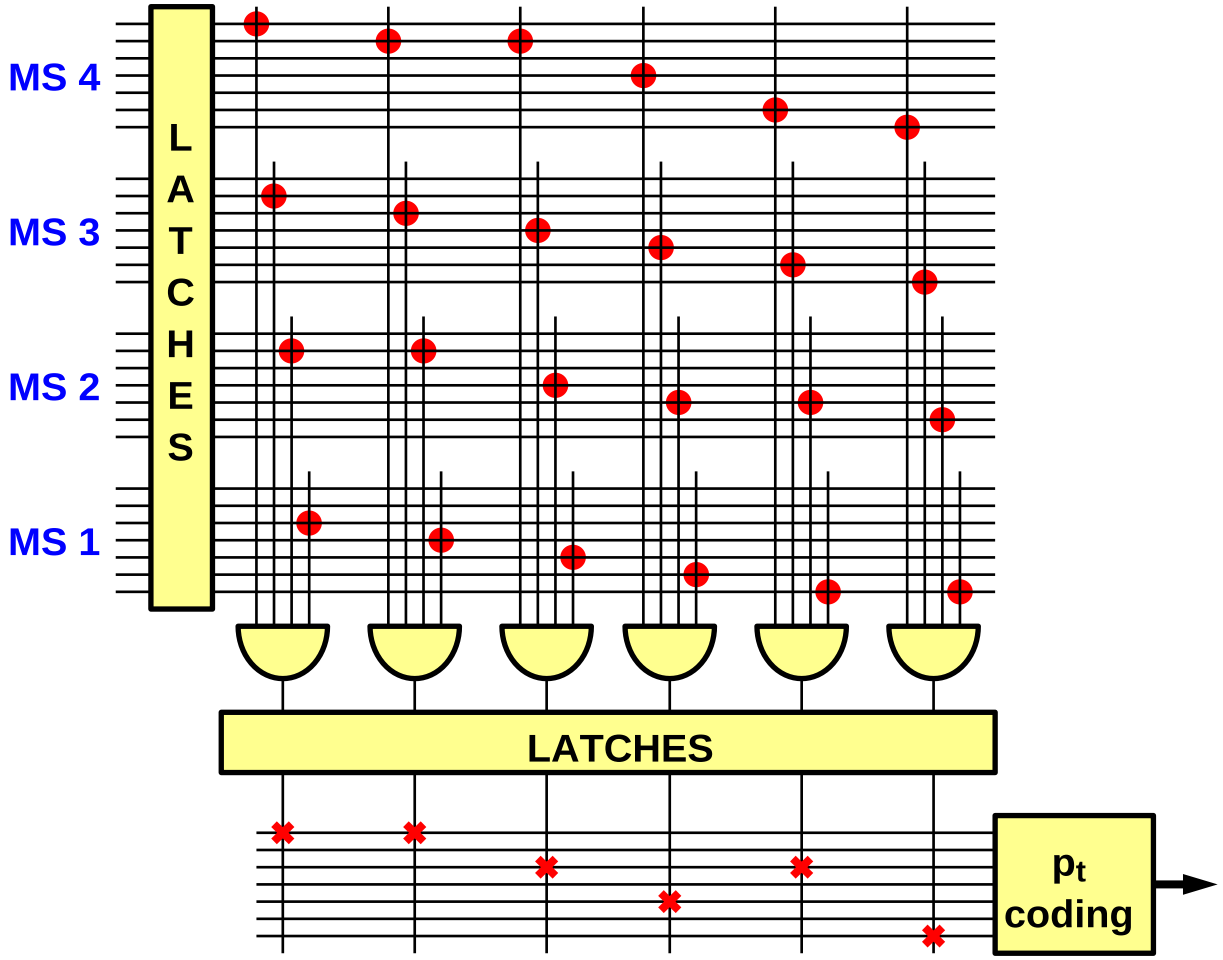


Padova, Bologna
Bari
RPC
DT
CSC
Korea
Helsinki
BTI, TraCo
Trig. Server
strip cards
wire cards
motherboards
USA
DUBNA
Port Cards
PACT
processors
Warsaw
Track Finder
Vienna
Bologna
USA
RPC ring sorter
Bari
Warsaw
RPC s/ring sorter
DT/CSC sorter
Vienna
Global Muon Trigger
CALO quiet regions
Global Trigger
CALO trigger

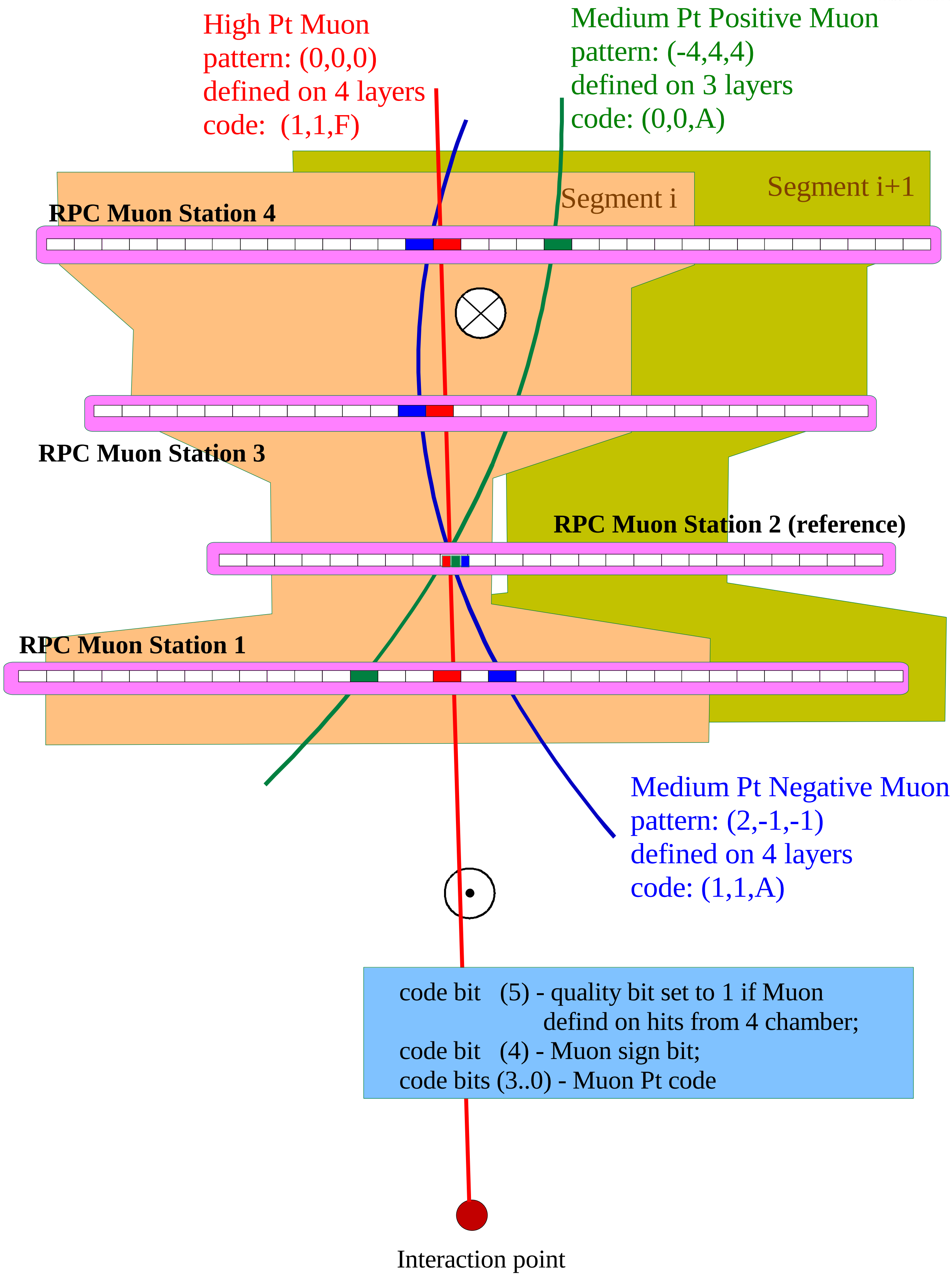
RPC Pattern Comparator Trigger

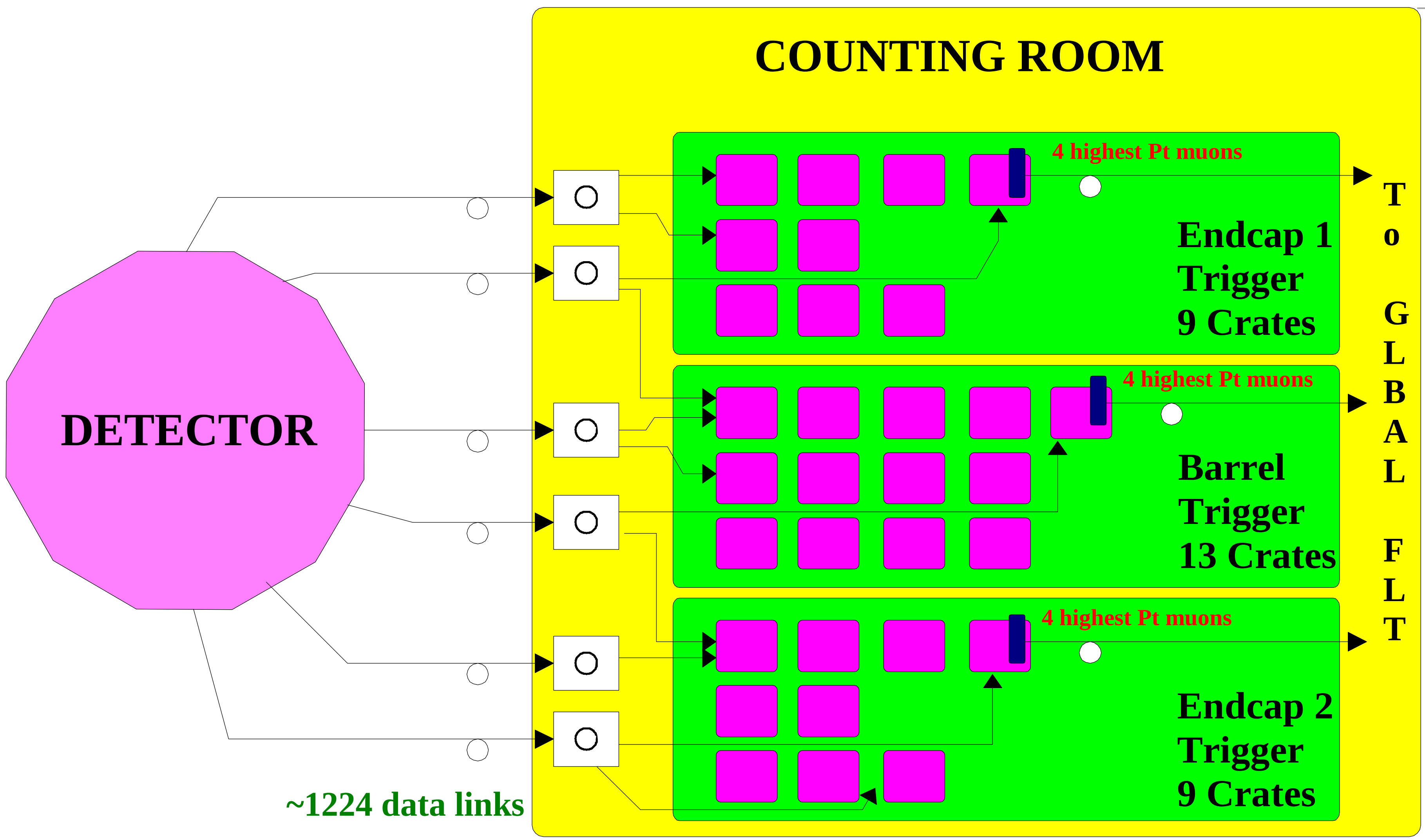


Principle: pattern of hit strips is compared to predefined patterns corresponding to various p_t.

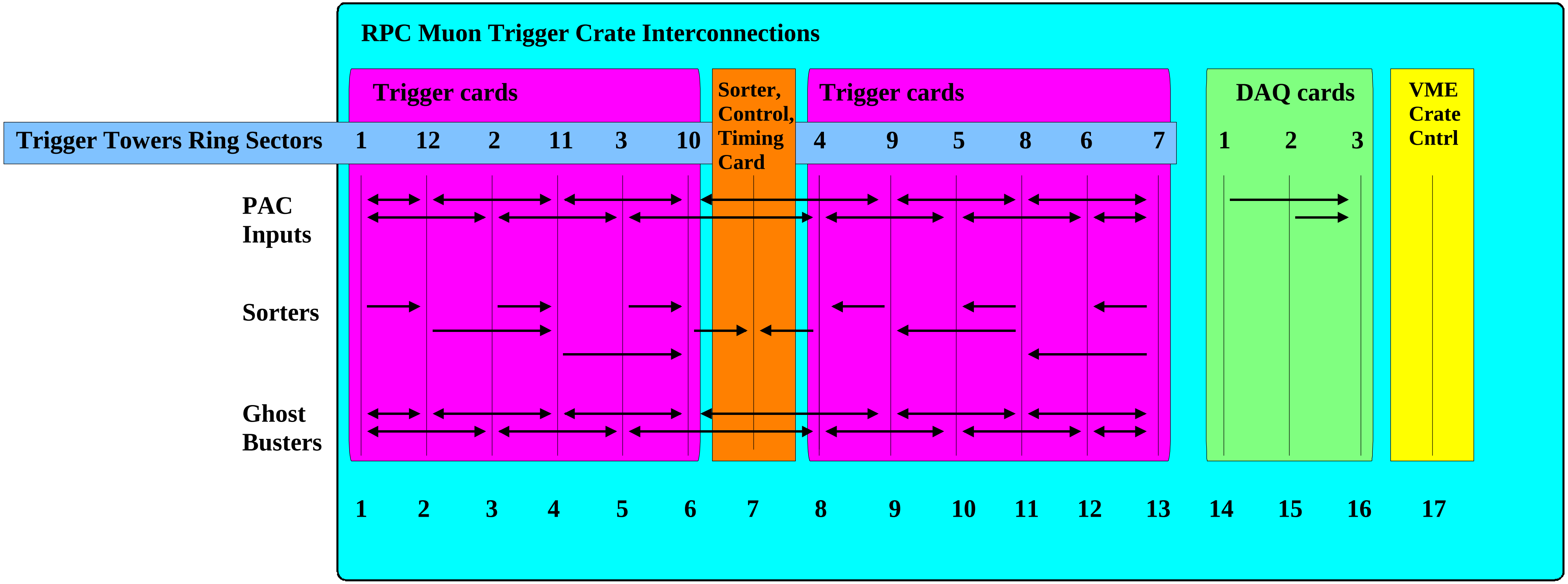


Pattern Comparator (PAC) - idea

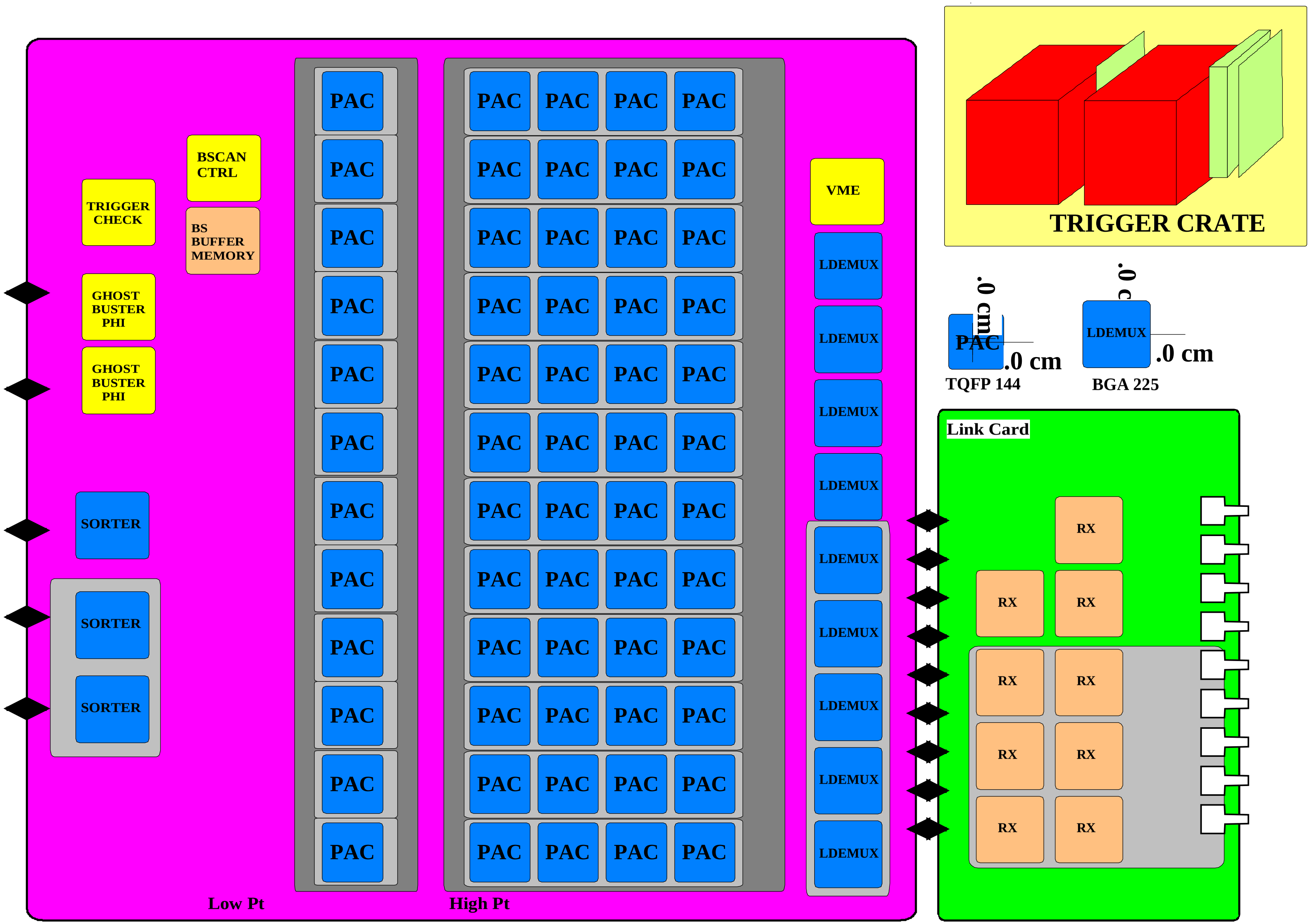



COUNTING ROOM
DETECTOR
4 highest Pt muons
Endcap 1
Trigger
9 Crates
4 highest Pt muons
Barrel
Trigger
13 Crates
4 highest Pt muons
Endcap 2
Trigger
9 Crates
To GLOBAL FLT
~1224 data links

Trigger Crate



Trigger Board (barrel)



PAC test results :

40 dies (10 packed, 30 unpacked) delivered March 98

All building blocks of every packed PAC tested.
The results are following:

- PAC programming (via JTAG - 10 MHz clock):
- **- 8 PAC's - OK;**
- **- 1 PAC - 1 pattern bank not accesible;**
- **- 1 PAC - intermittent error.**

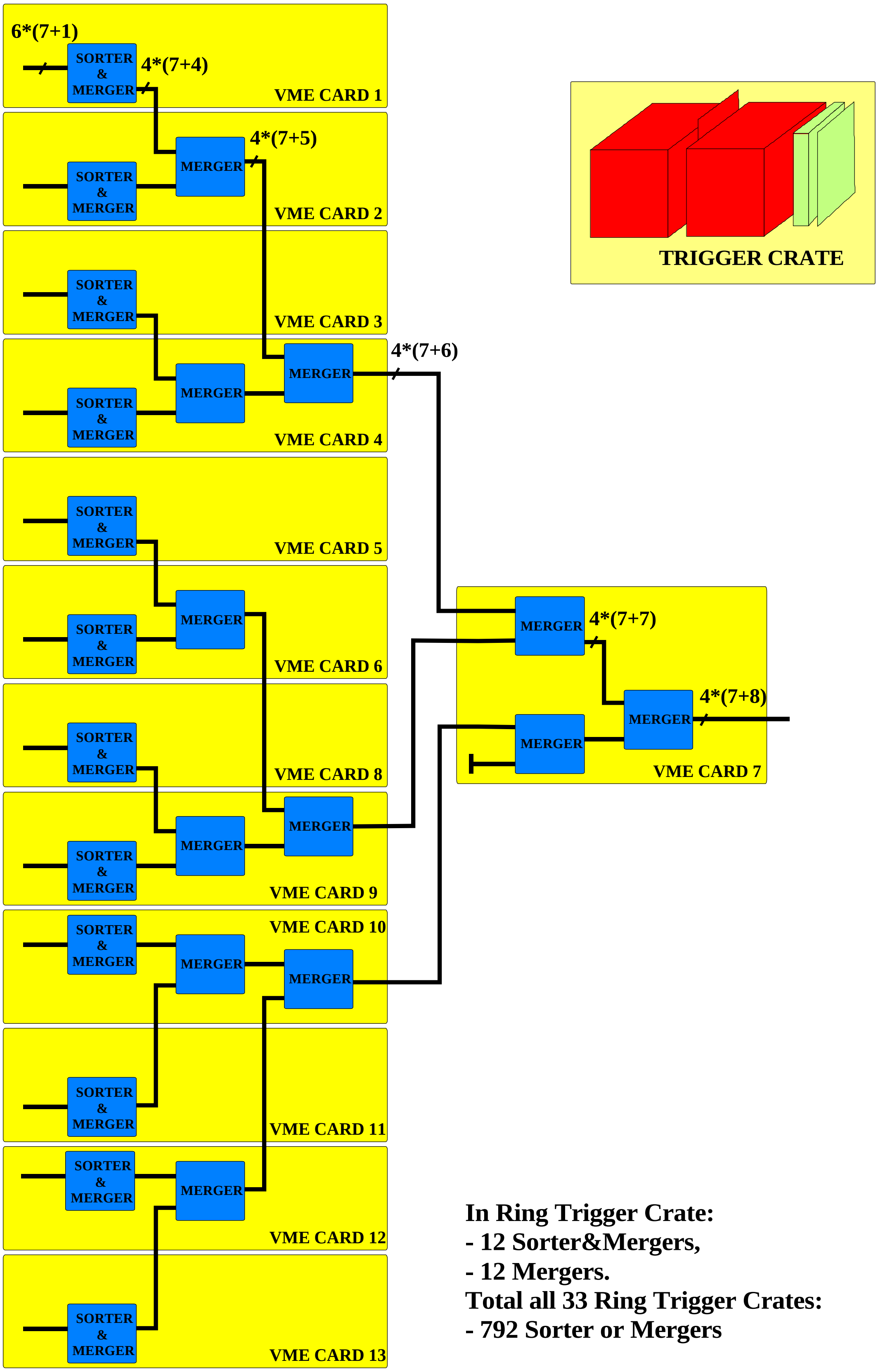
- cascade, mask circuit:
- **- 10 PAC's - OK;**

- encoding circuit:
- **- 10 PAC's - OK;**

- code selection circuit (demuxes):
- **- 10 PAC's - OK;**

- pattern selection circuit (muxes):
- **- fast test - logically OK**
  but timing problem found at level of input buffer and dynamic logic:
  - 3/4 tracks are working from 30 ns clock,
  - 4/4 track code are extended to 2 bx's.

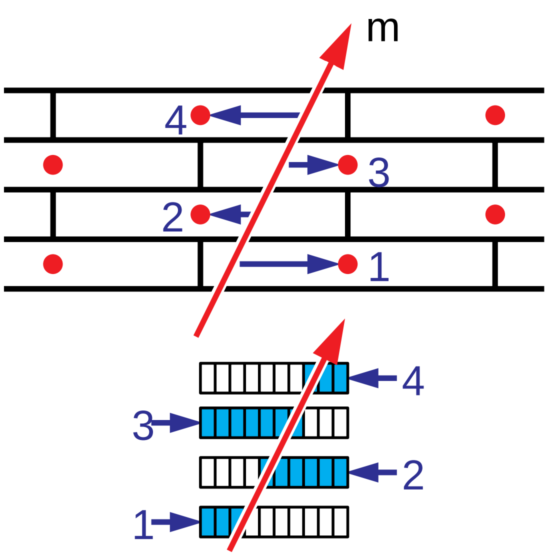
Sorting tree in Ring Trigger Crate



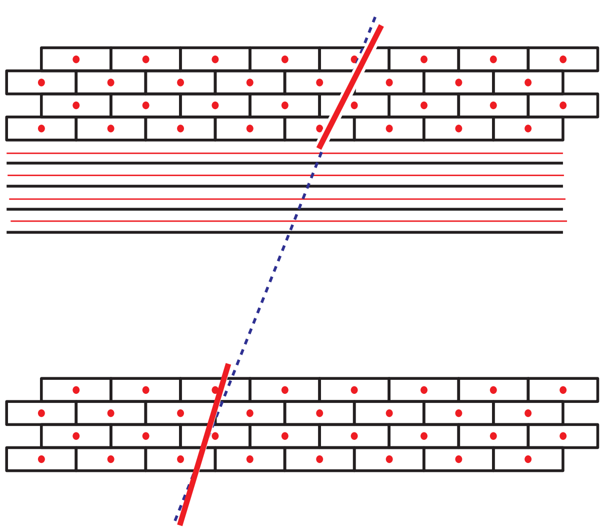
In Ring Trigger Crate:
- 12 Sorter&Mergers,
- 12 Mergers.
Total all 33 Ring Trigger Crates:
- 792 Sorter or Mergers

Muon Chamber Triggers

Drift Tubes (DT)

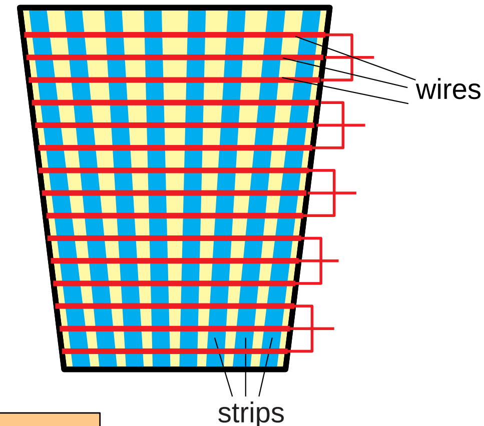


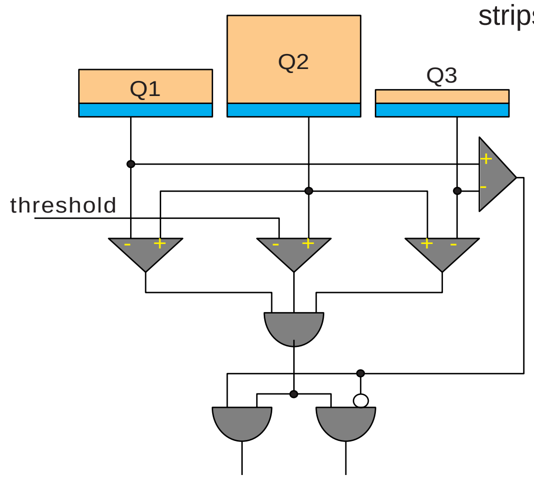
Meantimers recognize tracks and form vector / quartet.



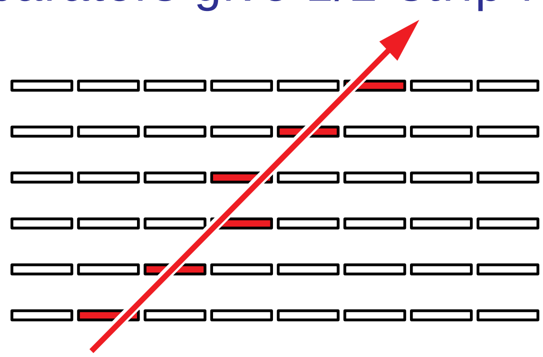
Correlator combines them into one vector / station.

Cathode Strip Chambers (CSC)

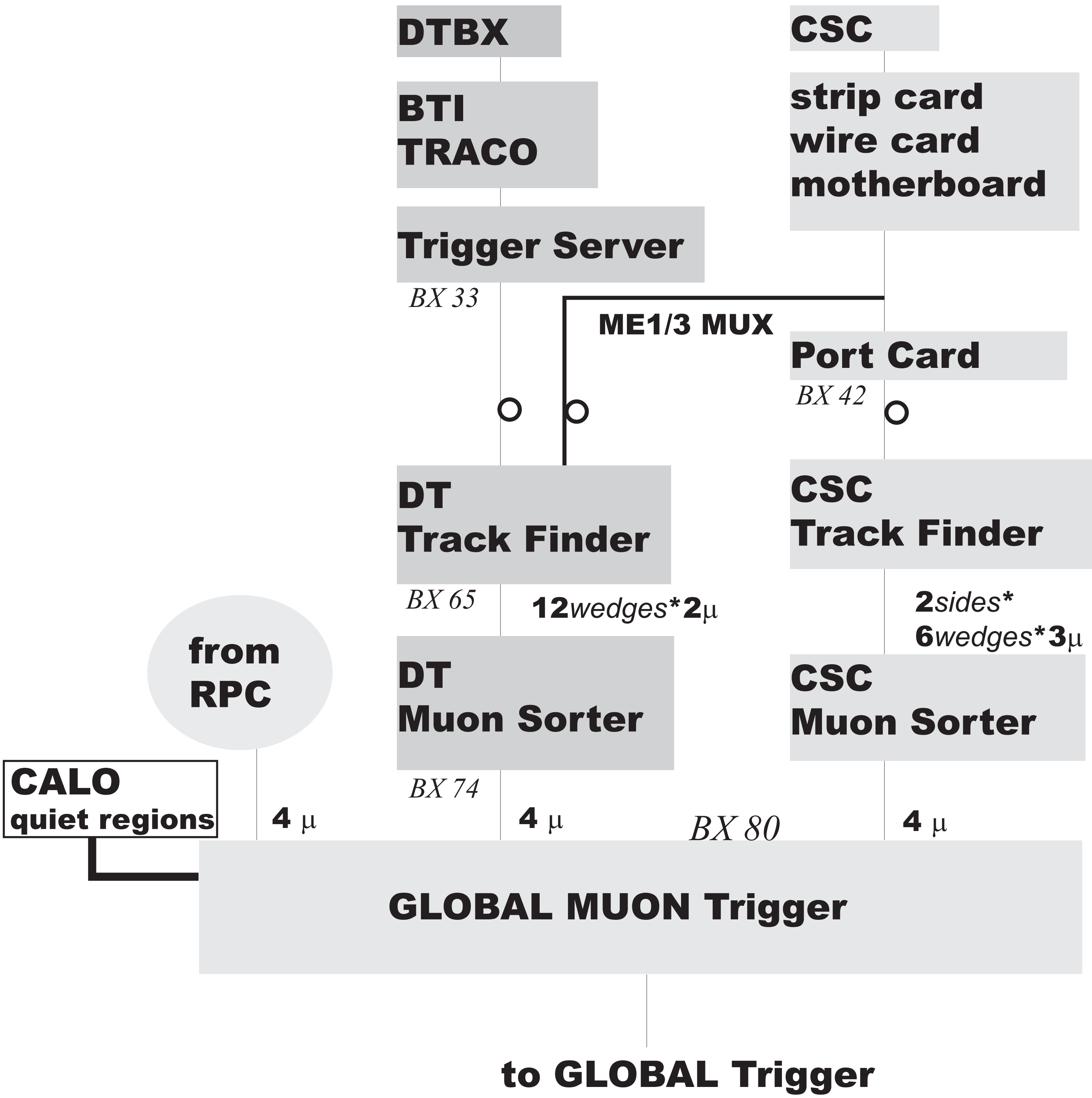




Comparators give 1/2-strip resol.

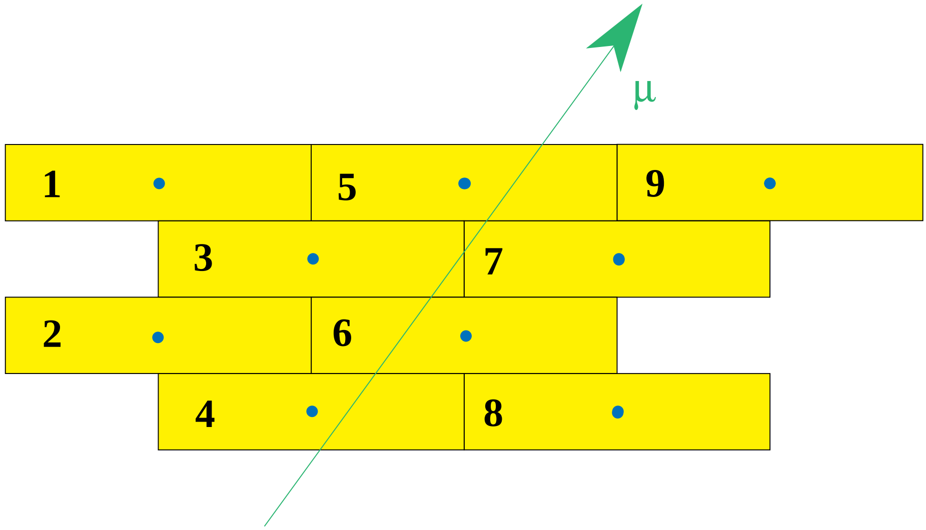


Hit strips of 6 layers form a vector.



M.Dallavalle /INFN Bologna

Bunch and Track Identifier

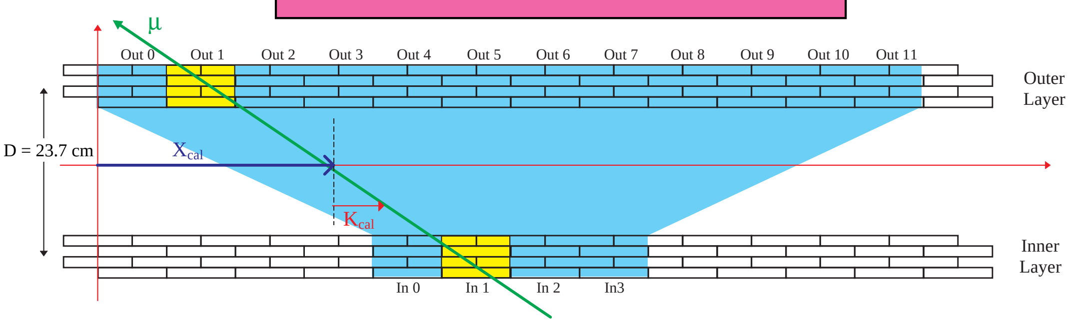


Bunch crossing is detected using a generalized mean-timer method
At the same time the track inclination and position are measured

Triggers → HTRG Alignment of four hits
LTRG Alignment of three hits

LTRG triggers close to a HTRG are suppressed (LTS mechanism)

Track Correlator

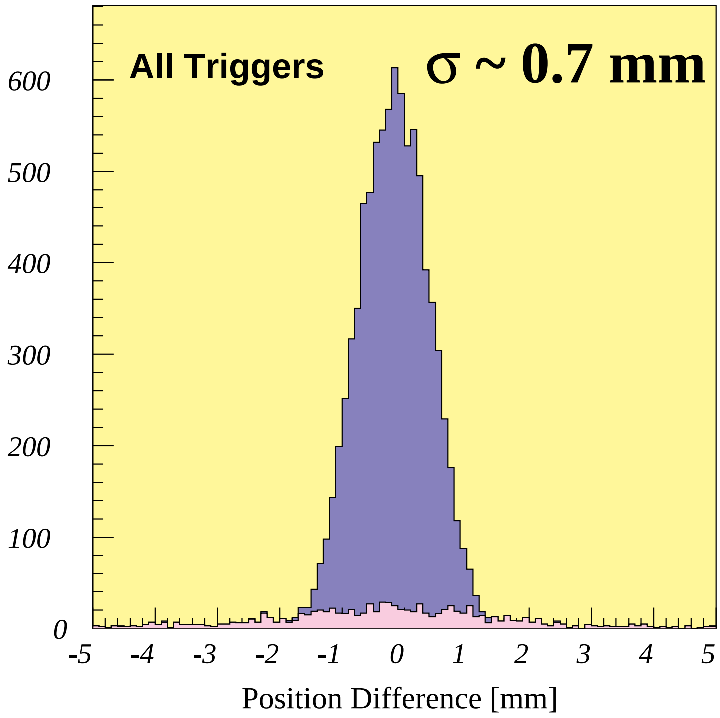


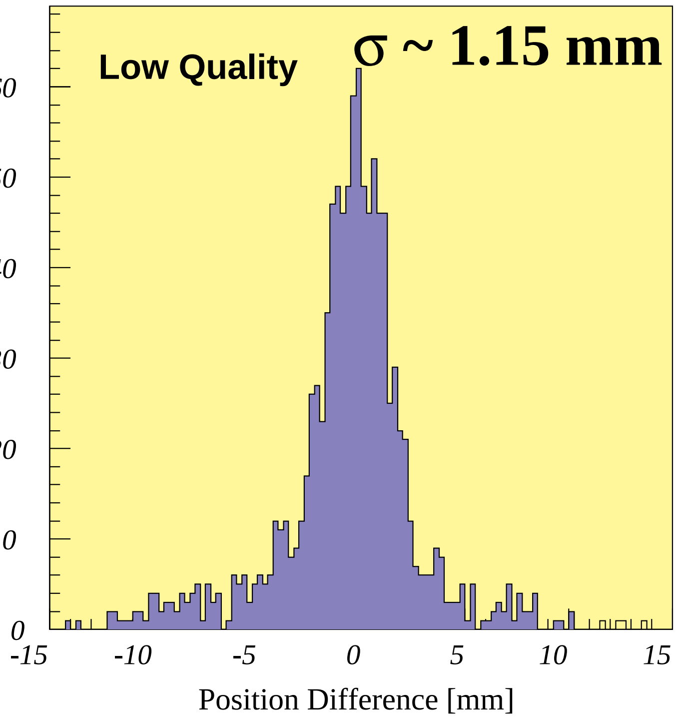
Correlates BTIs in the inner and outer Superlayers
Refines the track measurement
Applies noise filtering using θ-view information

Position parameter quality

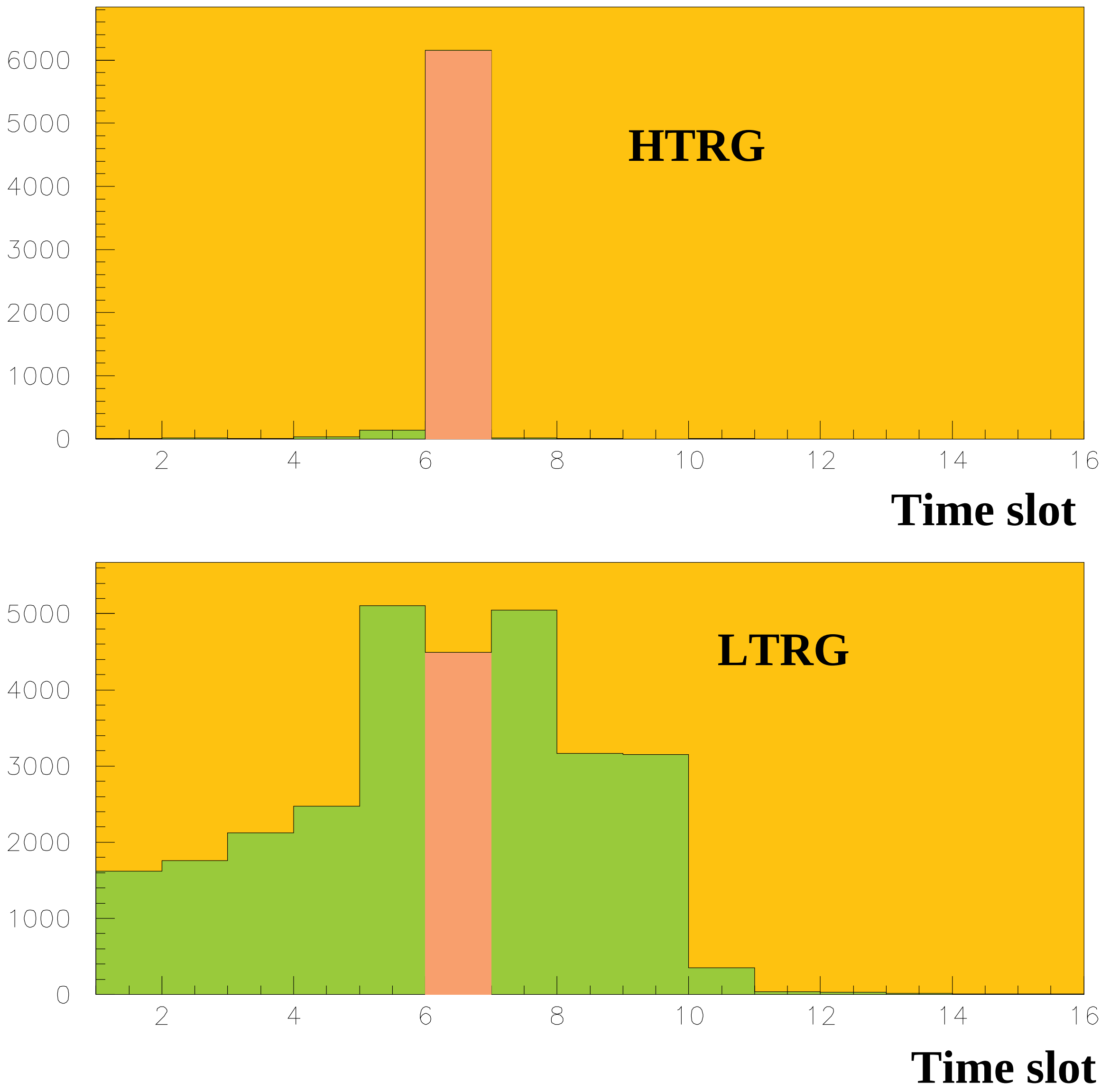
BTI # 6

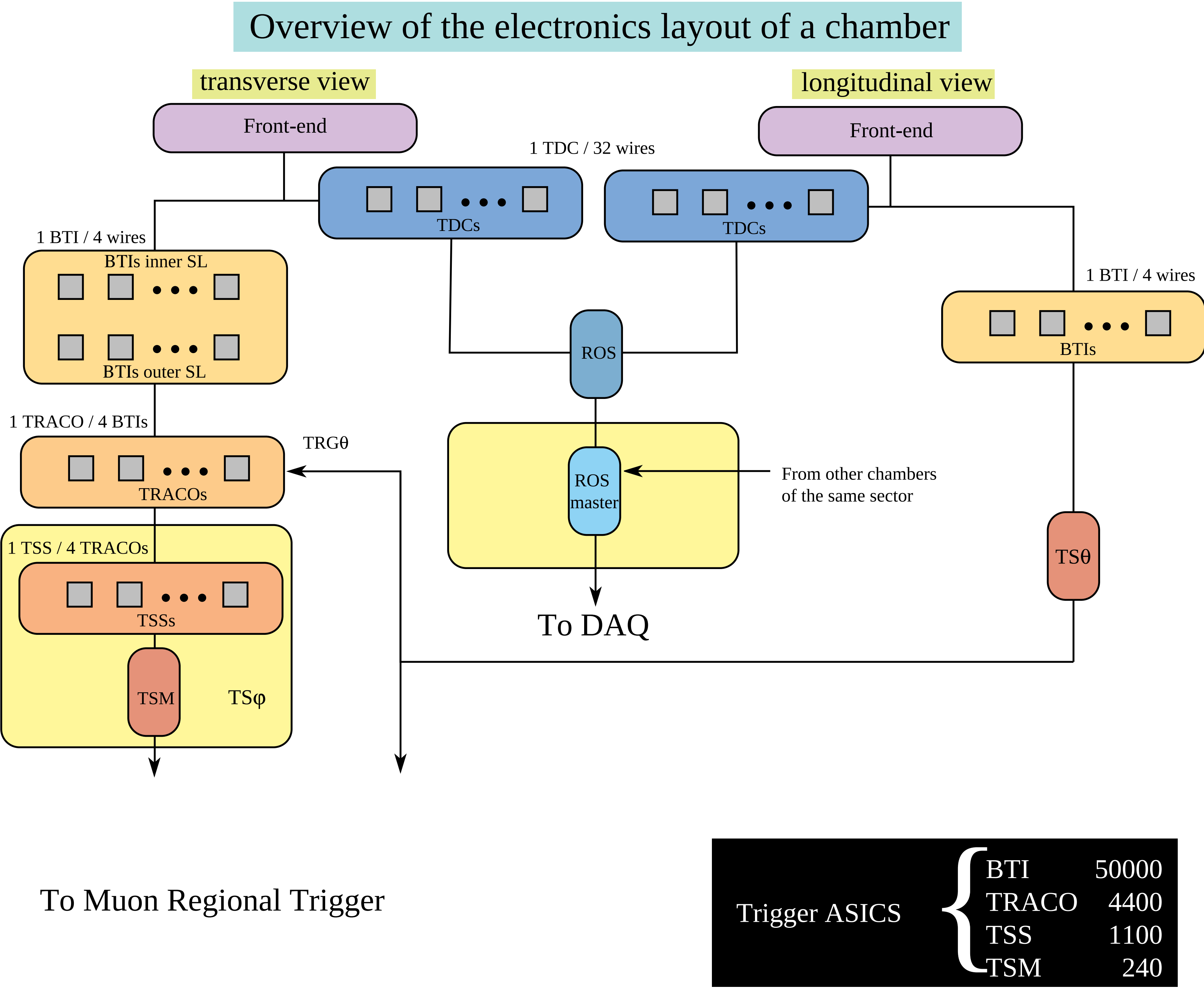
in the right time slot



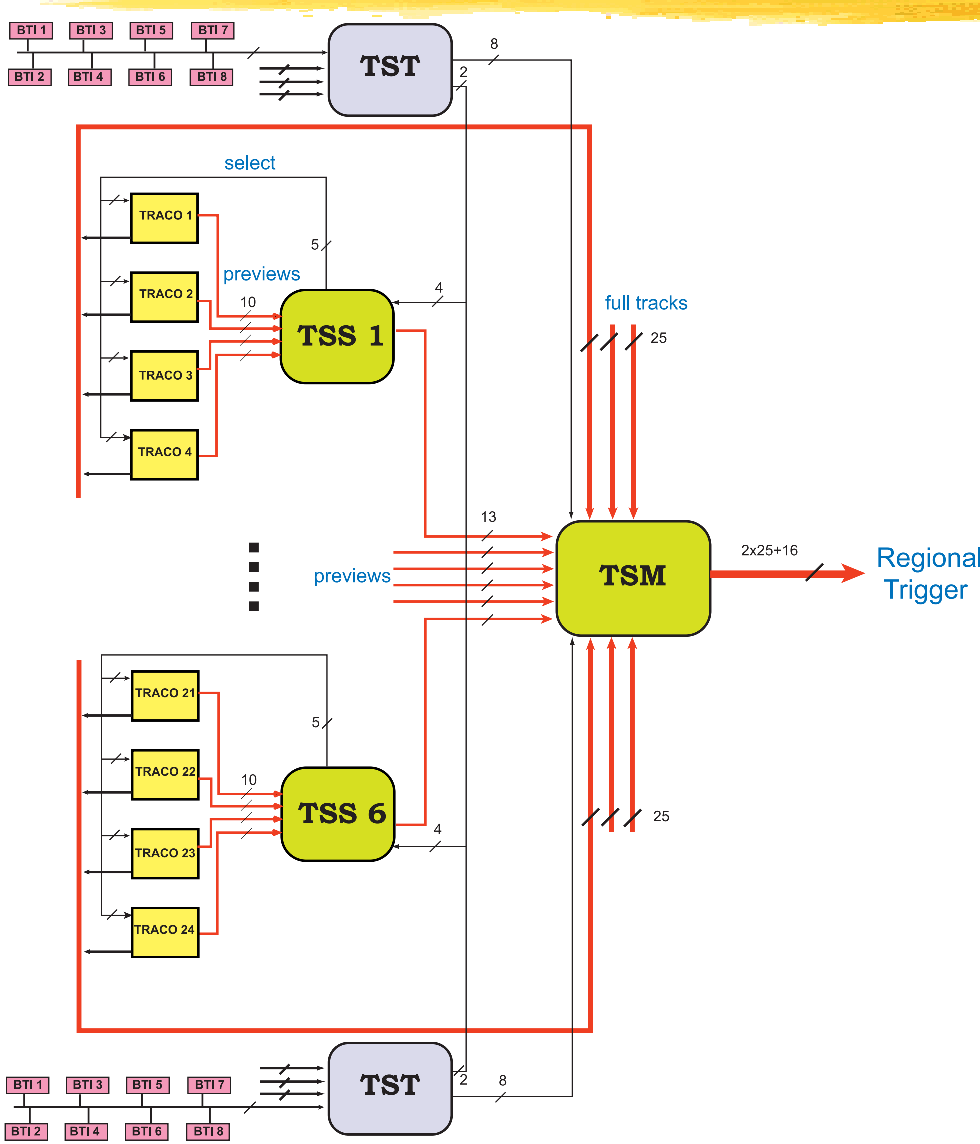


Time distribution of BTI triggers




Overview of the electronics layout of a chamber
transverse view
longitudinal view
Front-end
Front-end
1 TDC / 32 wires
TDCs
TDCs
1 BTI / 4 wires
BTIs inner SL
BTIs outer SL
1 BTI / 4 wires
BTIs
ROS
1 TRACO / 4 BTIs
TRGθ
TRACOs
ROS
master
From other chambers
of the same sector
1 TSS / 4 TRACOs
TSSs
TSθ
To DAQ
TSM
TSφ
To Muon Regional Trigger
Trigger ASICS
BTI 50000
TRACO 4400
TSS 1100
TSM 240

The Trigger Server architecture (1)



- In order to minimize the speed and the logic, the best solution is a parallel sorting, based on a 2by2 fast comparator, among groups of 4 TRACOs

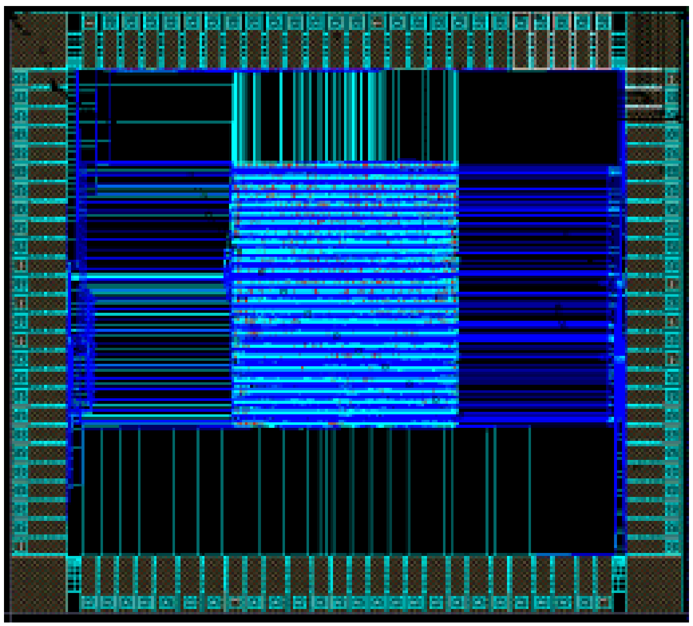
Two layers of processing units in ϕ:

- first layer: one *Track Sorter Slave* (***TSS***) every 4 TRACOs
- second layer: one *Track Sorter Master* (***TSM***) per chamber

In the θ view the *Trigger Server Theta* (***TST***) provides the OR of groups of BTIs: eventually used in ϕ as trigger validation

Full performance ASIC prototype of TSS

- Test performed with programmable devices (XilinX, Altera, QuickLogic) revealed the need of using ASIC to fit the speed requirement



- 10 ASIC prototypes were ready at the beginning of this year:

  CMOS 0.7 μm (ES2 through EuroPractice)
  23 mm² Silicon area
  104 I/O pads
  JTAG and backup parallel interface
  full programmability of sorting

Simulation of the Trigger Server

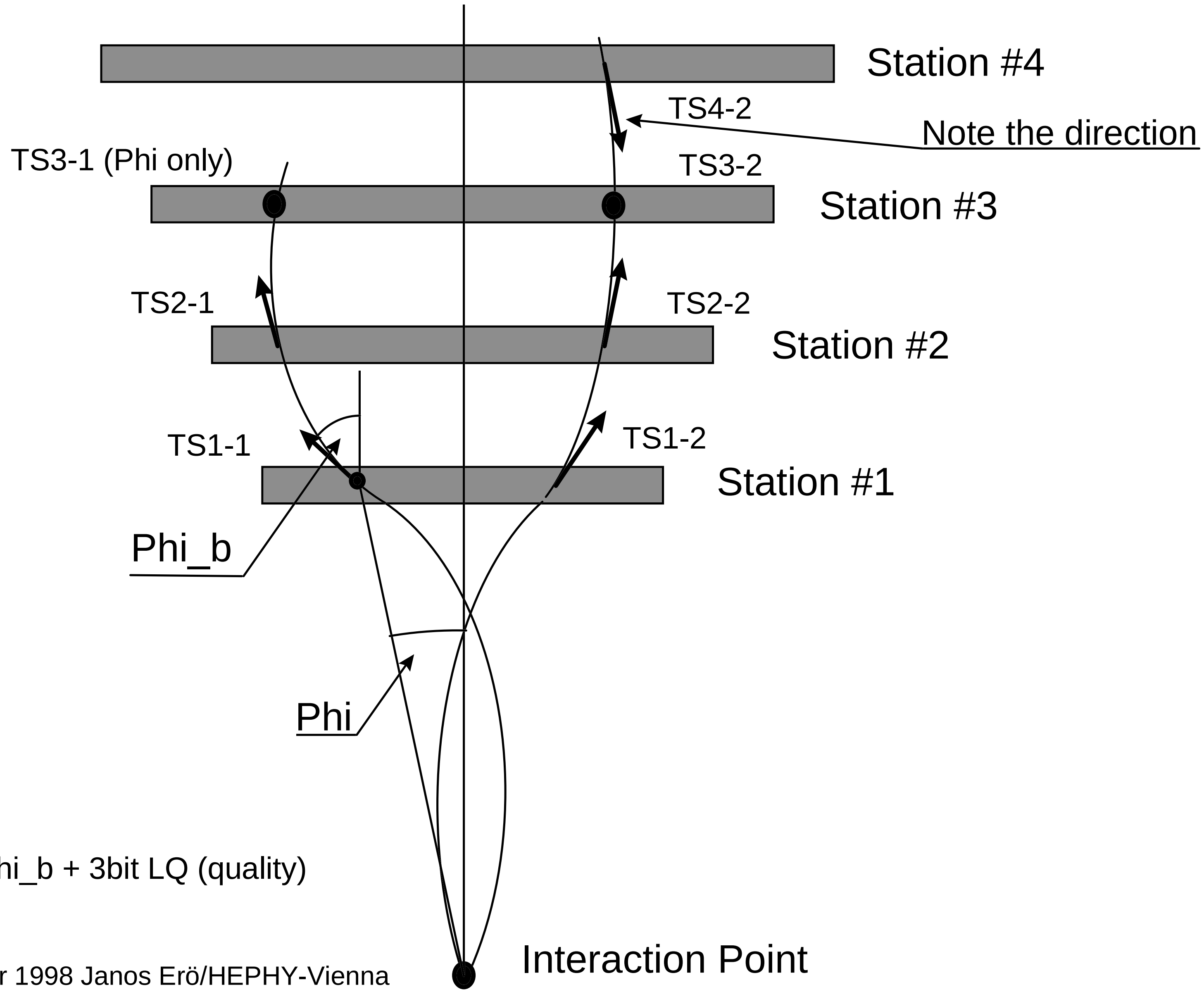
- The TS algorithm has been tested in the frame of the simulation of CMS
- The ideal algorithm should find:
  - only one track segment in single muon events
    (reject ghosts produced by nearby TRACOs)
  - two correct segment in two muon events
    (high efficiency and purity on second segment)

- Simulation with one or two muons of 100 GeV gives positive results

Efficiency for 2nd track	80 %
Efficiency for 2nd track in open pairs	**98 %**
Prob. of correct id of both tracks	86 %
Prob. of correct id of both tracks in open pairs	**95 %**
Prob. of generating a fake 2nd track (in one muon events)	**< 4 %**

Open pairs = two muons distant more than 1 TRACO

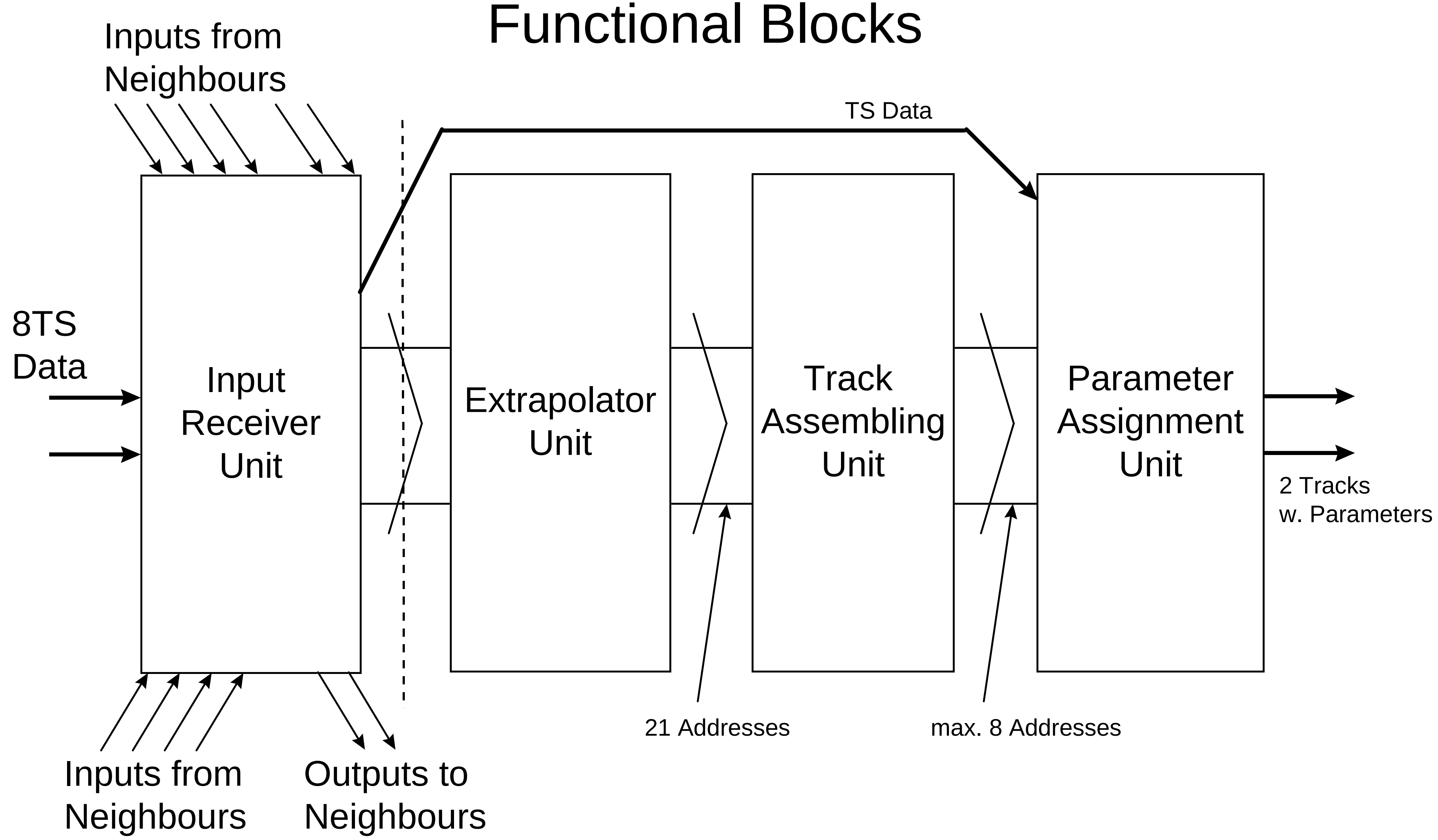
Find a Muon Track



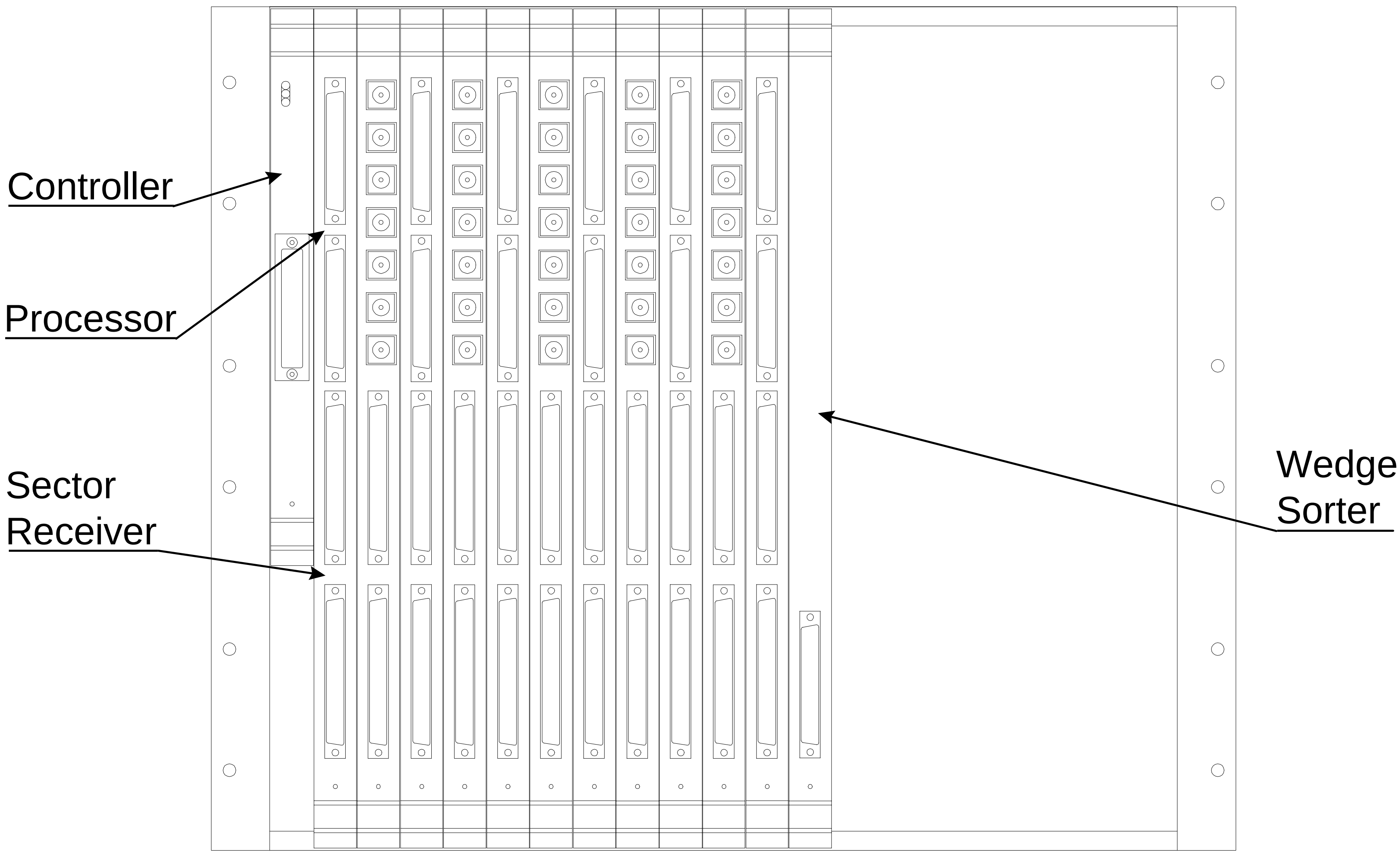
TS: 11bit Phi +8bit Phi_b + 3bit LQ (quality)

Track Finder Processor

Functional Blocks



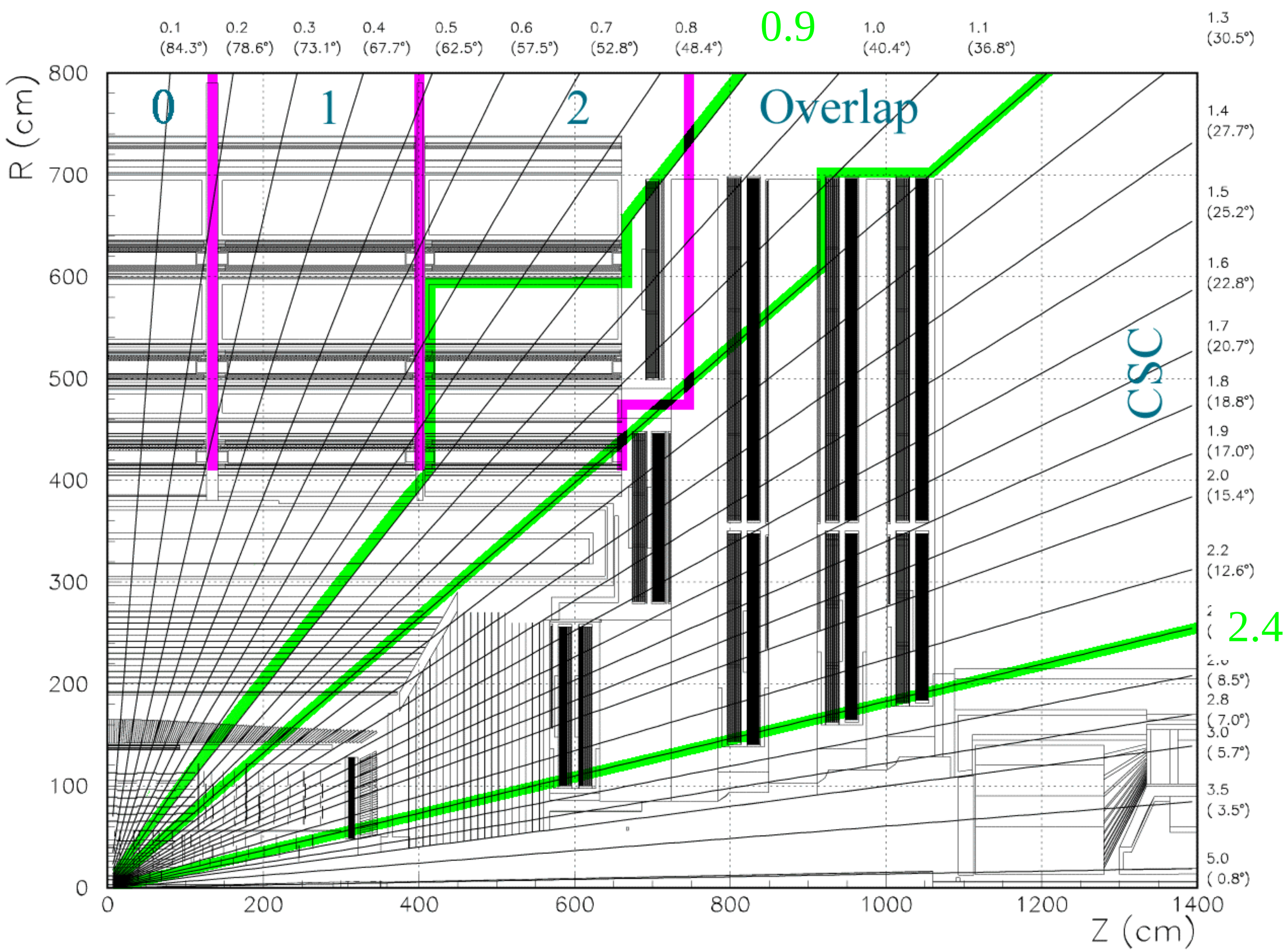
Crate with Sector Receivers



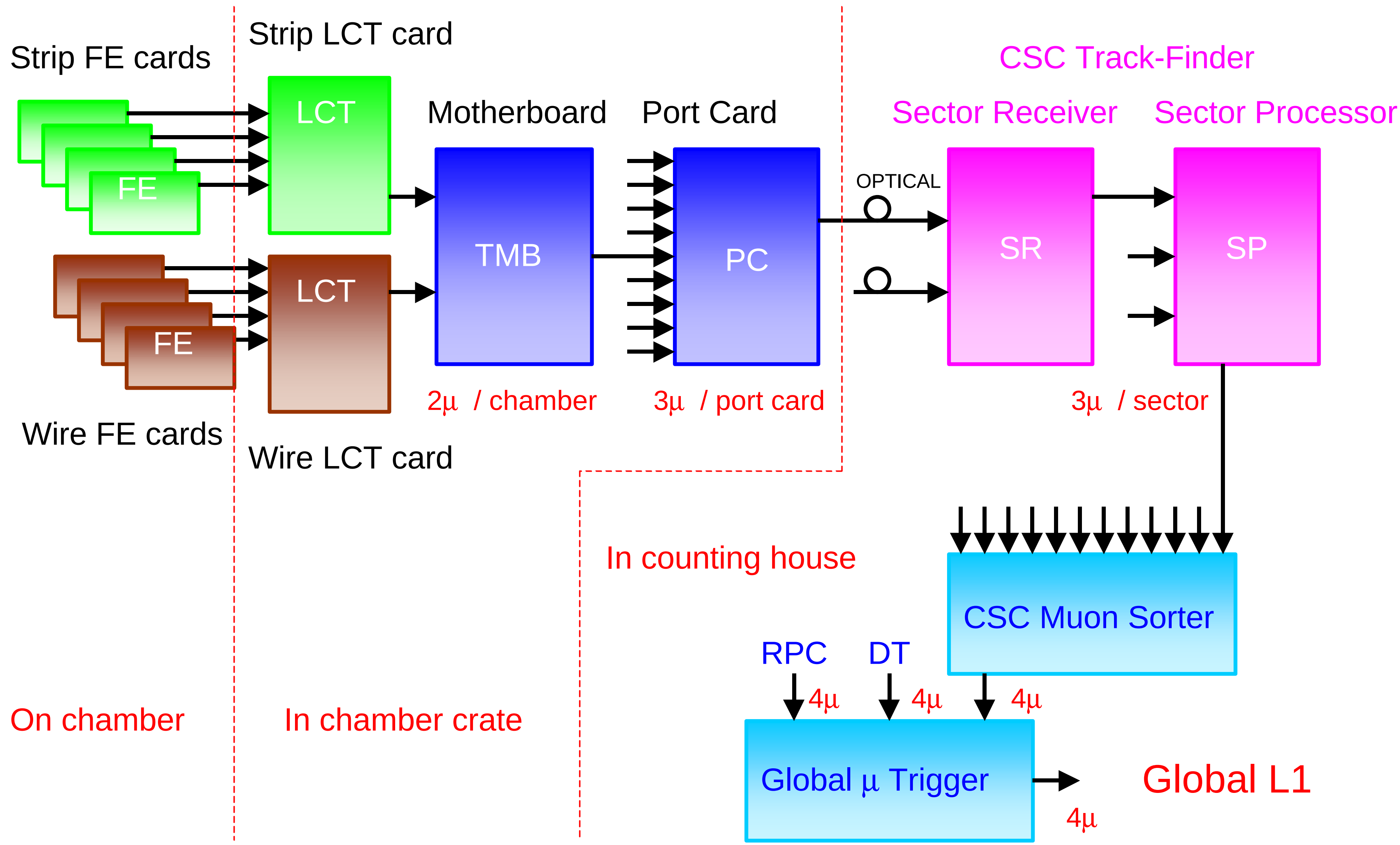
Drift Tube Regional Trigger

Vienna Prototype Track-Finder Test Setup

Trigger Regions in η



CSC Muon Trigger Scheme



Trigger Crates

Each iron disk handles 12 sectors

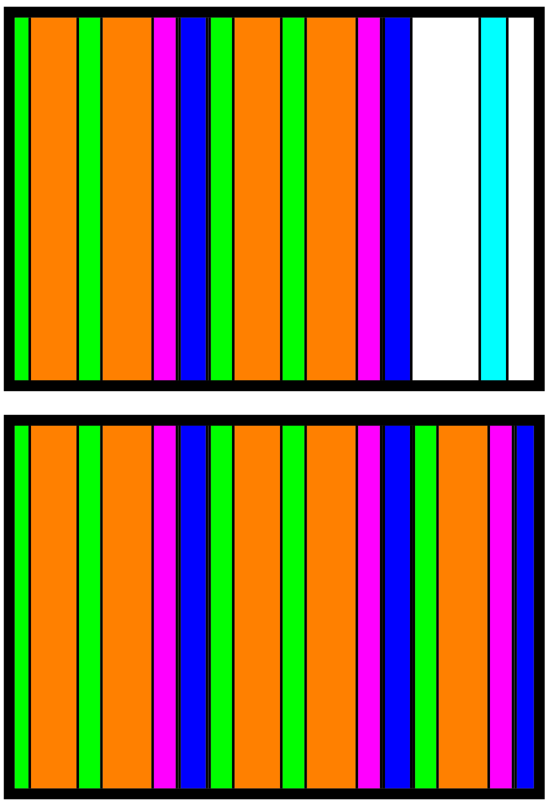
30^{o} sectors on YE1 for ME1,

60^{o} sectors on YE2 for ME2 and ME3

Per sector:

Type	Board	Slots
CLCT	9	9
ALCT	9	18
MBT	5	5
MBD	5	5
MPC	1	1
Total	29	38

Fits two 9U crates



Positions of 24 crates around the iron disks is under discussion.

‘98 Prototypes: 48-ch LCT Card

Software configurable as anode or cathode LCT

Channel link
To TMB

P0 Mezzanine Card
Comparators,
A/D conversion

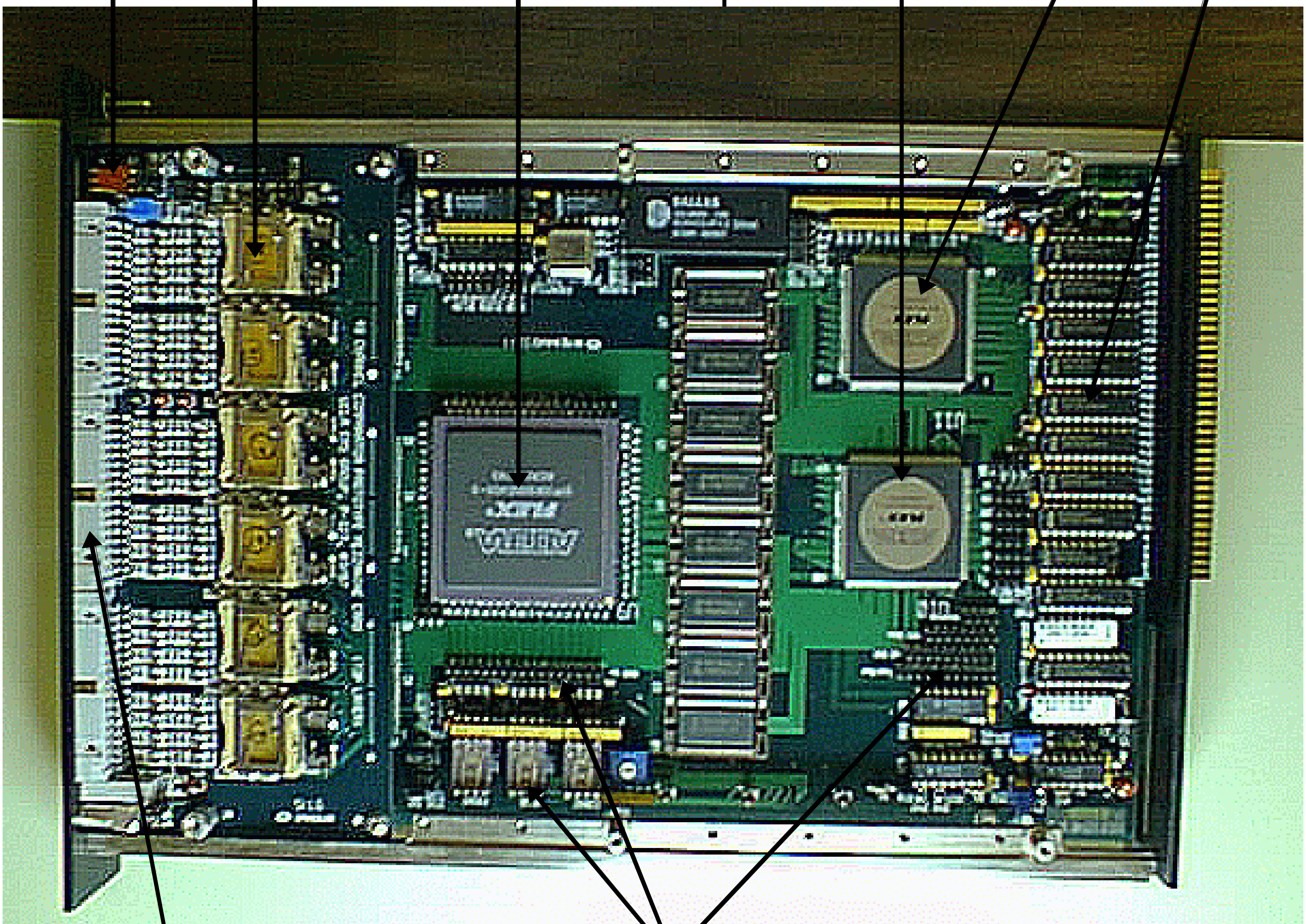
Input Gate Array
Altera 10K50
Data selection

RAM tables
128K x 8 bit

Output Gate Array
Altera 10K20
Priority encoders,
Sequencer

CAMAC Gate Array
Altera 10K20

Buffers

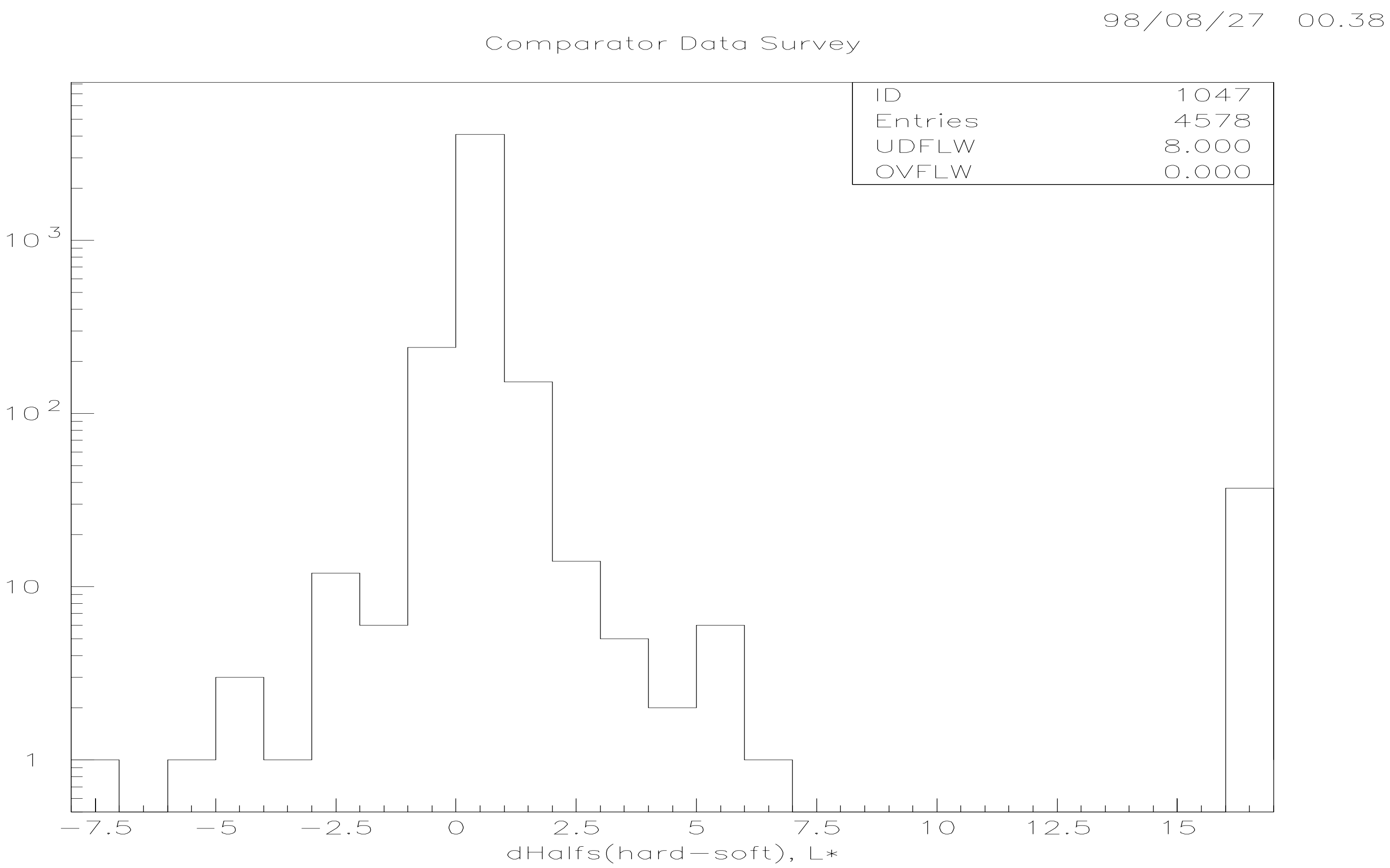


JTAG ports,
Analog inputs,
Ext Clk, Trig,
LEDs

Test points,
LEDs

Comparator Study #2

- **Fit track in Layers 1,2,4,5,6, look at comparator bits in Layer 3.**
- **Simple tracking results are good**
  - →**No corrections for gain, xtalk, etc.**
  - →**Energy-weighted means**
  - →**Corrected means by sin(x) gives ~300um resolution**



Anode BX Efficiency Summary

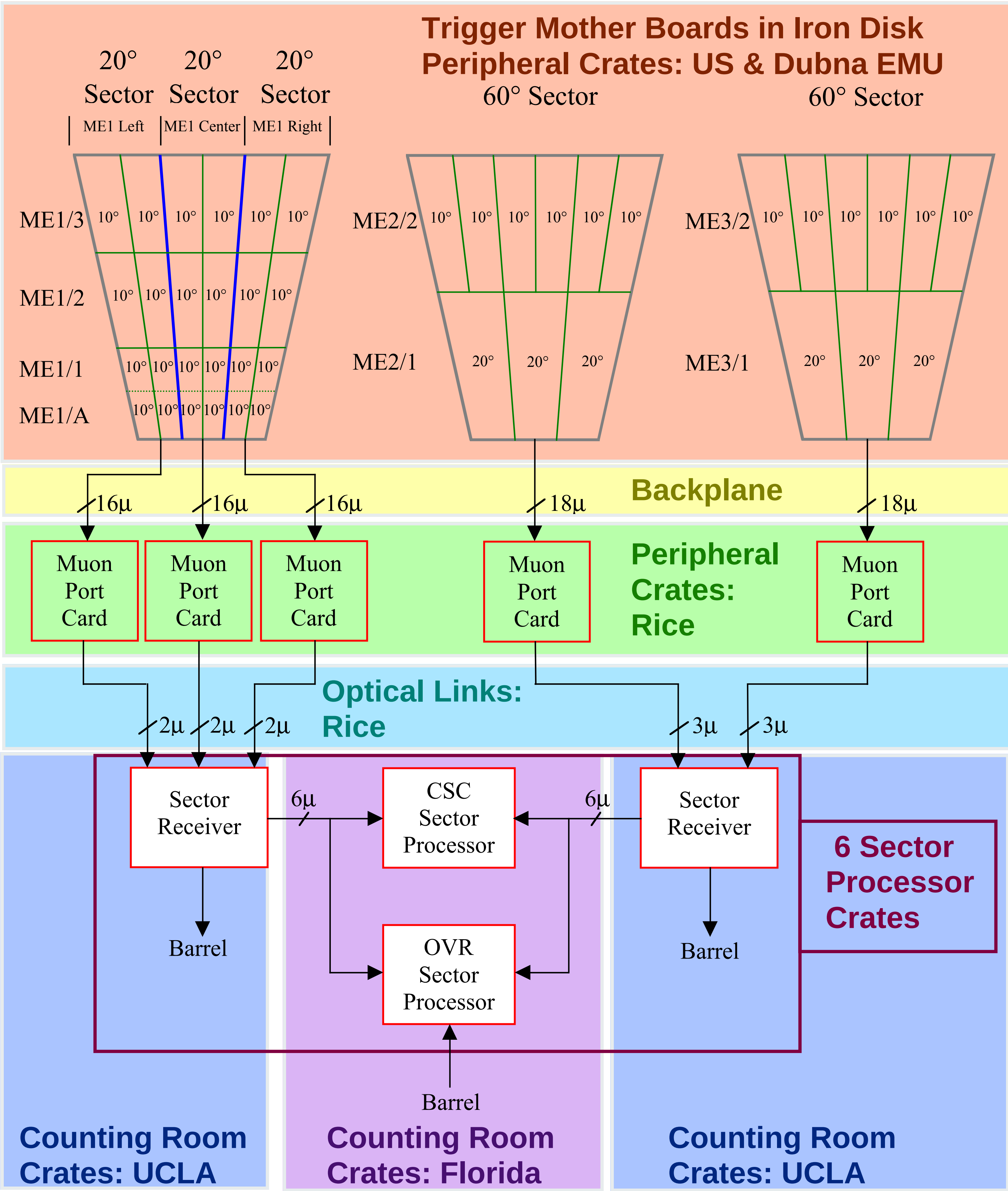
Run 183 at H2

old gas, HV=3.9kV, θ=25°, ϕ=0°, μ^+(225), 4x4cm trig

anode thresholds 15~58fC

Coincidence Level	Relative Timing	BX Efficiency
1	0ns	98.0±1.0%
2	**+3ns**	**99.2±0.3%**
3	+8ns	99.2±0.3%
4	+12ns	99.1±0.5%
5	+14ns	98.5±0.6%
6	+19ns	98.0±0.8%

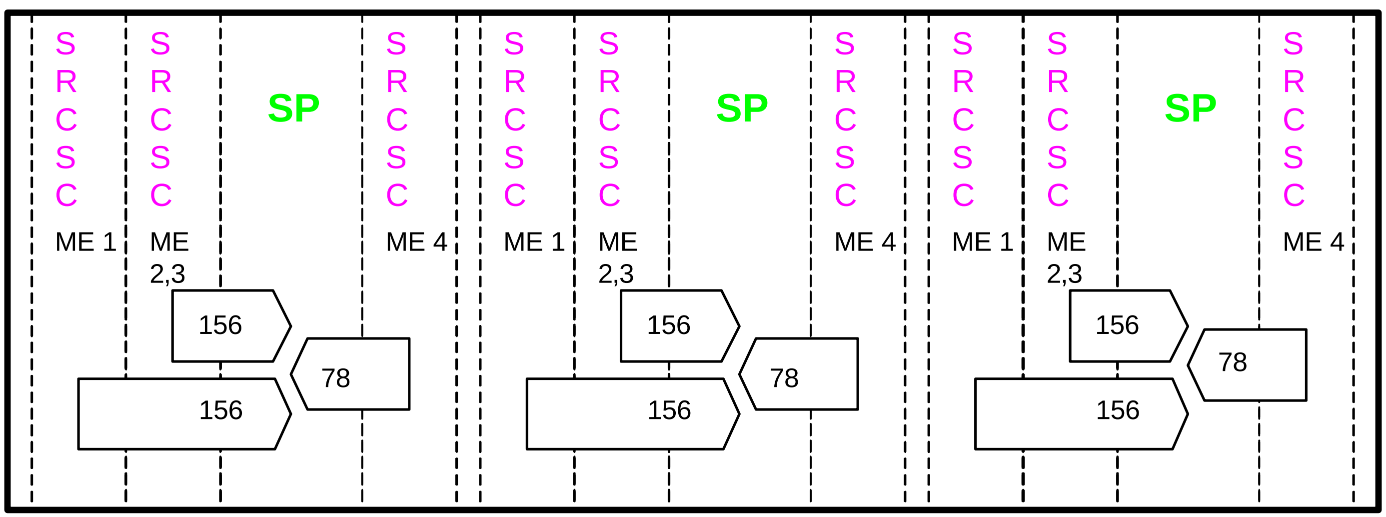
CSC Trigger Layout



Inputs to CSC Sector Processor

- 1 CSC stub = 12 φ bits + 6 Ψ bits + 5 η bits + 3 Q bits = 26 bits
- 1 Port Card sends 3 stubs
- 1 Sector Receiver accepts 2 Port Cards = 6 stubs
- 1 Sector Processor accepts 6 + 3 + 3 + 3 = 15 stubs (divided between 2.5 Sector Receivers)
- 15 stubs $\times$ 26 bits = 390 bits

CSC crate: 9U VME with custom point-to-point backplane for last 3U



Sector Processor Block Diagram

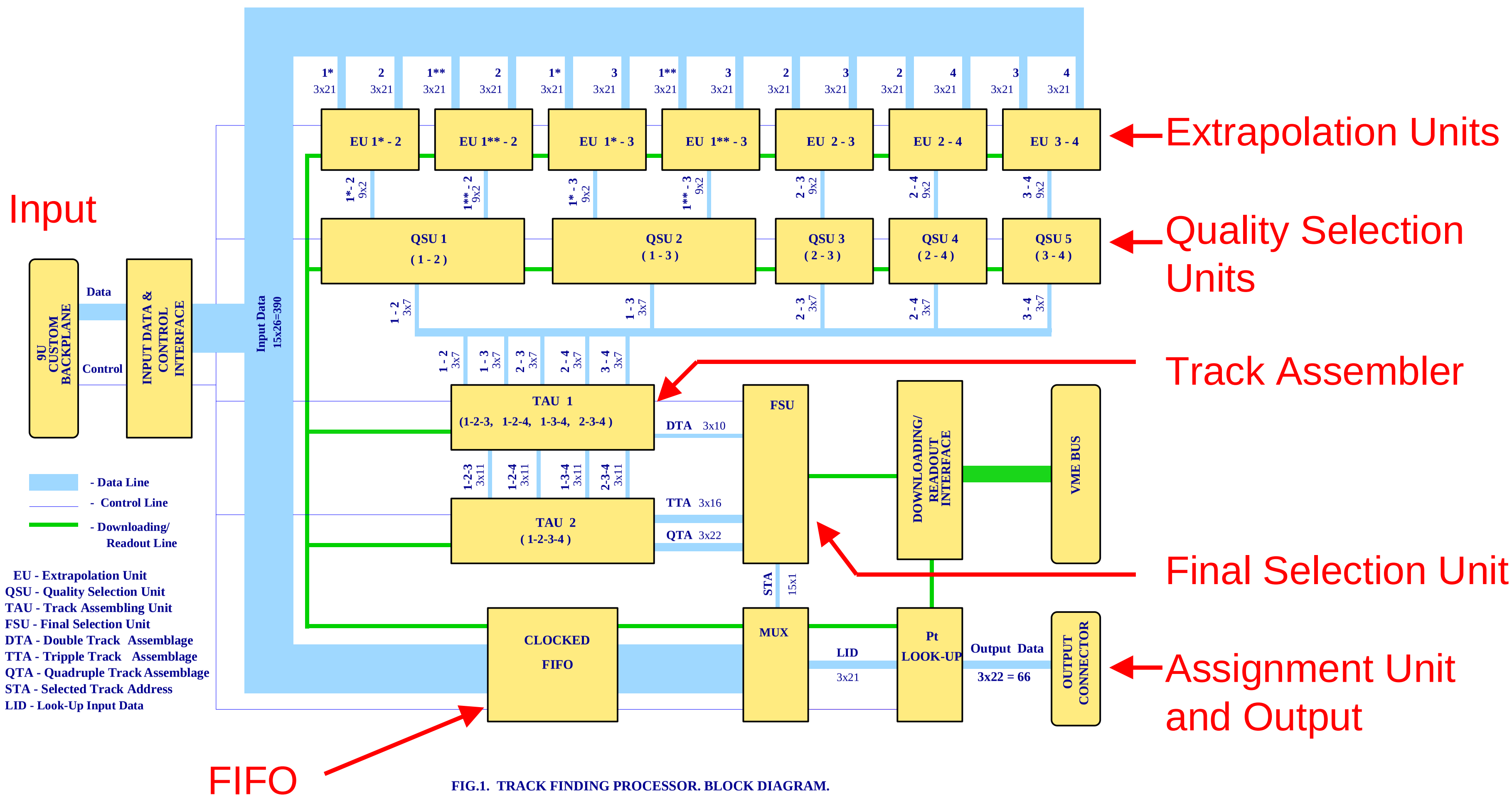
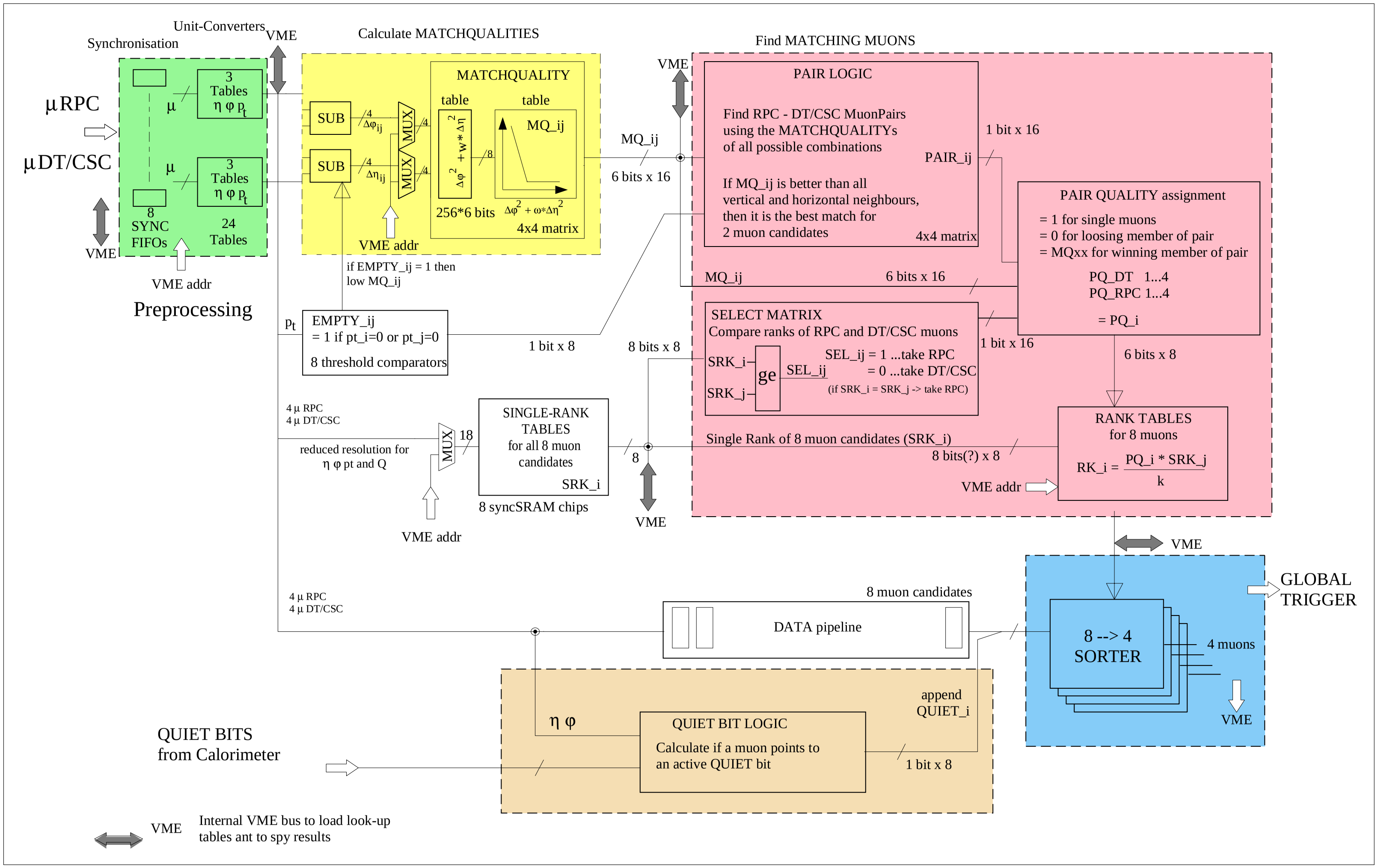


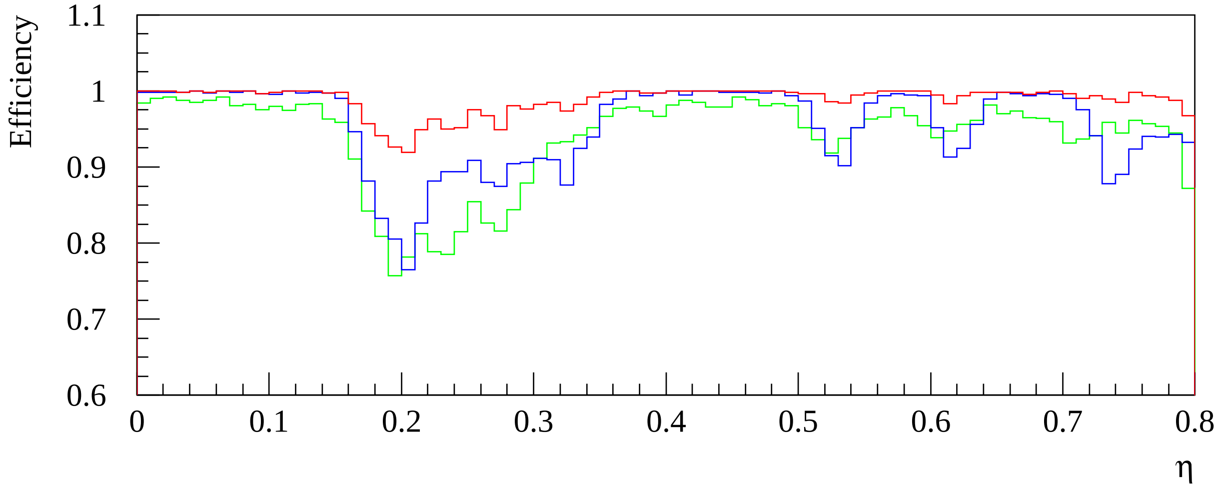
FIG.1. TRACK FINDING PROCESSOR. BLOCK DIAGRAM.

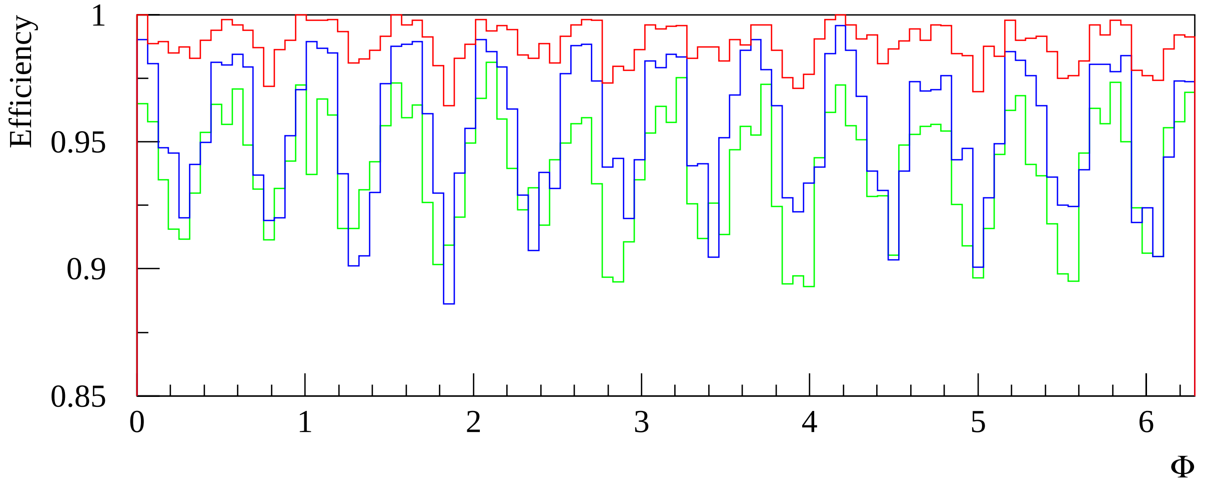
NOVEMBER, 2nd.

GMT: Present Design



Global Muon Trigger





Trigger efficiency [%] for 1 μ events

|η|<0.8	0 μ	1 μ	>1 μ
RPC	4.49 ±0.10	95.49 ±0.61	0.02 ±0.01
DT	6.08 ±0.11	93.70 ±0.60	0.22 ±0.02
GMT	1.04 ±0.05	98.78 ±0.70	0.18 ±0.02

Trigger efficiency [%] for 2 μ events

|η|<0.8	0 μ	1 μ	2 μ	>2 μ
RPC	0.24 ±0.03	8.98 ±0.22	90.72 ±0.93	0.05 ±0.02
DT	0.39 ±0.04	12.75 ±0.27	86.40 ±0.90	0.46 ±0.05
GMT	0.00 ±0.01	2.70 ±0.12	96.87 ±0.98	0.42 ±0.05

Muon and Calorimeter Trigger Rates

LV2 input 100 kHz / safety factor 3 = LV1 output 15+15 kHz

	$L = 10^{33} cm^{-2}s^{-1}$			$L = 10^{34} cm^{-2}s^{-1}$		
trigger type	**threshold [GeV]**	**rate [kHz] indiv.**	**rate [kHz] cumul.**	**threshold [GeV]**	**rate [kHz] indiv.**	**rate [kHz] cumul.**
ΣE_t	150	1.0	1.0	400	0.5	0.5
E_t^{miss}	40	2.1	2.8	80	1.3	1.7
e	12	10.3	12.3	25	6.8	8.3
e e	7	1.5	13.1	12	1.5	9.5
j	50	2.0	13.5	100	2.1	10.7
j j	30	1.6	13.9	60	2.2	11.6
j j j	20	1.0	14.1	30	3.2	13.3
j j j j	15	0.7	14.2	20	3.0	14.3
e j	9, 15	6.0	15.2	12, 50	1.4	14.9
μ	7	7.0	7.0	20	7.8	7.8
$\mu\ \mu$	2-4	0.5	7.3	4	1.6	9.2
μ e/γ	2-4, 7	2.4	9.2	4, 8	5.5	14.4
$\mu\ e_b$	2-4, 4	5.2	12.8			
μ j	2-4, 10	4.2	14.4	4, 40	0.3	14.3
$\mu\ E_t^{miss}$	2-4, 40	0.2	14.4	4, 60	1.0	15.3
$\mu\ \Sigma E_t$	2-4, 100	0.7	14.4	4, 250	0.2	15.3

LV2 input 75 kHz / safety factor 3 = LV1 output 12+12 kHz

μ	7	7.0	7.0
$\mu\ \mu$	2-4	0.5	7.3
μ e/γ	2-4, 7	2.4	9.2
$\mu\ e_b$	2-4, 4.5	3.3	11.1
μ j	2-4, 15	2.0	11.9
$\mu\ E_t^{miss}$	2-4, 40	0.2	11.9
$\mu\ \Sigma E_t$	2-4, 100	0.7	11.9

LV1 output rate is reduced to the required limit by adjusting the trigger thresholds

threshold 2-4 GeV means the minimal possible muon p_t cut ~4 GeV in the barrel, ~2 GeV in the endcap

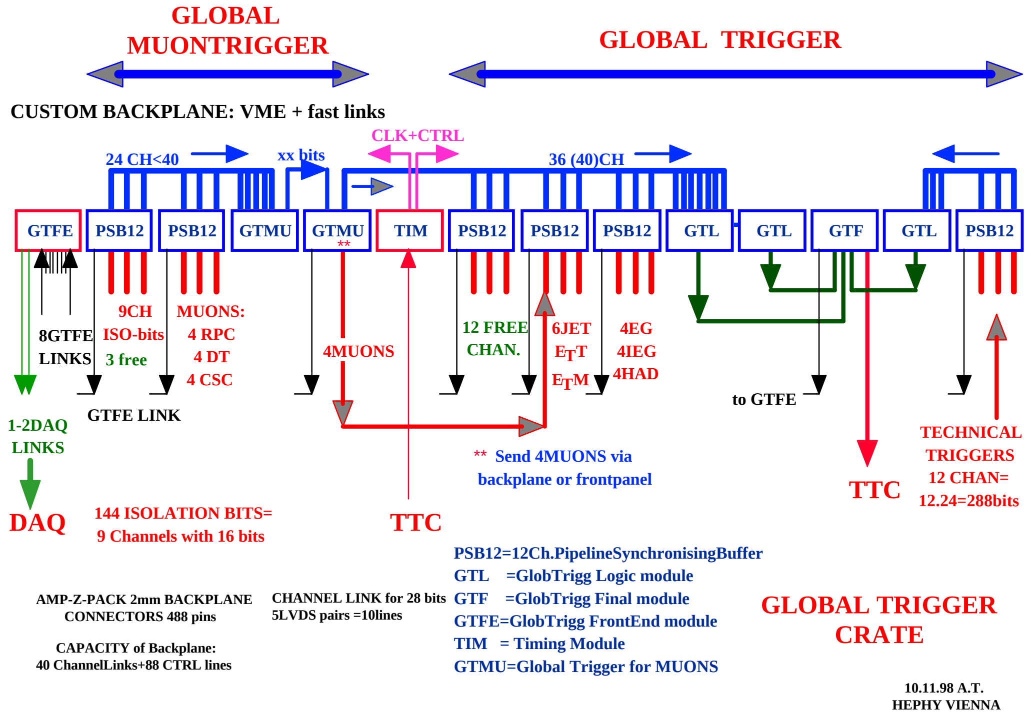
Global Trigger System

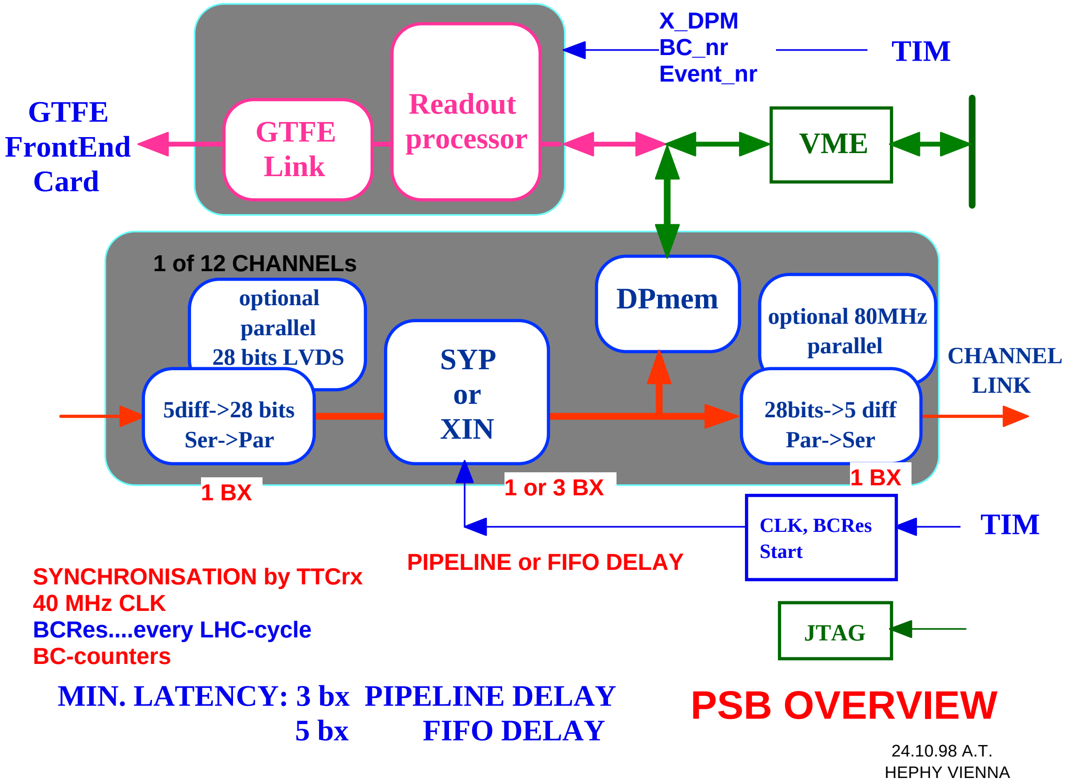
Final level-1 decision logic

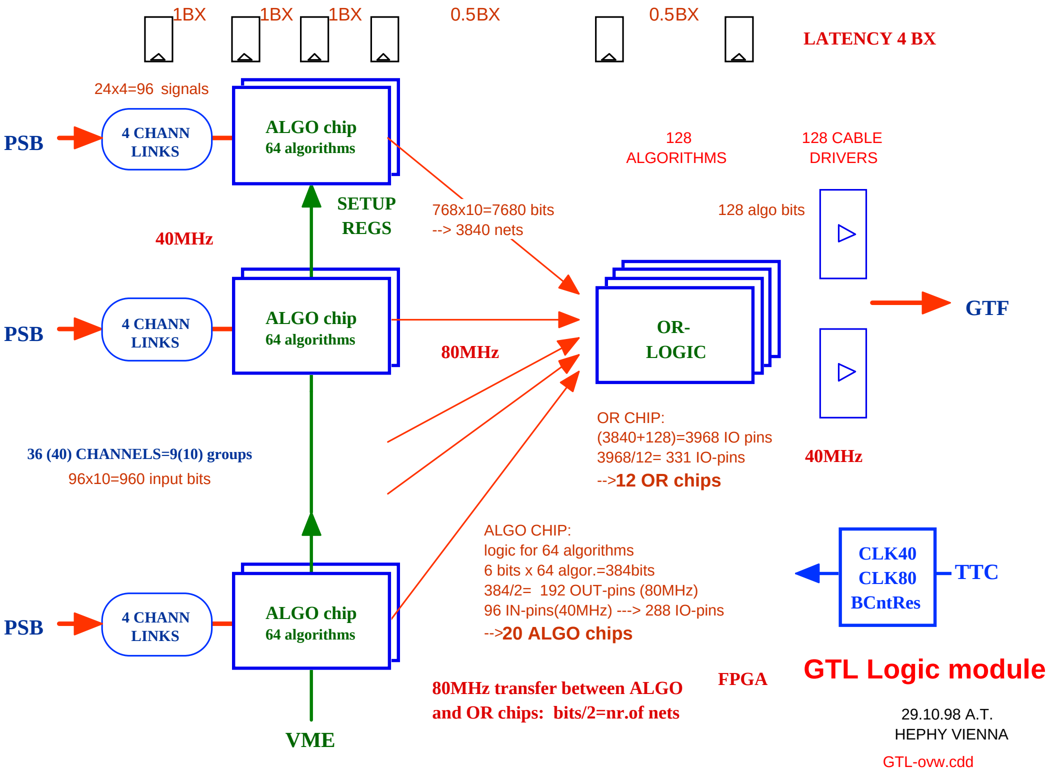
- **32 inputs with energy, coordinate, quality bits**
  - 4 muons, 4 isolated e/γ, 4 non-isolated e/γ
  - 6 jets & total number of jets above threshold
  - Total E_T, Missing E_T
- **128 Output Triggers**
  - example:
    1 μ > 20 GeV & 1 isolated e/γ > 10 GeV

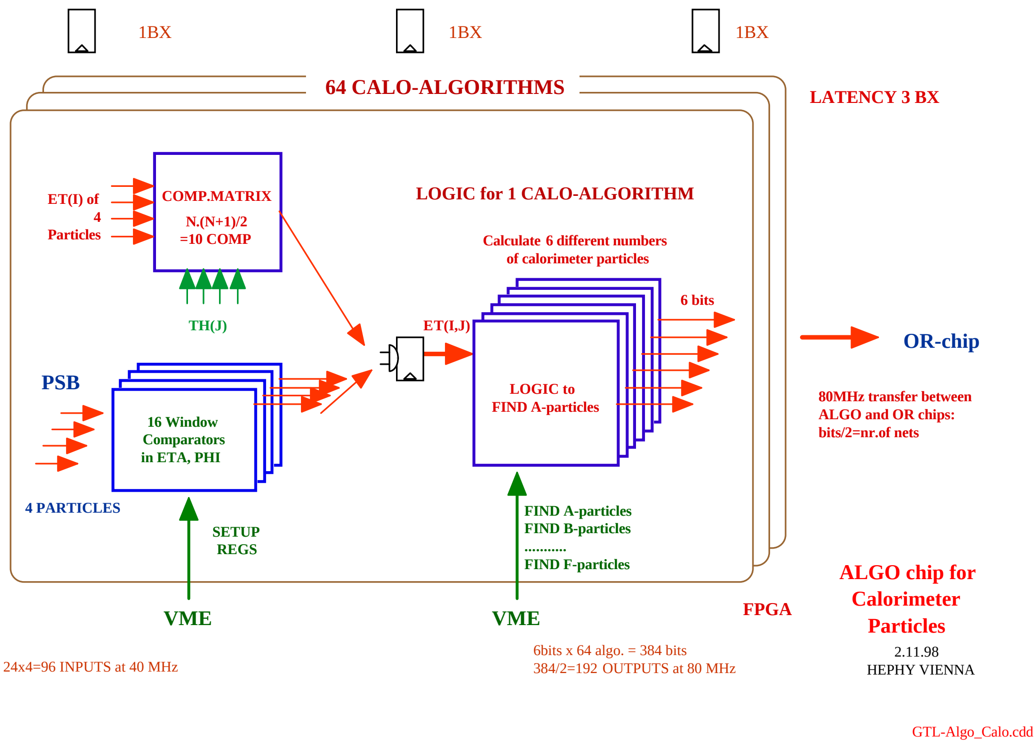
Cards:

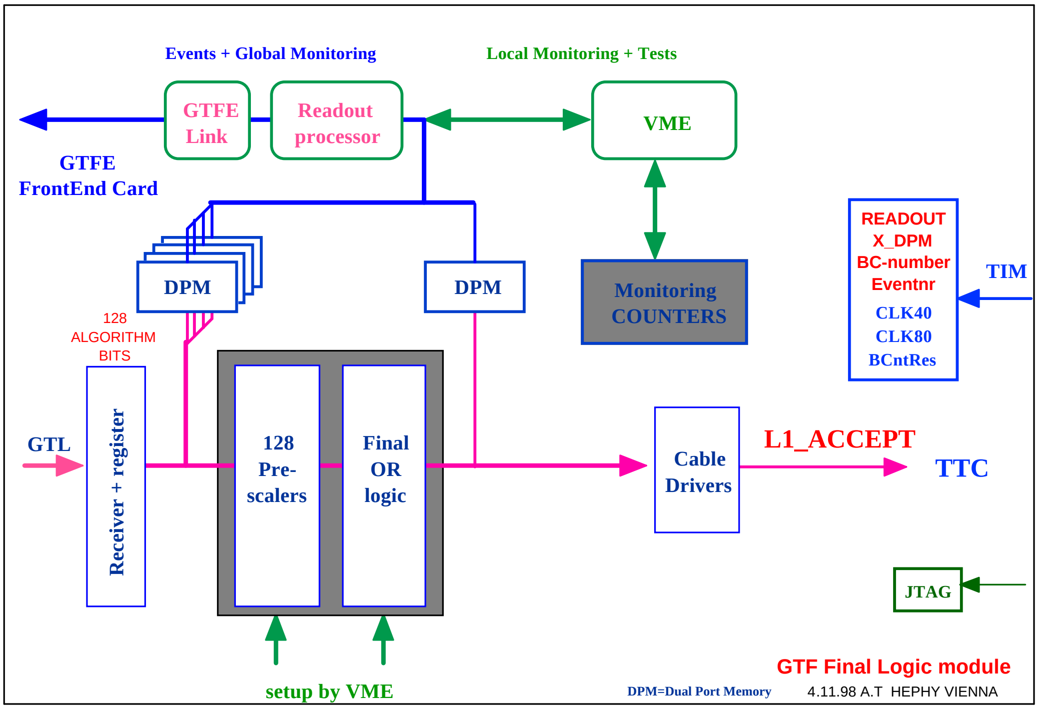
- **Pipeline Synchronizer & Buffer**
  - Aligns data from different subsystems
- **Global Trigger Logic**
  - Threshold & Comparator stages
  - Cuts on E_T, p_T, quality, η
- **Global Trigger Final**
  - Combinatorial logic array
  - Prescales


GLOBAL MUONTRIGGER
GLOBAL TRIGGER
CUSTOM BACKPLANE: VME + fast links
CLK+CTRL
24 CH<40
xx bits
36 (40)CH
GTFE
PSB12
PSB12
GTMU
GTMU
**
TIM
PSB12
PSB12
PSB12
GTL
GTL
GTF
GTL
PSB12
8GTFE
LINKS
9CH
ISO-bits
3 free
MUONS:
4 RPC
4 DT
4 CSC
4MUONS
12 FREE
CHAN.
6JET
E_TT
E_TM
4EG
4IEG
4HAD
to GTFE
1-2DAQ
LINKS
GTFE LINK
** Send 4MUONS via
backplane or frontpanel
TECHNICAL
TRIGGERS
12 CHAN=
12.24=288bits
TTC
DAQ
144 ISOLATION BITS=
9 Channels with 16 bits
TTC
PSB12=12Ch.PipelineSynchronisingBuffer
GTL =GlobTrigg Logic module
GTF =GlobTrigg Final module
GTFE=GlobTrigg FrontEnd module
TIM = Timing Module
GTMU=Global Trigger for MUONS
AMP-Z-PACK 2mm BACKPLANE
CONNECTORS 488 pins
CHANNEL LINK for 28 bits
5LVDS pairs =10lines
CAPACITY of Backplane:
40 ChannelLinks+88 CTRL lines
GLOBAL TRIGGER
CRATE
10.11.98 A.T.
HEPHY VIENNA

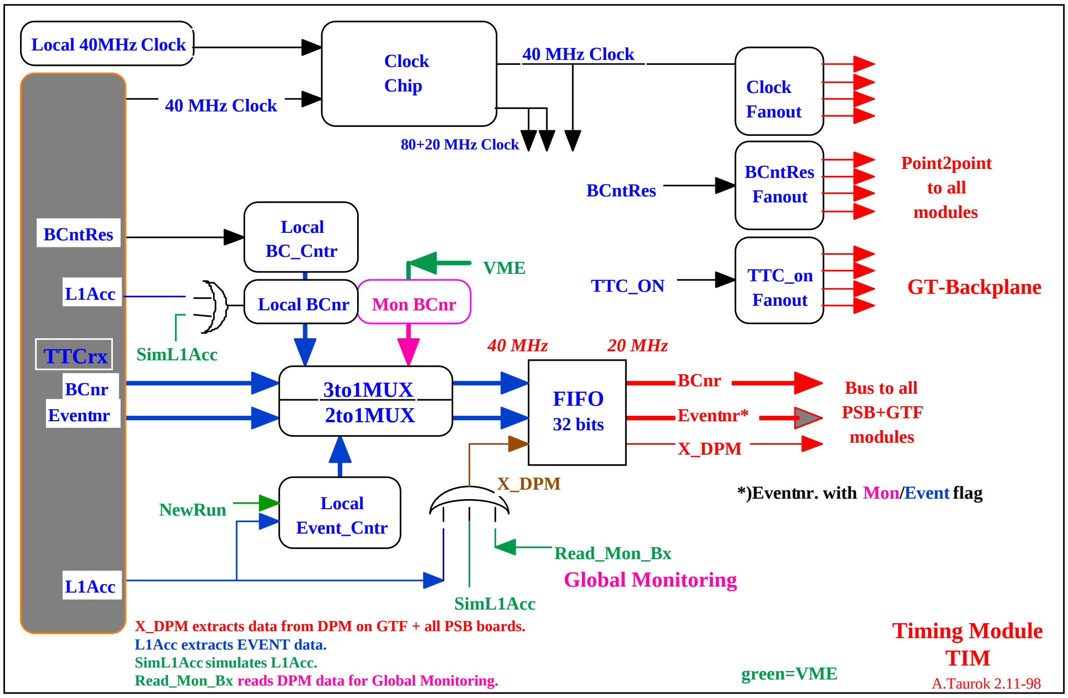

X_DPM
BC_nr
Event_nr
TIM
GTFE
FrontEnd
Card
GTFE
Link
Readout
processor
VME
1 of 12 CHANNELs
optional
parallel
28 bits LVDS
DPmem
optional 80MHz
parallel
CHANNEL
LINK
5diff->28 bits
Ser->Par
SYP
or
XIN
28bits->5 diff
Par->Ser
1 BX
1 or 3 BX
1 BX
CLK, BCRes
Start
TIM
PIPELINE or FIFO DELAY
JTAG
SYNCHRONISATION by TTCrx
40 MHz CLK
BCRes....every LHC-cycle
BC-counters
MIN. LATENCY: 3 bx PIPELINE DELAY
5 bx FIFO DELAY
PSB OVERVIEW
24.10.98 A.T.
HEPHY VIENNA


1BX
1BX
1BX
0.5BX
0.5BX
LATENCY 4 BX
24x4=96 signals
PSB
4 CHANN LINKS
ALGO chip
64 algorithms
SETUP REGS
40MHz
768x10=7680 bits
--> 3840 nets
128 ALGORITHMS
128 CABLE DRIVERS
128 algo bits
80MHz
OR- LOGIC
GTF
OR CHIP:
(3840+128)=3968 IO pins
3968/12= 331 IO-pins
-->12 OR chips
40MHz
36 (40) CHANNELS=9(10) groups
96x10=960 input bits
ALGO CHIP:
logic for 64 algorithms
6 bits x 64 algor.=384bits
384/2= 192 OUT-pins (80MHz)
96 IN-pins(40MHz) ---> 288 IO-pins
-->20 ALGO chips
CLK40
CLK80
BCntRes
TTC
FPGA
GTL Logic module
80MHz transfer between ALGO and OR chips: bits/2=nr.of nets
VME
29.10.98 A.T.
HEPHY VIENNA
GTL-ovw.cdd


1BX
1BX
1BX
64 CALO-ALGORITHMS
LATENCY 3 BX
ET(I) of 4 Particles
COMP.MATRIX
N.(N+1)/2
=10 COMP
LOGIC for 1 CALO-ALGORITHM
Calculate 6 different numbers of calorimeter particles
6 bits
TH(J)
ET(I,J)
PSB
16 Window Comparators in ETA, PHI
LOGIC to FIND A-particles
OR-chip
80MHz transfer between ALGO and OR chips: bits/2=nr.of nets
4 PARTICLES
SETUP REGS
FIND A-particles
FIND B-particles
....
FIND F-particles
VME
VME
FPGA
ALGO chip for Calorimeter Particles
2.11.98
HEPHY VIENNA
24x4=96 INPUTS at 40 MHz
6bits x 64 algo. = 384 bits
384/2=192 OUTPUTS at 80 MHz
GTL-Algo_Calo.cdd

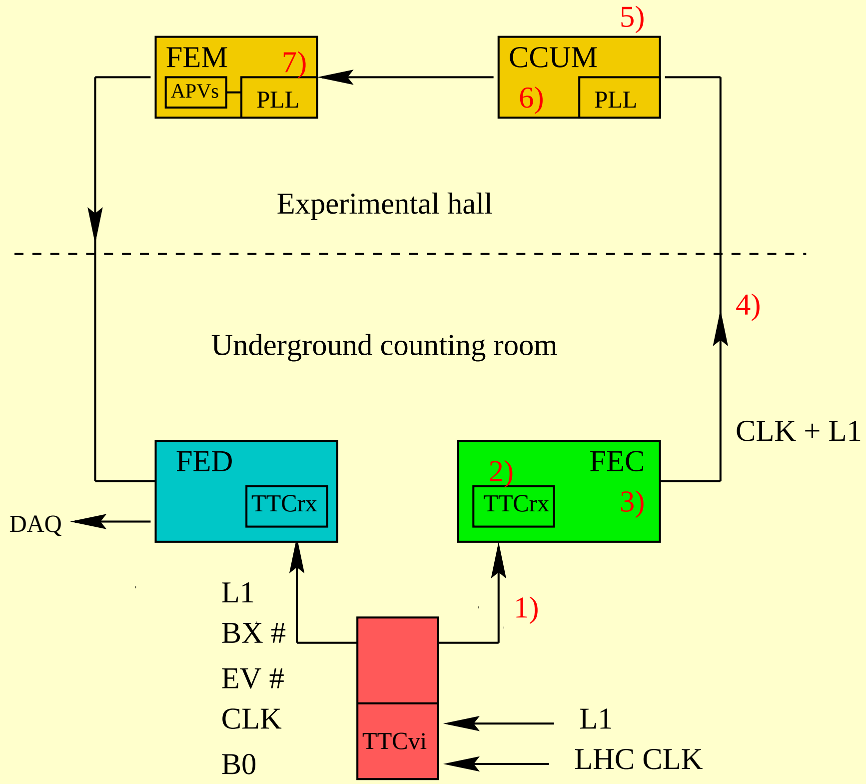


GTF-ovw.cdd



TIM-Ovw.cdd

Distribution of CLK and L1 to Front–End



L1 delay along the critical path TTCvi → FEM:

1) **TTCvi (input) → TTCrx (output): ≃ 135ns + 5ns/m (10 BX with 20m fibre)**

2) **TTCrx on FEC: programmable delay, foreseen to be set to zero**

3) **FEC, opto→electrical conversion: < 50ns (< 2 BX)**

4) **FEC → CCUMs: 90 to 120 m optical fibre → 450 to 600 ns (18 to 24 BX)**

5) **Ring of CCUMs: ≃ 2m of electrical cables → ≃ 20ns (< 1 BX)**

6) **CCUM: opto→electrical conversion + distribution via electrical cables to the PLLs in the FE + (CLK+L1) decoding → ≃ 75ns (3 BX) (?)**

7) **PLL on the FEM: programmable (fine and coarse) delay**

Impact on the latency

Heavy Ion Luminosity and trigger rates

Initial luminosities for 1 experiment, 125 ns bunch spacing

	pp	**O O**	**Ca Ca**	**Nb Nb**	**Pb Pb**
luminosity [$cm^{-2}s^{-1}$]	10^{34}	$3.2 \cdot 10^{31}$	$2.5 \cdot 10^{30}$	$9 \cdot 10^{28}$	10^{27}
average collision rate [kHz]	550 000	32 000	5200	400	7.6
1μ trigger rate [kHz]	190	120	53	10	0.5

- **bunch spacing 25 ns ⇒ luminosity × 4-5** (not possible for Pb-Pb)
- **2 experiments ⇒ luminosity / 3-4**
- **3 experiments ⇒ luminosity / 6-9**

Pb Pb: experiments	**1**	**2**	**3**
luminosity [$cm^{-2}s^{-1}$]	10^{27}	$3.3 \cdot 10^{26}$	$1.7 \cdot 10^{26}$
average collision rate [Hz]	7600	2500	1300
1μ trigger rate [Hz]	500	165	85
2μ trigger rate [Hz]	60	20	10

Heavy Ion Trigger Summary

- **The p_t spectra above 1 GeV in AA collisions at $\sqrt{s}$ = 5-7 TeV are not much different from those in pp collisions at $\sqrt{s}$ = 14 TeV**

- **Simple scaling by $A^{2 \cdot 0.95}$ works well**

- **Thus one can use a lot of predictions calculated for the pp case**
  - For example one gets Pb-Pb rates at $L=10^{27} cm^{-2}s^{-1}$ multiplying pp rates at $L=10^{34} cm^{-2}s^{-1}$ by 0.0025

- **For Pb-Pb at $L=10^{27} cm^{-2}s^{-1}$ one can expect single muon trigger rate:**
  - **210 Hz** from prompt muons *(c- and b-quark decays)*
  - **280 Hz** from hadronic punchthrough and decays *(mainly π and K)*

Strategy for dimuon trigger

Assumptions

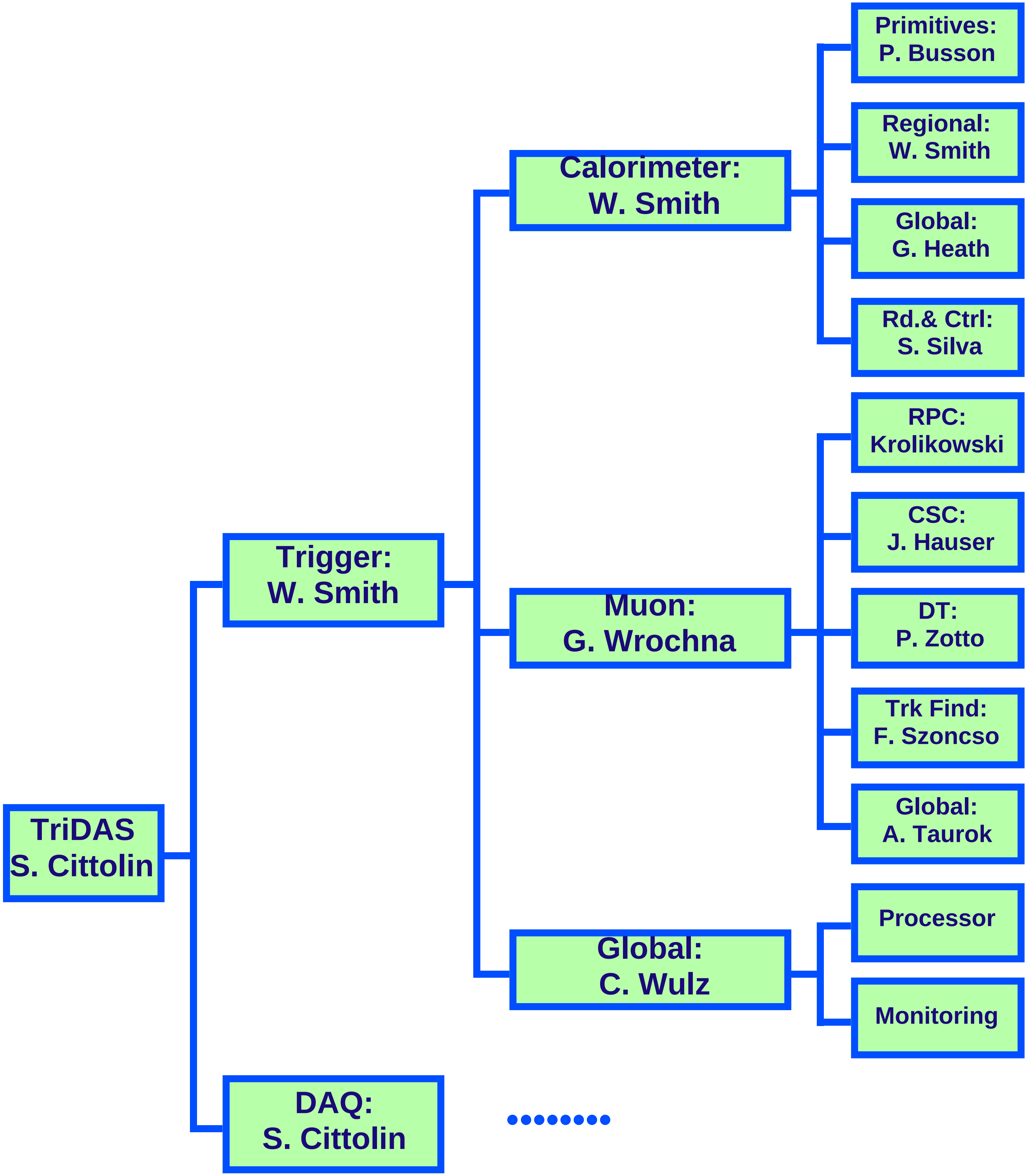
- $L=10^{27}cm^{-2}s^{-1}$ (1 experiment running at the time) for Pb-Pb
- mass storage capacity: ~100 MB/s
- equal rates for muon and calorimeter triggers
- max. event size (central collisions):

Detector	Occupancy	k Bytes
Pixel barrel	**< 0.5 %**	**300**
MSGC 4 layers + 4 disks	**~ 10 %**	**826**
ECAL full (1 time slice)	**100 %**	**260**
HCAL full	**100 %**	**28**
Muon DT+CSC+RPC	**< 0.1 %**	**54**
TOTAL		**~1.5 MB**

Trigger strategy

- **Require single muon trigger** ($|\eta|<1.5$) **at the first level** $\Rightarrow$ **500 Hz**
- **Search for a second muon** ($|\eta|<1.5$) **at the second level** $\Rightarrow$ **60 Hz**
- **Little or no reduction needed at higher levels**

CMS Trigger Organization



Trigger cost book 9

	CMS Cost Estimate - Version 9		Release Date: March 31, 1998			
No.	Item	Unit Type	# Units	Unit Cost	Total Cost	
6.1.1	**CALORIMETER TRIGGER**				5225	0
6.1.1.1	Regional trigger	System	1	4050.020	4050	
6.1.1.2	Global Cal. Trigger	System	1	400.000	400	
6.1.1.3	Readout & Control	System	1	255.000	255	
6.1.1.4	Data Communication	System	1	520.000	520	
6.1.2	**CSC TRIGGER**				1100	0
6.1.2.1	Muon Port Card	Board	63	7.475	471	
6.1.2.2	Sector Receivers	Board	65	4.217	274	
6.1.2.3	Sector Processors	Board	15	7.020	102	
6.1.2.4	Overlap Processors	Board	15	7.020	105	
6.1.2.5	Clock and Control Card	Board	12	5.233	63	
6.1.2.6	Crate Monitor Card	Board	10	1.300	13	
6.1.2.7	Trigger Crate	Crate	10	7.107	71	
6.1.2.7	Institute Manpower	Manyears	0	0.000	0	
6.1.3	**DT TRIGGER**				780	0
6.1.3.1	Trigger Crate	Crate	4	6.000	24	
6.1.3.2	Sector Processor Card	Board	60	8.000	480	
6.1.3.3	Muon Sorter Card	Board	5	8.000	40	
6.1.3.4	Clock and Control Card	Board	4	4.000	16	
6.1.3.5	Crate Monitor Card	Board	4	2.000	8	
6.1.3.6	Cables	Cables	1	50.000	50	
6.1.3.7	Readout and Control	System	1	32.000	32	
6.1.3.8	Monitoring and Test	System	1	70.000	70	
6.1.3.9	Prototypes and spares	System	1	60.000	60	
6.1.3.10	Institute Manpower	Manyears	0	0.000	0	0
6.1.4	**RPC TRIGGER**				3695	0
6.1.4.1	Link Board	Board	936	0.475	445	
6.1.4.2	Data Communication	System	1	755.160	755	
6.1.4.3	Trigger Board (Barrel)	Board	156	3.830	597	
6.1.4.4	Trigger Board (EndCap)	Board	240	3.350	804	
6.1.4.5	Final Sorter Board	Board	33	1.600	53	
6.1.4.6	Readout board	Board	396	0.700	277	
6.1.4.7	Readout Concentrator Board	Board	33	1.000	33	
6.1.4.8	Clock Control Board	Board	33	4.000	132	
6.1.4.9	Trigger Crate	Crate	33	8.600	284	
6.1.4.10	Readout and Control	System	1	15.300	15	
6.1.4.11	ASICs Development	Service	1	200.000	200	
6.1.4.12	Prototypes and spares	System	1	100.000	100	
6.1.4.13	Institute Manpower	Manyears	0	0.000	0	0
6.1.5	**GLOBAL TRIGGER**				1340	0
6.1.5.1	Global Trigger Crate	Crate	1	27.046	27	
6.1.5.2	PipelineSyncBuffer	Board	5	8.290	41	
6.1.5.3	Global Trigger Logic	Board	5	12.168	61	
6.1.5.4	Global Trigger Final	Board	1	5.199	5	
6.1.5.5	Cables	Cables	1	4.070	4	
6.1.5.6	Global Muon Trigger	System	1	158.272	158	
6.1.5.7	Readout and Control	System	1	30.000	30	
6.1.5.8	Prototypes	System	1	32.700	33	
6.1.5.9	Monitoring & Test	System	1	80.000	80	
6.1.5.10	Trigger Throttle System	System	6000	0.150	900	
6.1.5.11	Institute Manpower	Manyears	0	0.000	0	0

Cost Detail Ex: Regional Cal. Trig $

M&S for Crates, Boards & Cables:

WBS	Item	Unit Cost	Number	Total
3.1.2.4	Power Supplies	3,600	22	79,200
3.1.2.5	Crates	600	22	13,200
3.1.2.6	Backplane	5,910	22	130,020
3.1.2.7	Clock & Control Card	2,960	22	65,120
3.1.2.8	Receiver Card	8,870	176	1,561,120
3.1.2.9	Electron ID Card	3,690	176	649,440
3.1.2.10	Jet Summary Card	4,670	22	102,740
3.1.2.11	Cables	$1/ft	7,300	7,300

Detail for Boards:

Card	Size	Board	Assmbl.	Parts	Total
Backplane	crate	1,000	300	4,610	5,910
Clock & Control	9Ux280mm	600	400	1,960	2,960
Receiver	9Ux400mm	800	650	7,420	8,870
Electron ID	9Ux280mm	400	300	2,990	3,960
Jet Summary	9Ux280mm	600	500	3,570	4,670

Detail for ASICS (WBS 3.1.2.2):

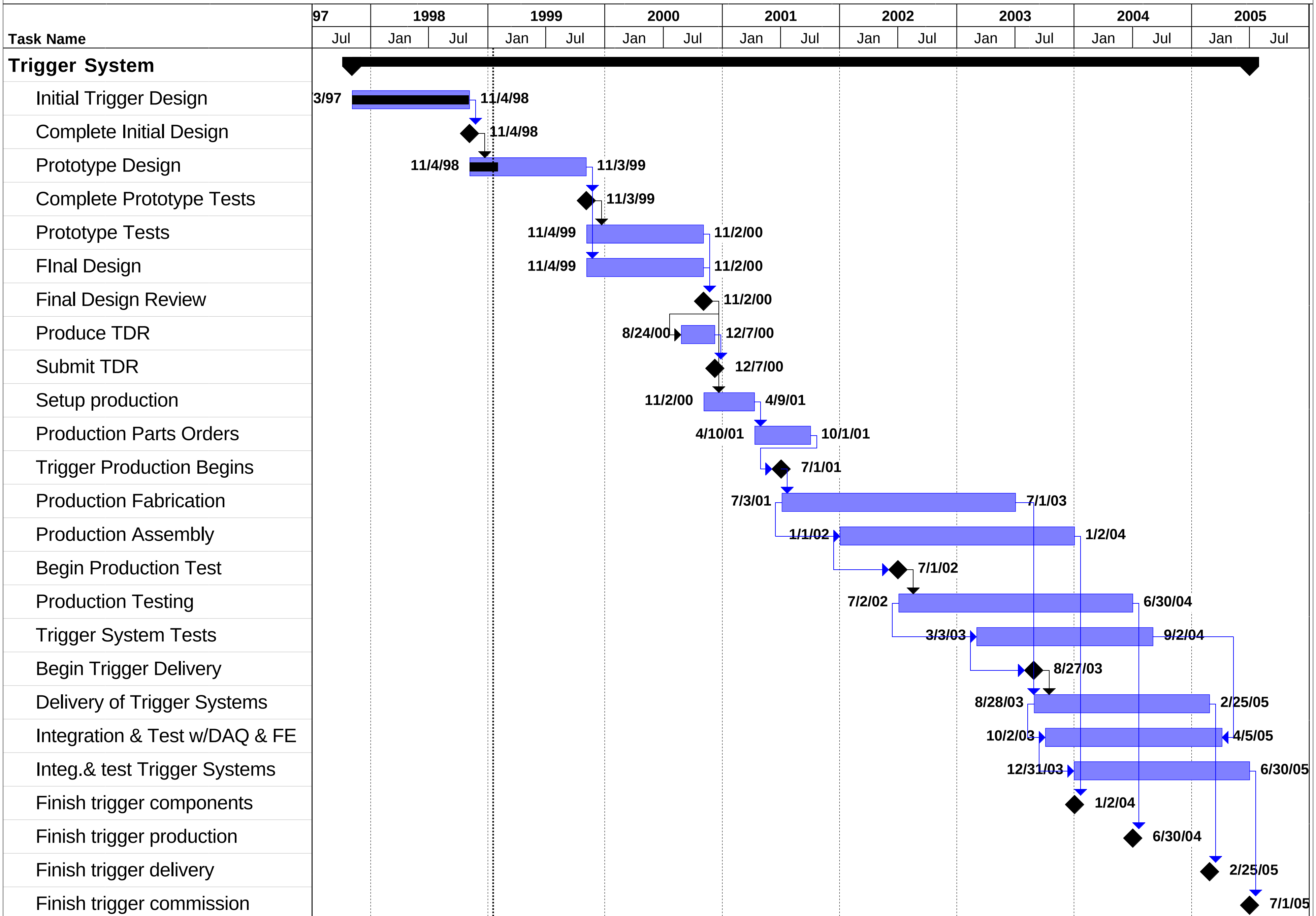
ASIC	NRE	Cst/Prt	#/RC	#/EIC	#/JSC	Tot.#
Adder (GaAs)	50,000	179	3	0	2	520
Phase (GaAs)	50,000	360	8	0	0	1,280
Sort (GaAs)	80,000	300	0	1	2	200
Electron ID(GaAs)	80,000	300	0	2	0	320
Bndry. Scan(GaAs)	50,000	150	1	1	1	340

(costs per part are included in board parts costs above)

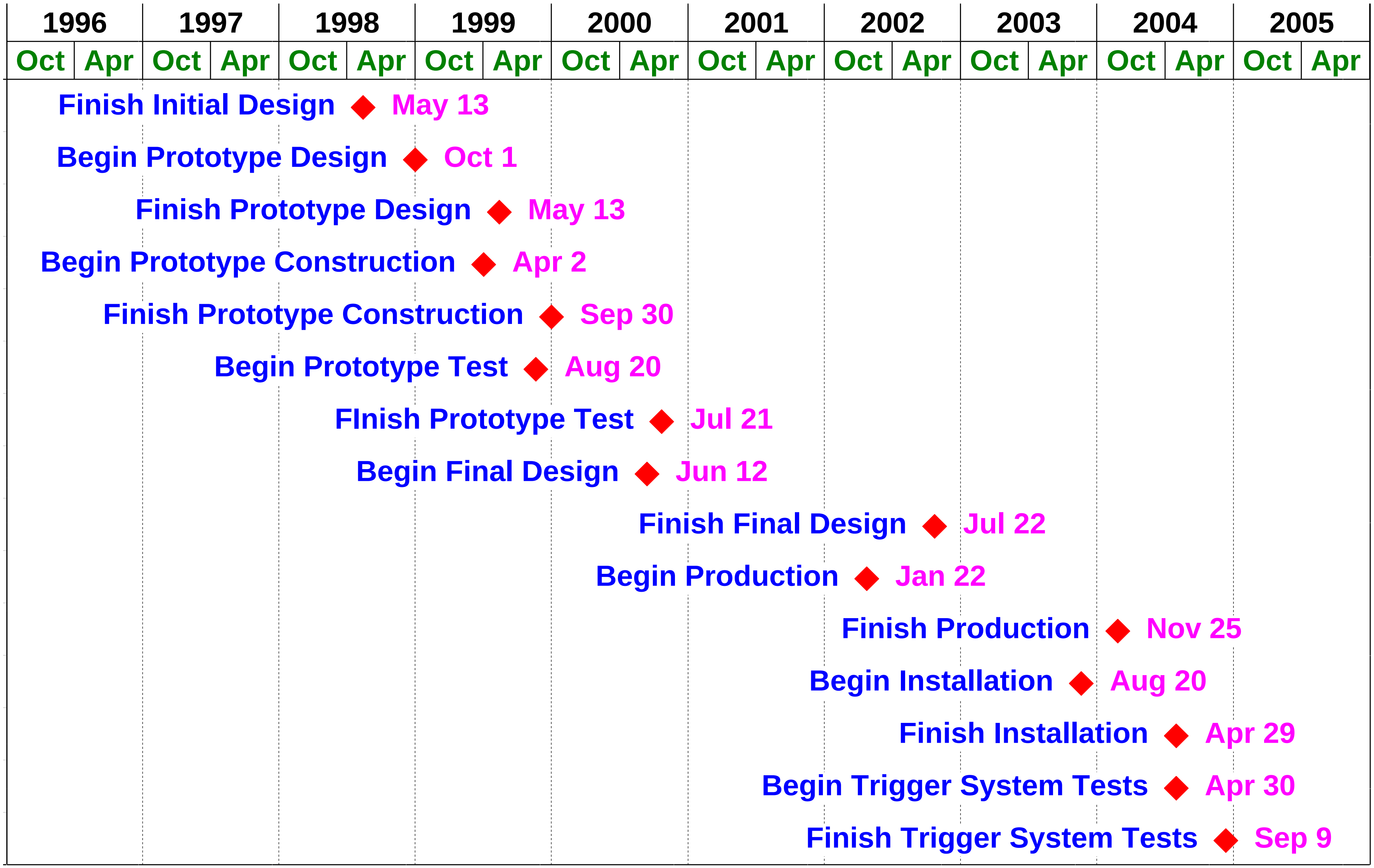
W. Smith, U. Wisconsin

CMS TRIGGER SCHEDULE

1/18/99



Ex: CSC Trigger Schedule



Trigger Milestone List

Level 1 (1998-2000)

- **Nov. 1998 Complete Initial Trigger Design:**
  - Algorithms finalized
  - Functional blocks determined
  - Numbers of ASICs, boards, cards and crates specified
  - Interfaces specified
  - Trigger geometry determined
- **Nov. 1999 Complete Phase 1 Prototype Design:**
  - Designs of boards, cards
  - ASICs for prototype tests done
- **Nov. 2000 Phase 1 Prototype Tests Finished:**
  - All tests necessary to begin design of production electronics are complete
- **Nov. 2000 Technical Design Report**

Level 2 (1998-2000)

- **Nov. 1998:**
  - Complete Initial Muon Trigger Design
  - Complete Initial Calorimeter Trigger Design
  - Complete Initial Global Trigger Design
- **Nov. 1999:**
  - Complete Prototype Muon Trigger Design
  - Complete Prototype Calorimeter Trigger Design
  - Complete Prototype Global Trigger Design
- **Nov. 2000:**
  - Prototype Muon Trigger Tests Finished
  - Prototype Calorimeter Trigger Tests Finished
  - Prototype Global Trigger Tests Finished

Trigger Milestone Progress

1998 L1 Milestone:

- **Nov. 1998 Complete Initial Trigger Design:**
  - Algorithms finalized
  - Functional blocks determined
  - Numbers of ASICs, boards, cards and crates specified
  - Interfaces specified
  - Trigger geometry determined
- **Status: Complete**

1998 L2 Milestones:

- **Nov. 1998:**
  - Complete Initial Muon Trigger Design
    - http://cmsdoc.cern.ch/ftp/afscms/TRIDAS/mutrig/html/
  - Complete Initial Calorimeter Trigger Design
    - http://cmsdoc.cern.ch/ftp/afscms/TRIDAS/caltrig/html/CalTrig.html
  - Complete Initial Global Trigger Design
    - http://sungraz.cern.ch/CMS/trigger/globalTrigger/Welcome.html
- **Status: Complete**

Trigger Project Management

CMS Annual Reviews

- **April: TriDAS Status**
  - Progress, draft R&D plans & expenses for next year
- **November: TriDAS Internal Review**
  - R&D Plans/Progress, Cost & Schedule, Milestones
  - Finalize R&D plans & expenses for next year
  - Internal CMS Review w/CMS referees
- **Internal Electronics Reviews by LHC Electronics Board CMS Reps.**
  - G. Hall (Imperial), G. Stefanini (CERN), J. Elias (FNAL) substituting for W. Smith (Wisc.)
  - Reports to CMS Management Board (last trigger review in Fall '98)

Conclusions - Trigger

Algorithms satisfy physics requirements

- **Active simulation program producing results**

Hardware design to implement algorithms

- **Full conceptual design with considerable engineering**
- **Extensive prototyping & test program**
  - "Proof of principle" of critical items
  - Number of successes already

Project Management

- **Experienced team in place with all tasks assigned**
- **Extensive system of reviews and monitoring in place**

Detailed documentation on WWW:

- **http://cmsdoc.cern.ch/ftp/afscms/TRIDAS/html/level1.html**