WBS 3.1.2 - Calorimeter Trigger

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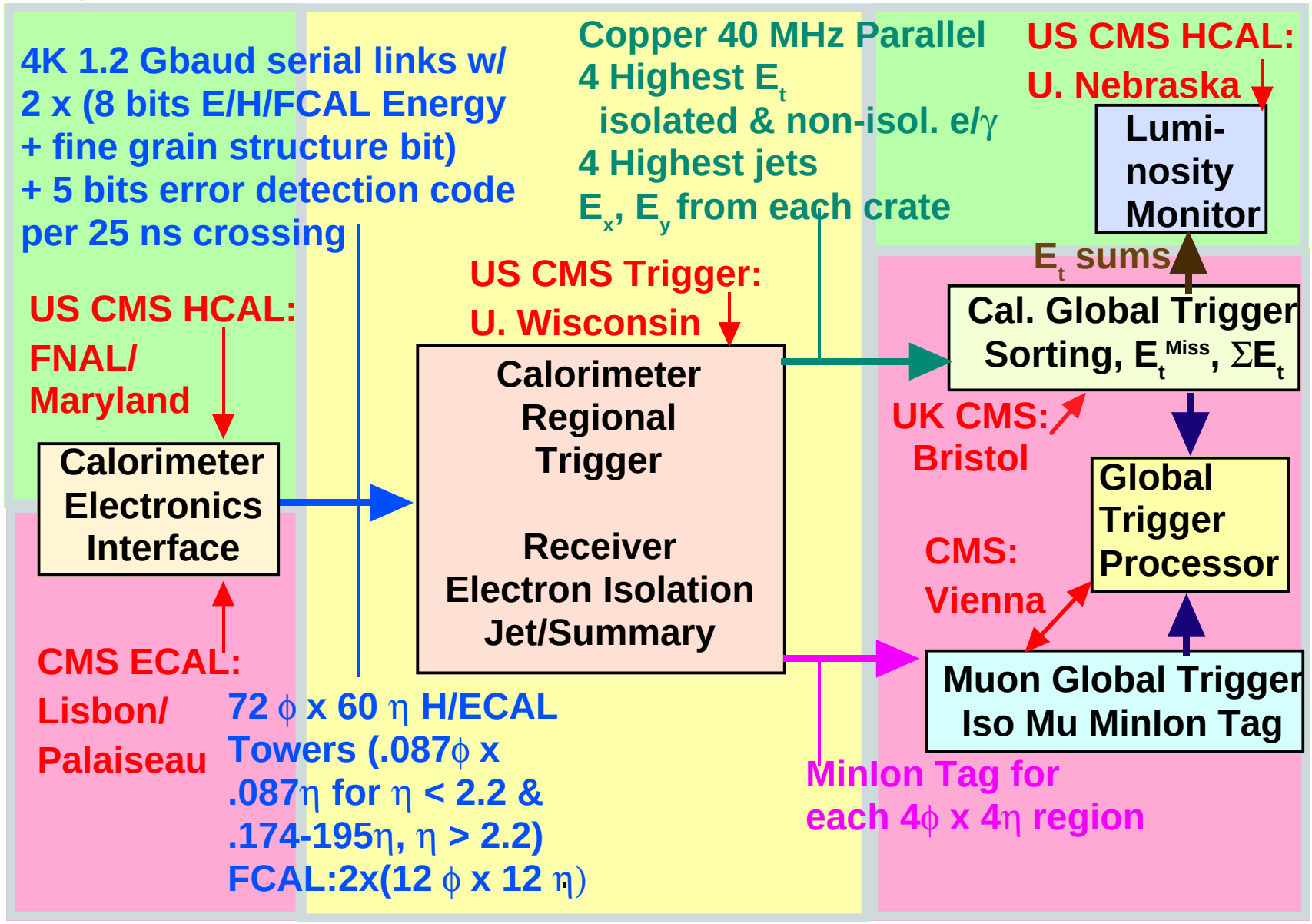
CMS Trigger Project Manager

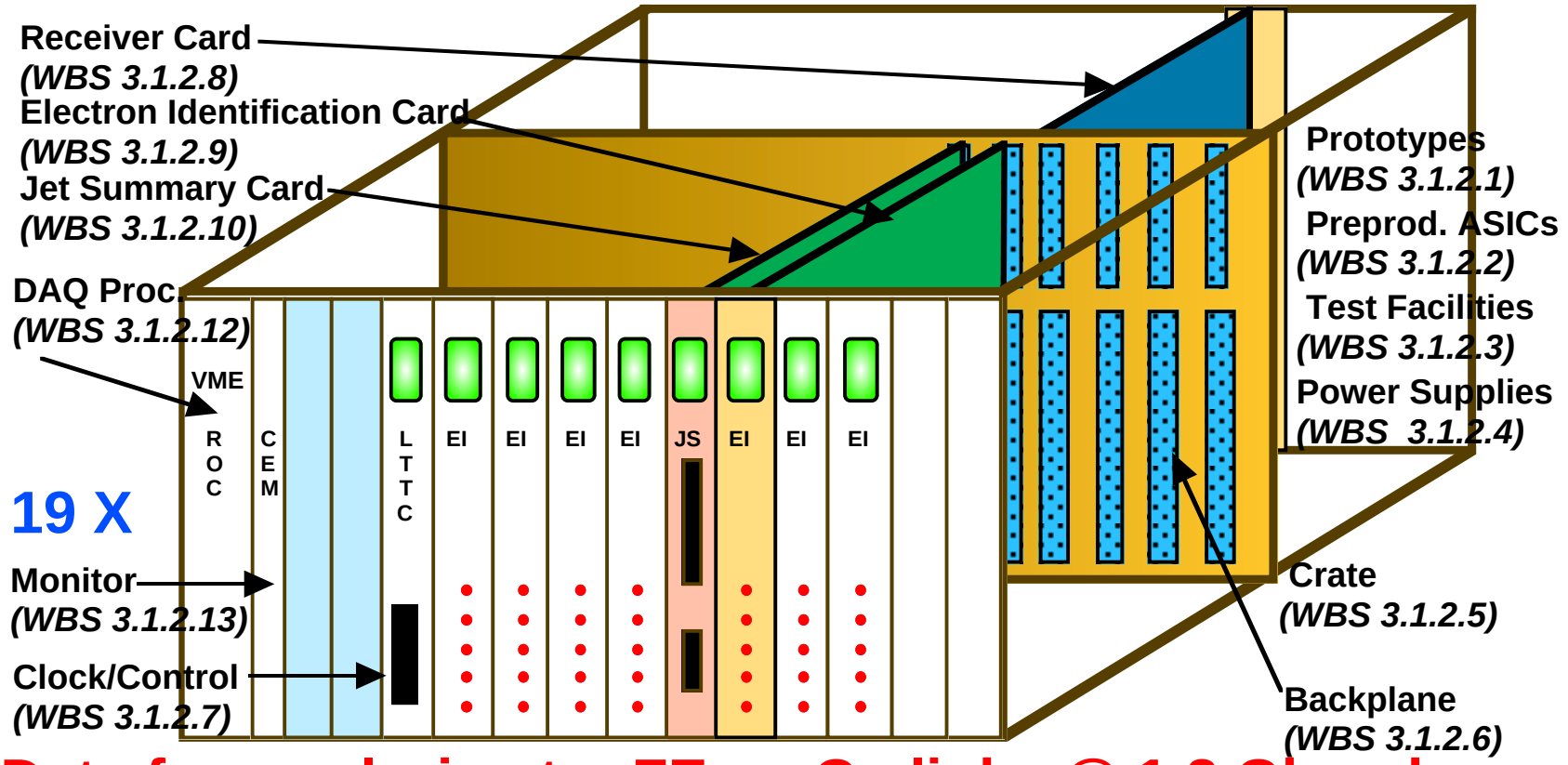
DOE/NSF Review
April 12, 2000

Calorimeter Trigger Overview



Regional Calorimeter Crate

(WBS 3.1.2)



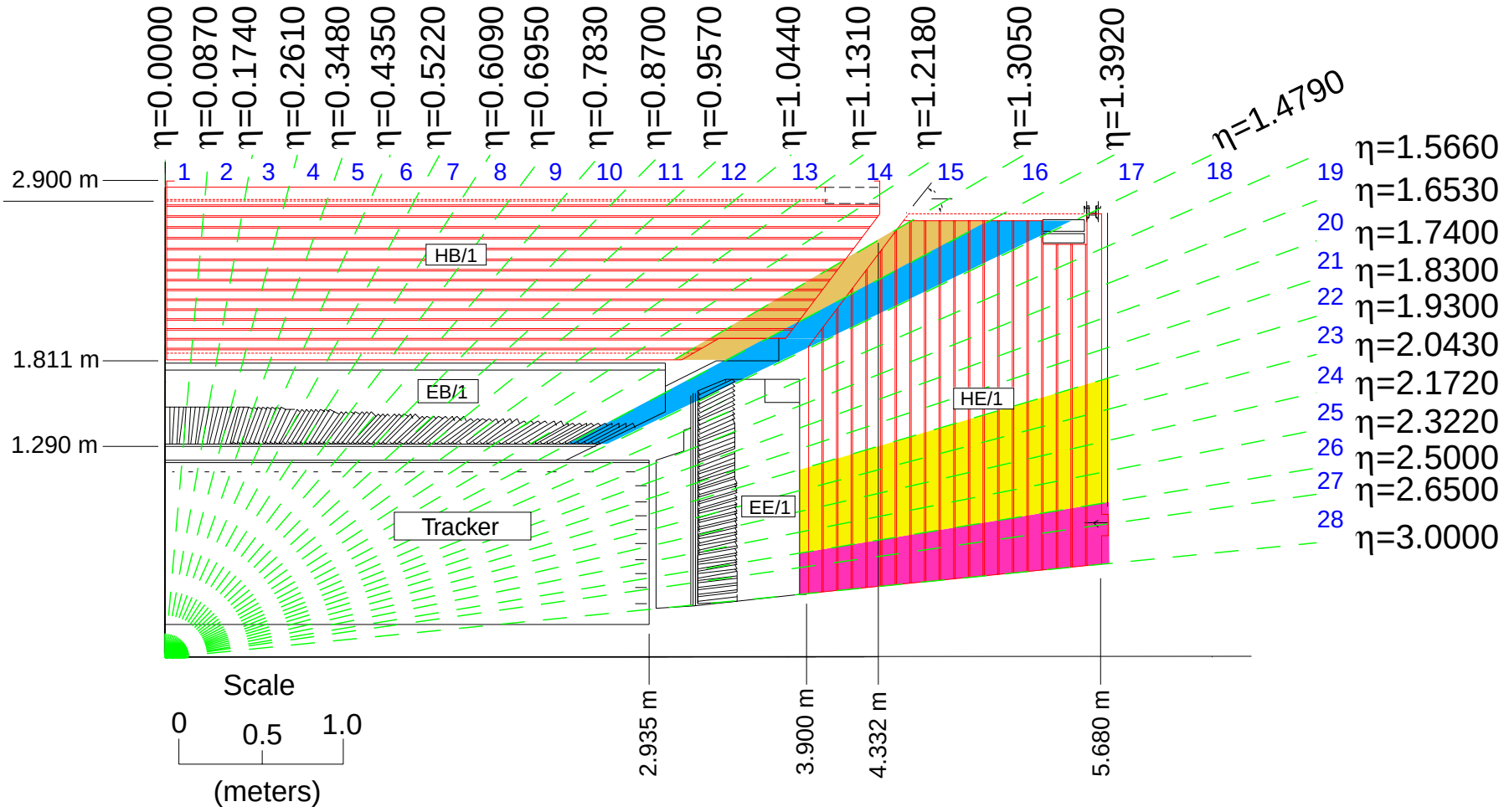
Data from calorimeter FE on Cu links @ 1.2 Gbaud (ptyp. tstd.)

- Into 133 rear-mounted Receiver Cards (ptyp. tstd. w/ ASICs)

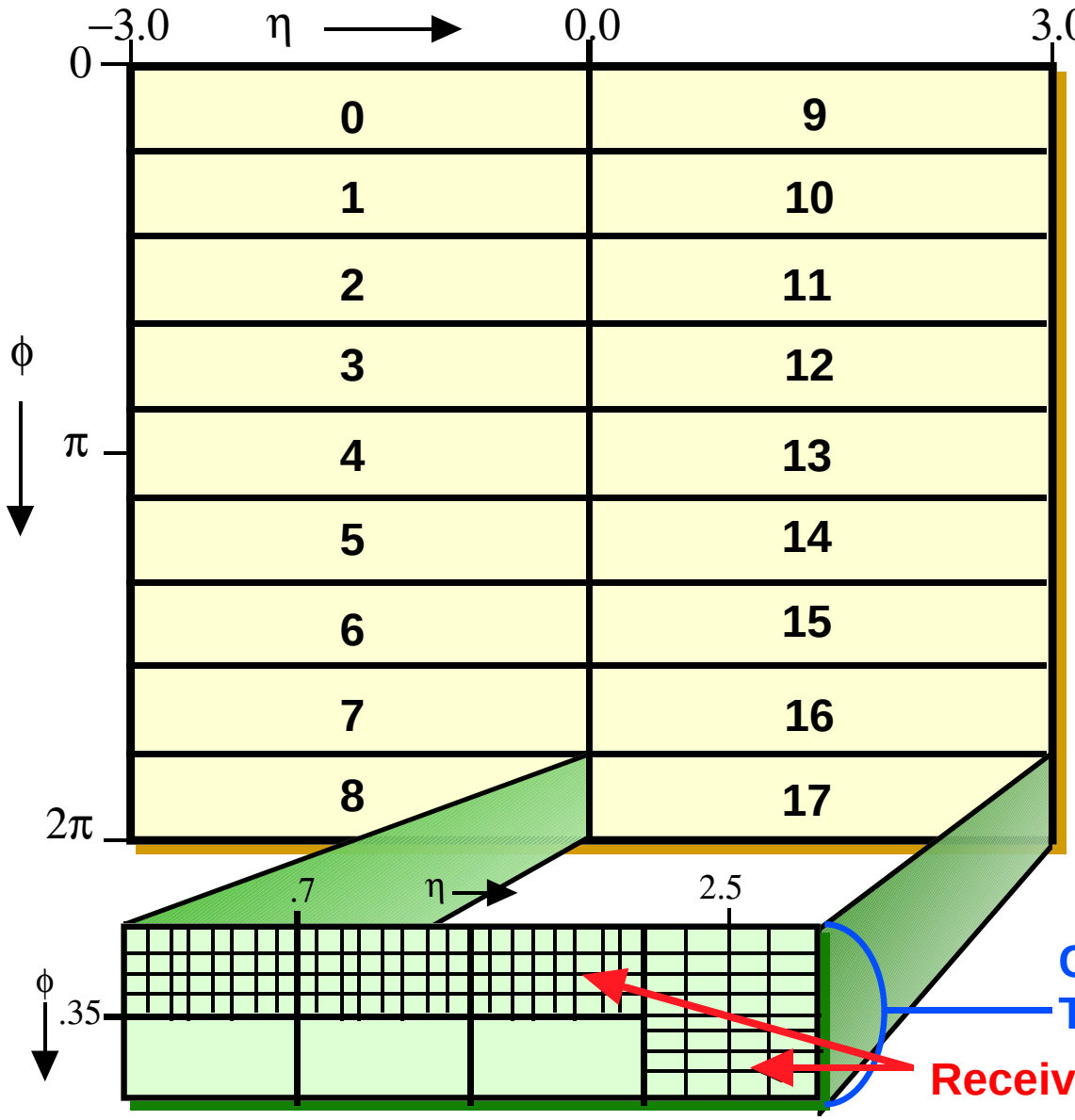
160 MHz point to point backplane (ptyp. tstd.)

- 19 Clock&Control (ptyp. tstd.), 133 Electron ID (ptyp. tstd.)
  19 Jet/Summary, Receiver Cards operate @ 160 MHz

Calorimeter Trigger Geometry



Cal. Trigger Tower Mapping



18 crates for barrel & endcap calorimeters + 1 for v. forward.

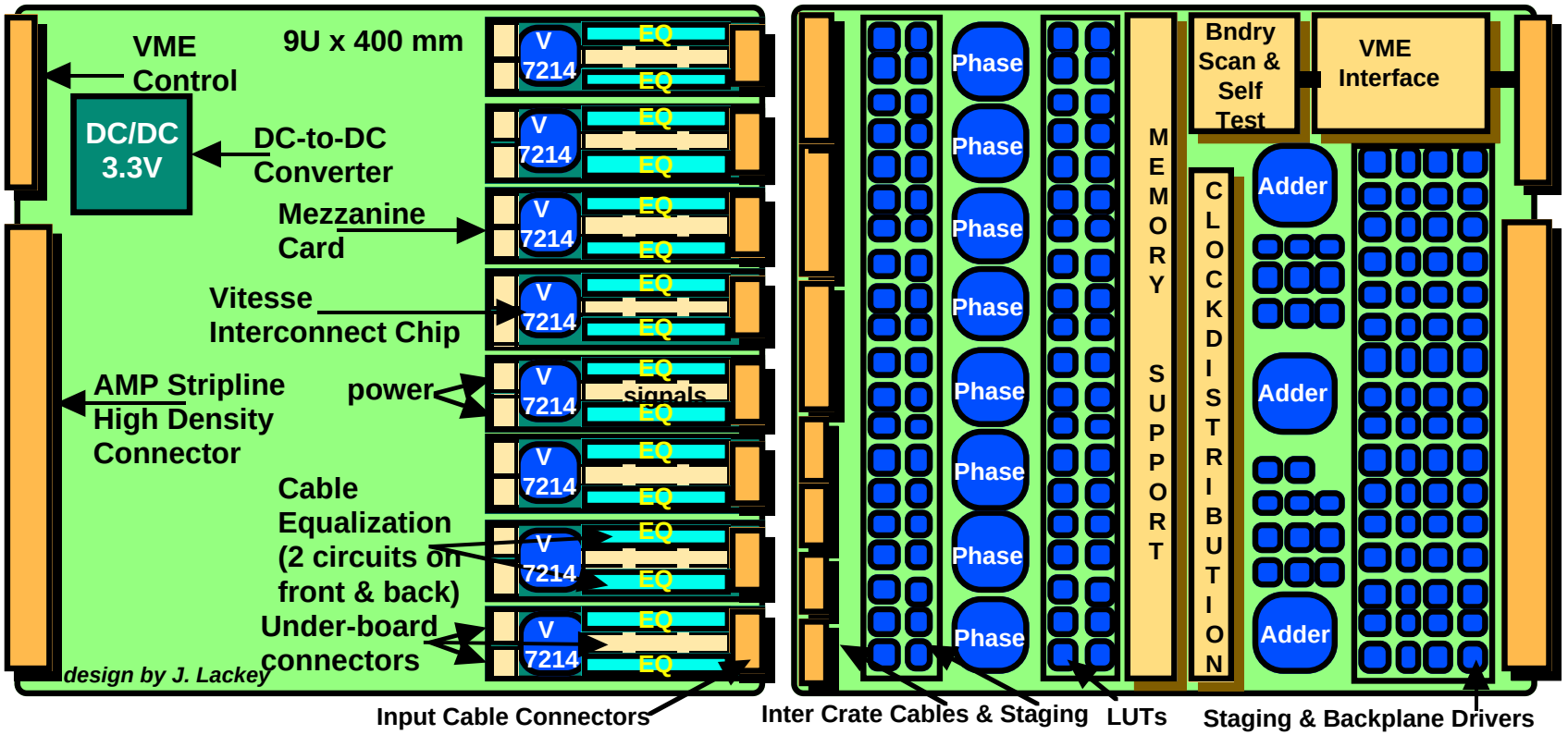
Each crate processes a 0.7 ϕ x 3.0 η region.

Each Receiver/Elec. ID card pair typically covers a .35 ϕ x 0.7 η region (modifed in high-η endcap region)

Calorimeter Regional Trigger Crate

Receiver Cards (x7/crate)

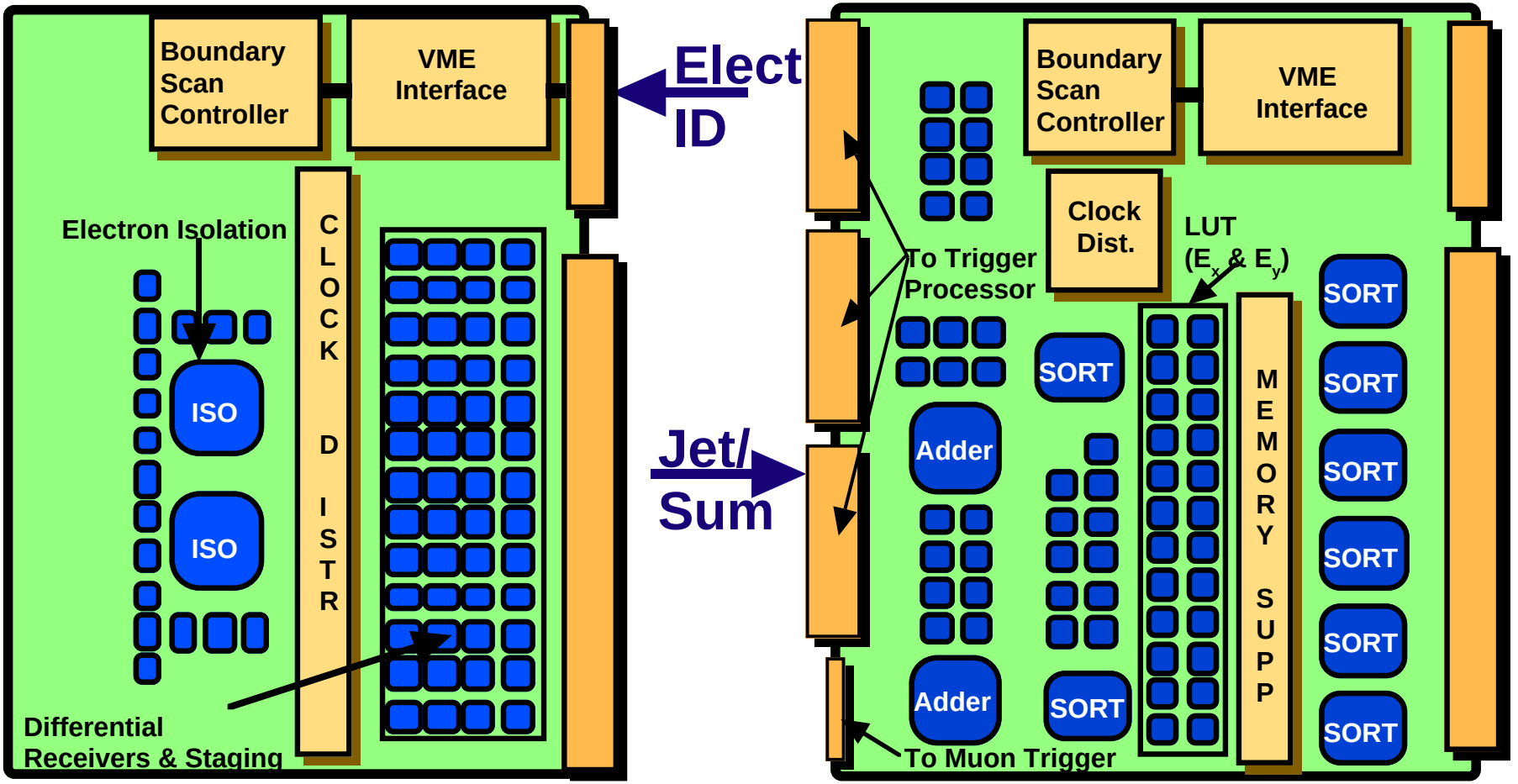
Receiver Card



Rear:
32 Channels =
4 Ch. x 8 mezzanine cards
1.2 GBaud copper rcvrs
18 bit (2x9) data + 5 bit error
Vitesse Chip:
Converts Serial to Parallel

Front: Data from Rear @ 120 MHz TTL
Phase ASIC: Deskew,Mux @ 160MHz
Error bit for each 4x4, Test Vectors
Memory LUT @ 160 MHz
Adder ASIC:
8 inputs @ 160 MHz in 25 ns.
Differential Output@160 MHz

Electron ID & Jet/Summary Cards



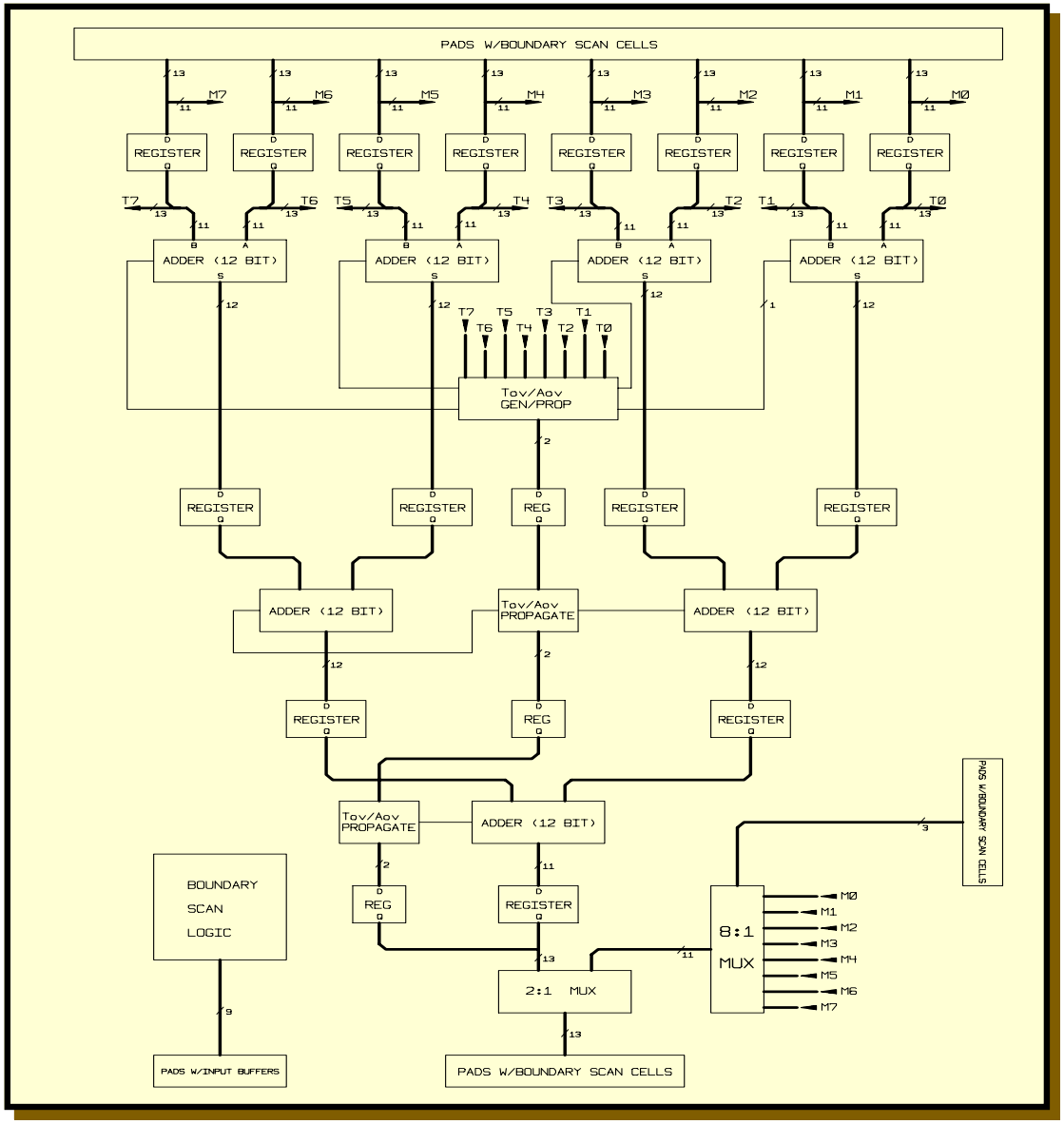
Processes 4x8 region @ 160 MHz
Electron isolation on ASIC
Lookup tables for ranking
Takes Max in each 4x4

Summarizes full crate:
Sorts 32 e's,4x4 E_t Æ top 4 e's, jets
LUTs: E_x & E_y from E_t for 4x4 area
Adder tree for E_t, E_x and E_y sums
Quiet/MinI bits for each 4x4 region

8 x 13-bit 160 MHz Adder ASIC

Vitesse 0.6μ H-GaAs
Process: ECL I/O

- 13 bits per operand
  x 8 operands
- Thirteen bit output
- Latency:
  25 ns @ 160 MHz
- Full Boundary Scan
- ~11,000 cells
- 4 Watts
- Tested > 200 MHz
- Operated on RC
- In Production



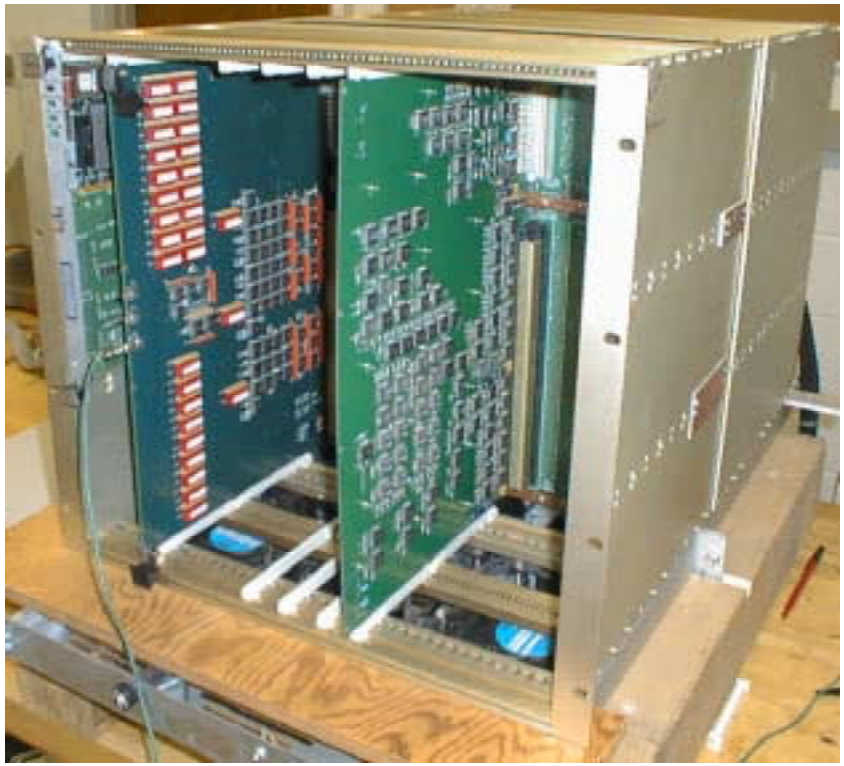
Cal. Trigger Dataflow Test

Prototype Crate with

- **160 MHz Backplane**
- **Proto. Receiver Card (rear)**
- **Proto. Clock Card (front)**
- **Proto. Electron ID Card (front)**

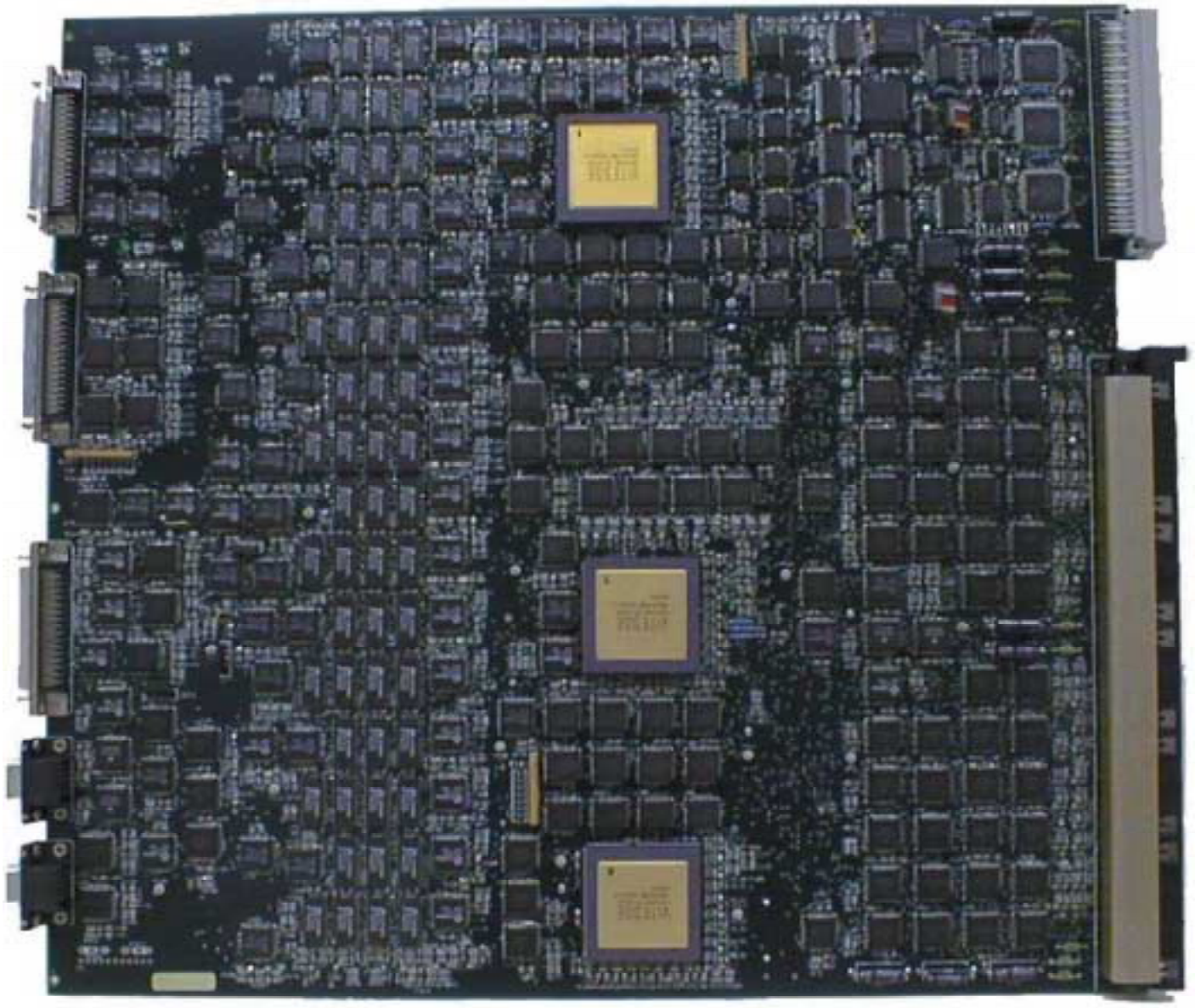
Full 160 MHz dataflow verified

REAR



FRONT

Prototype Receiver Card



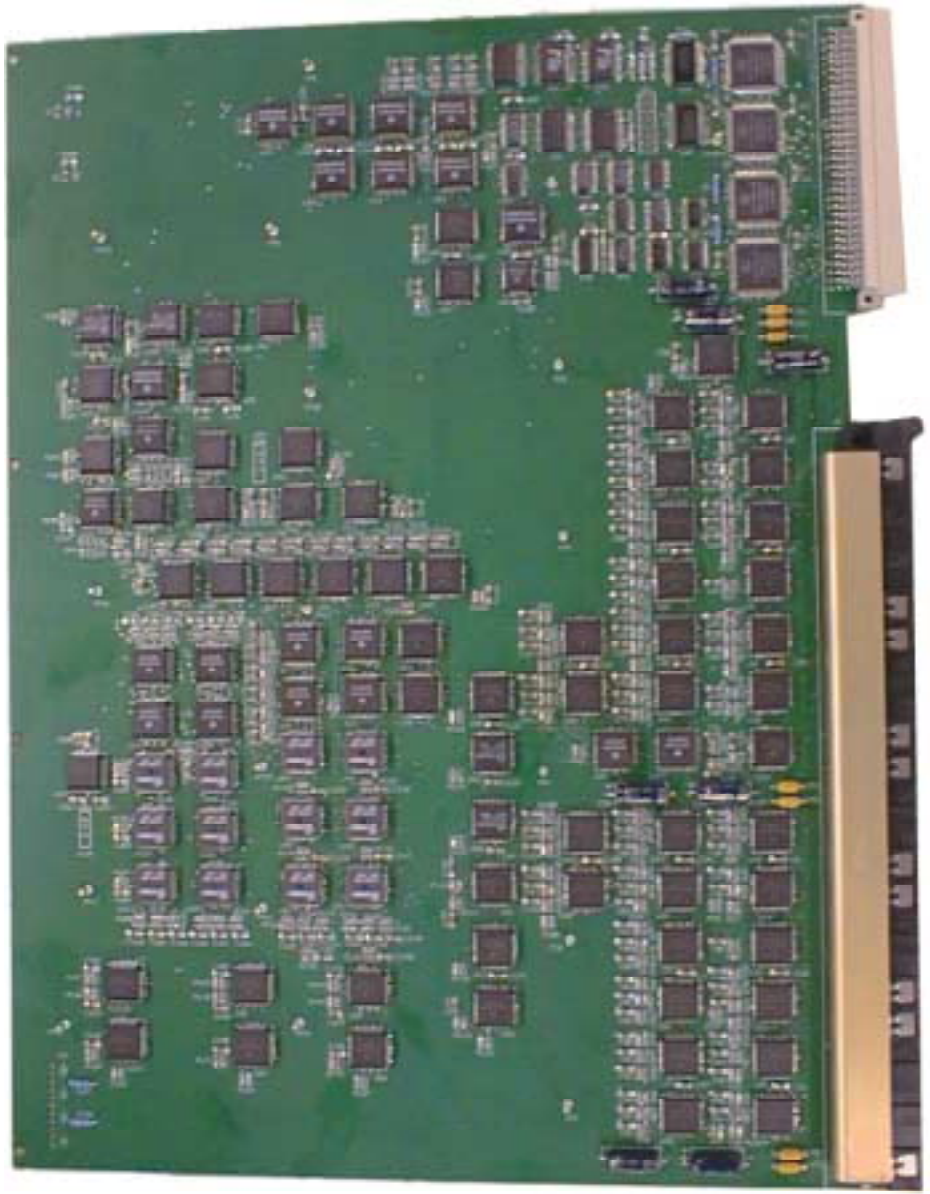
160 MHz Prototype Receiver Card tests:

- VME Interface checked
- Adder ASIC's checked
- Timing checked
- Intercrate sharing checked

Electron ID Card Prototype

Card tested:

- VME Interface working
- Dataflow from Receiver Card through custom backplane works
- Timing checked
- Logic verified



ASIC Development - Receiver

Prototype Phase ASIC (Receiver Card)

- Input: 120 MHz TTL data from Gbit Link Mezzanine Card
- Output: 160 MHz ECL data & error detection
- Status:
  - Layout & simulation finished, test vectors developed
  - Vitesse design reviews passed, ready for manufacture

Prototype Boundary Scan ASIC (Receiver Card)

- Boundary scan of Receiver Card Input
- Backplane drivers -- compact circuitry
- Status:
  - Layout & simulation finished, test vectors developed
  - Vitesse design reviews passed, ready for manufacture

Will test with new Receiver Card prototype

ASIC Development - EID & JS

Electron ID ASIC (Electron ID Card)

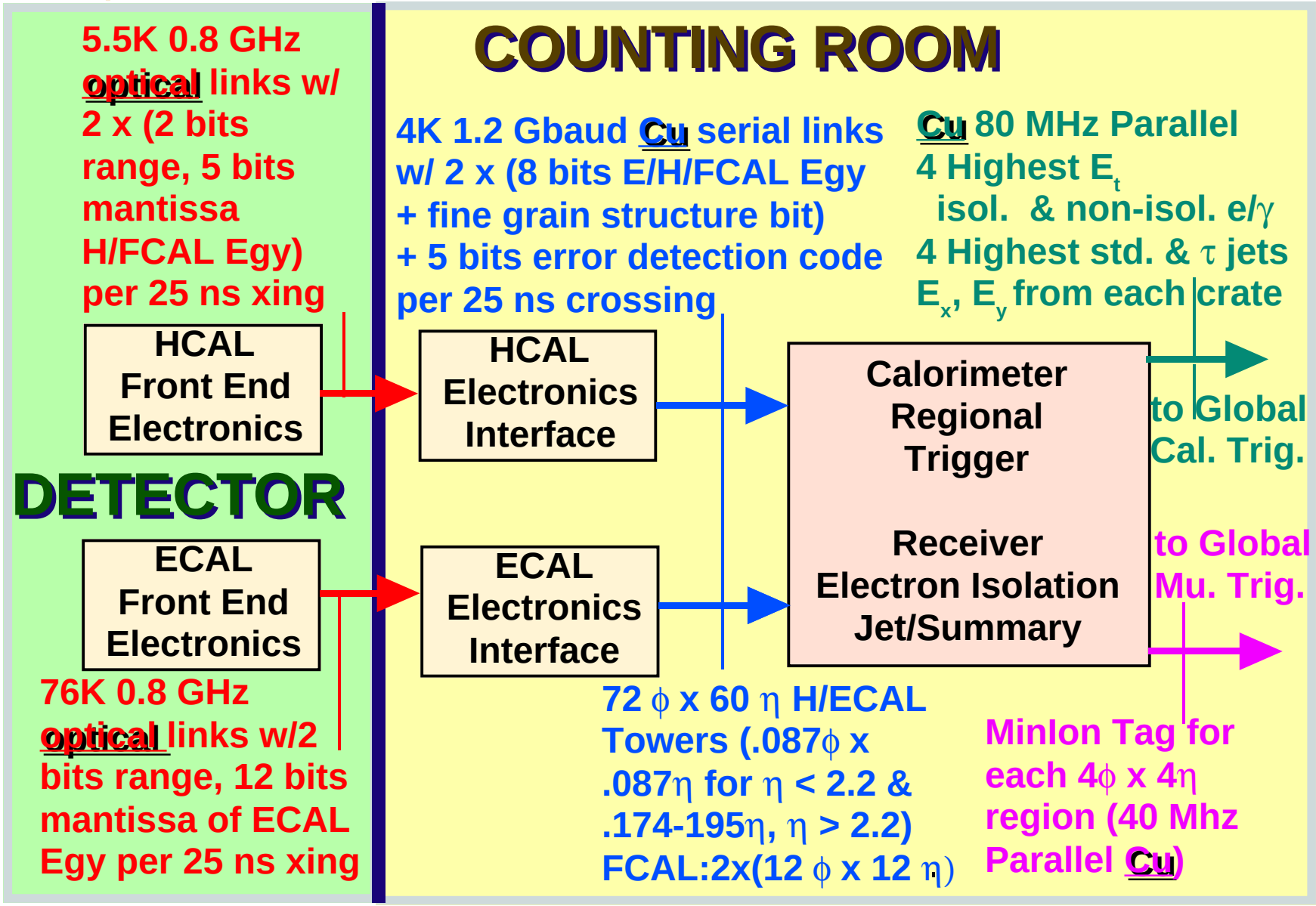
- **Implements Electron Isolation algorithm**
  - Described in talk of S. Dasu
- **Status: planned for completion by end of summer**
  - Design & Schematics Finished
  - Layout & simulation next

Sort ASIC (EID & Jet/Summary Card)

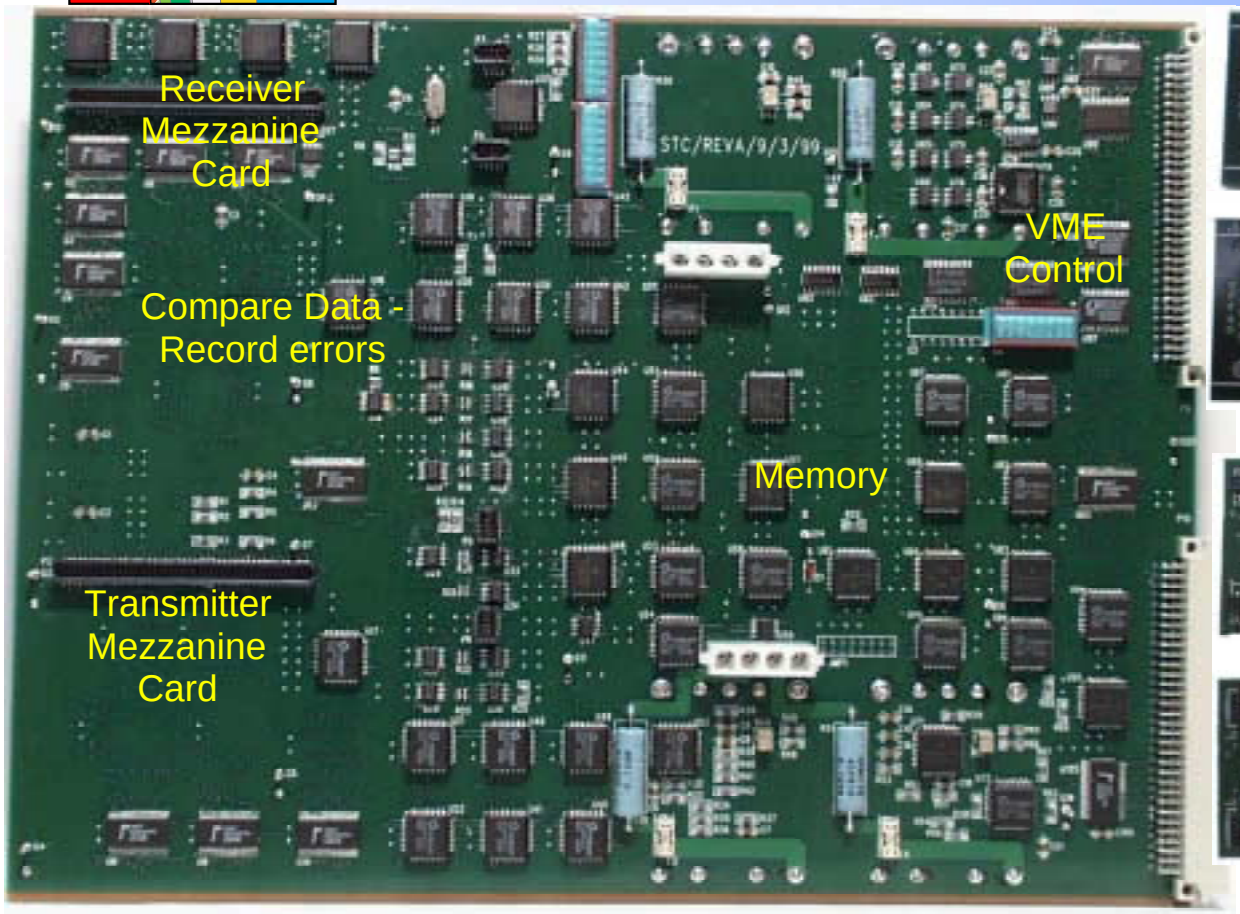
- **Integrated backplane receivers & sorting**
  - Passes 4 highest rank of 32 inputs
  - Sorts input before passing unto card
- **Status: planned for completion by end of summer**
  - Design & Schematics Finished
  - Layout & simulation next

Will test with new Electron ID Card prototype

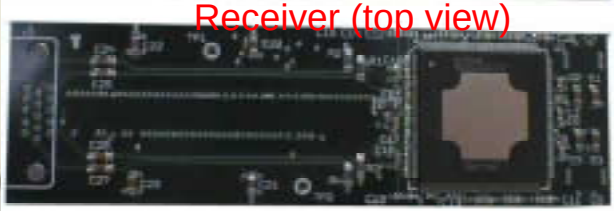
Calorimeter Trigger Links



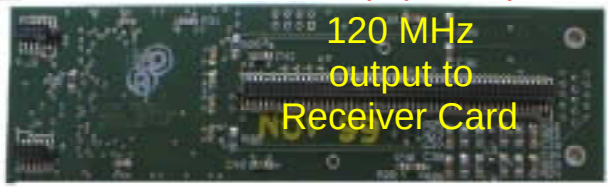
Copper Cable Gbit Serial Data Tests



Receiver (top view)



Transmitter (top view)



Receiver (bottom view)

Transmitter (bottom view)

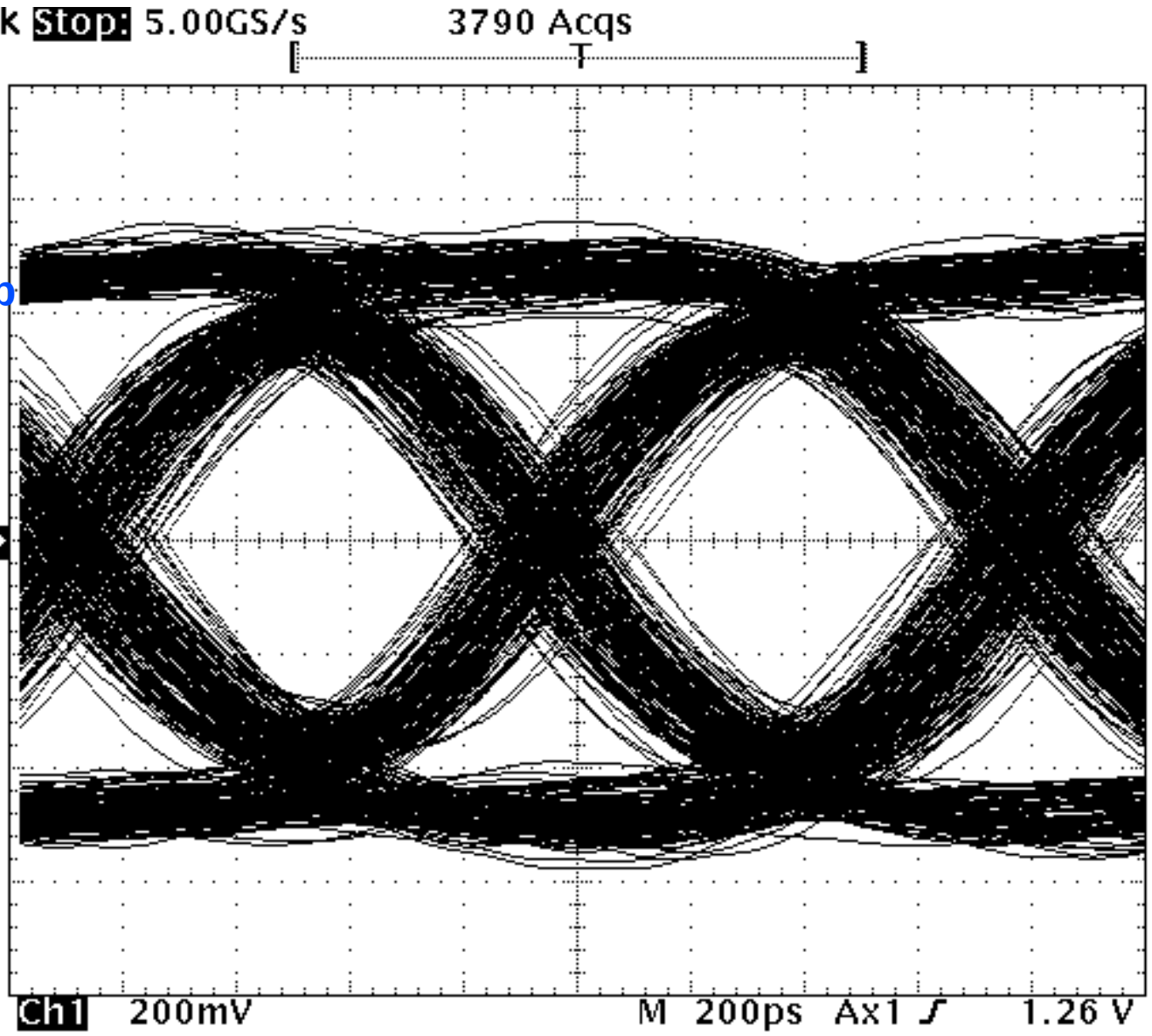
Serial Link Test Card includes VME, memories & comparison circuitry to fully test serial links @ 120 MHz TTL from Mezzanine Cards. (U. Wisconsin)

Mezzanine Transmit & Receive Cards convert 4 x 1Gb/s links to 120 MHz TTL w/ Vitesse 7214 & cable equalization

GBit Data Transmission

Tests over 20 m copper cable

- **PRELIMINARY!**
- **Vitesse 7214 4 x Gigabit Interconnect chip**
- **twisted pair cables (Belden 9182 (150 ohm, 22AWG, foamed dielectric,twin-ax) grouped by fours & terminated with 8-pin DIN style connectors $318 per 500 foot spool ($2.10 per meter).**



Trigger Link Bit Error Detection

Link error code simulation:

- **Between ECAL & HCAL Upper Level Readout & Cal. Regional Trigger**
  - 2x(8 bits E_T + 1 bit finegrain) + 5 bits error detection code* + 1 bit "Gap Flag" = 24 bits/25 ns
  - Full 5-bit Hamming Code* finds all 1 & 2-bit errors (most common)
  - Also finds more than 96% of any other error type
- **Procedure upon error is to zero and log the error for readout by DAQ**
- **Full implementation in Phase ASIC**
  - Passed Vitesse Design Review.

Bits with errors	Number of Patterns	Percent of Errors not found
0	1	0.00
1	24	0.00
2	276	0.00
3	2024	3.45
4	10626	3.49
5	42504	3.03
6	134596	0.08
7	346104	0.17
8	735471	0.06
9	1307504	0.14
10	1961256	0.01
11	2496144	0.01
12	2704156	0.02
13	2496144	0.01
14	1961256	0.10
15	1307504	0.15
16	735471	0.06
17	346104	0.30
18	134596	0.08
19	42504	3.24
20	10626	3.23
21	2024	2.77
22	276	0.03
23	24	0.00
24	1	0.00

Plans for Next Year

ASIC Development

- **Boundary Scan & Phase ASIC**
  - Test prototype run from Vitesse
- **Sort & Electron ID ASIC**
  - Finish layout & simulation
  - Vitesse to manufacture, then test

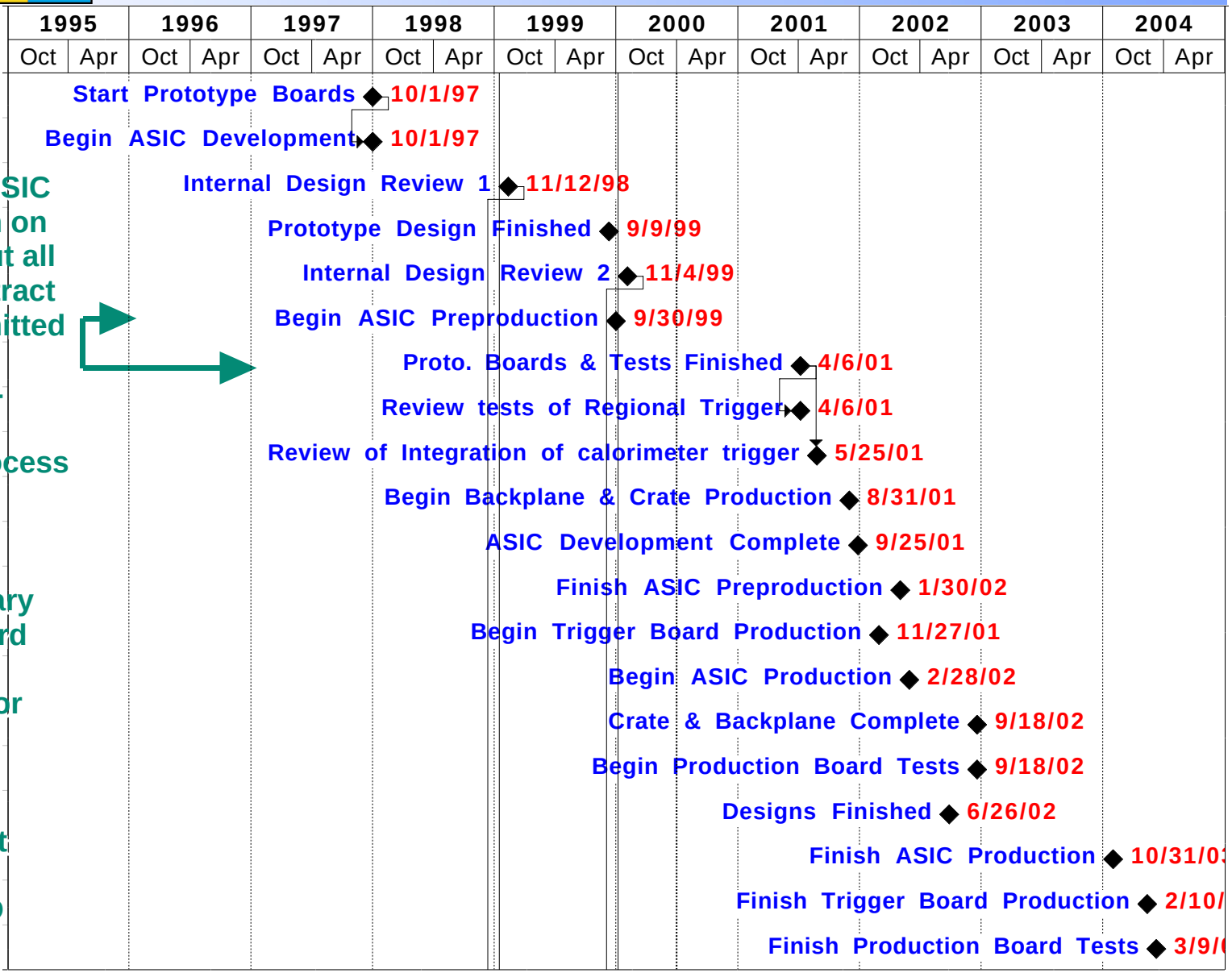
Next generation prototypes

- **Backplane**
  - Designed for final algorithms
- **Receiver Card**
  - Used for testing Phase & Boundary Scan ASICs
  - Will be fit with Gbit link mezzanine cards
- **Electron Isolation Card**
  - Used for testing Sort & Electron ID ASICs

Serial Link Tests

- **Select final cable**
- **Integrate new generation Vitesse link chip (7216)**
- **provide test boards for integration with HCAL, ECAL**

Cal Trigger Schedule & Milestones



Advance ASIC production on order to put all under contract with committed delivery schedule -- reduces vendor/process risk

Delay Jet/Summary Proto. Board since not essential for design validation. Move J/S component tests to Electron ID Card.

Cal Trigger Personnel

Physicists (at Wisconsin)**:**

- **Faculty: W. Smith & new hire**
- **Scientists: S. Dasu & P. Chumney (new)**

Engineers (experienced team at Wisconsin)**:**

- **J. Lackey -- Lead Engineer & Designer**
  - Also Lead Engineer for Zeus Calorimeter Trigger
- **M. Jaworski -- Board Layout & Design support**
  - Worked on Zeus Calorimeter Trigger
- **H. Zhang -- ASIC Layout/Simulation (new)**
  - Worked on Zeus Calorimeter Trigger
- **D. Wahl -- Copper Link Test/Development (new)**
  - PSL Engineer, assisted by lead PSL electronics engineer, P. Robl, who worked on Zeus Trigger

Issues

Committee Concerns:

- **Increase Physicists & Engineering Personnel**
  - Done (see previous slide)
- **Apply engineering resources to recover schedule**
  - Done: application to ASIC development & Gbit Link

Issue at time of last review:

- **Watch ASIC availability issues, as early procurement may become necessary.**
  - Entire ASIC production under contract with Vitesse
  - Schedule rearranged to procure all of each ASIC immediately after successful test.
  - Detailed series of reviews set up with Vitesse to provide strict QA/QC & testability
  - Vitesse to deliver fully tested packaged ASICs

Conclusions

Successful Prototyping Program

- Crate, Backplane & Clock Card
- Receiver Card
- Electron Isolation Card
- Serial Link Test & Mezzanine Cards
- Adder ASIC -- now in production

Plans for next year

- Completion of all first prototype & some second.
- Link prototypes used for integration w/ECAL,HCAL

Cost & Schedule experience:

- ASIC vendor/schedule accelerated
- Personnel augmented
- No use of contingency, on schedule