



# WBS 3.1 - Trigger

**Wesley Smith, *U. Wisconsin*  
CMS Trigger Project Manager**

**DOE/NSF Review  
May 8, 2001**



# Outline

- **Overview of Calorimeter Trigger**
- **Calorimeter Trigger Status & Technical Progress**
- **Overview of Muon Trigger**
- **Muon Trigger Status & Technical Progress**
- **Cost & Schedule Performance**
- **Concerns**
- **Plans**
- **Summary and Conclusions**

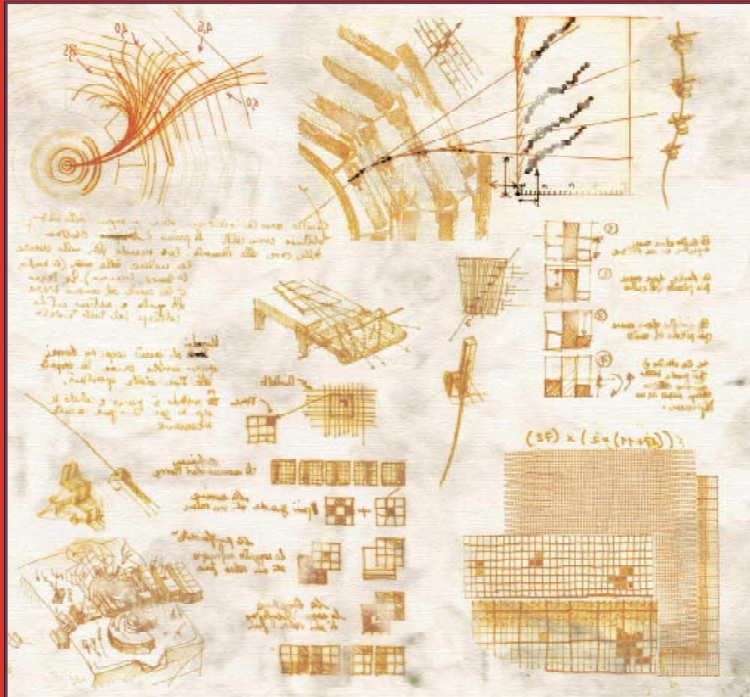


# CMS Level -1 Trigger TDR

LABORATOIRE EUROPEEN POUR LA PHYSIQUE DES PARTICULES  
CERN EUROPEAN LABORATORY FOR PARTICLE PHYSICS

CERN/LHCC 00-xx  
CMS TDR 6.1  
November 2000

# C M S



The TriDAS project. Volume I  
The Trigger Systems

## CMS Level 1 Milestone

Submitted to LHCC  
on Nov. 28, 2000:  
CERN/LHCC 2000 - 38  
CMS TDR 6.1

Approved in March, 2001.

[http://cmsdoc.cern.ch/cms/  
TDR/TRIGGER-public/trigger.html](http://cmsdoc.cern.ch/cms/TDR/TRIGGER-public/trigger.html)



# Regional Calorimeter Crate

(WBS 3.1.2)

Receiver Card  
(WBS 3.1.2.8)

Electron Identification Card  
(WBS 3.1.2.9)

Jet Summary Card  
(WBS 3.1.2.10)

DAQ Proc  
(WBS 3.1.2.12)

Prototypes  
(WBS 3.1.2.1)

Preprod. ASICs  
(WBS 3.1.2.2)

Test Facilities  
(WBS 3.1.2.3)

Power Supplies  
(WBS 3.1.2.4)

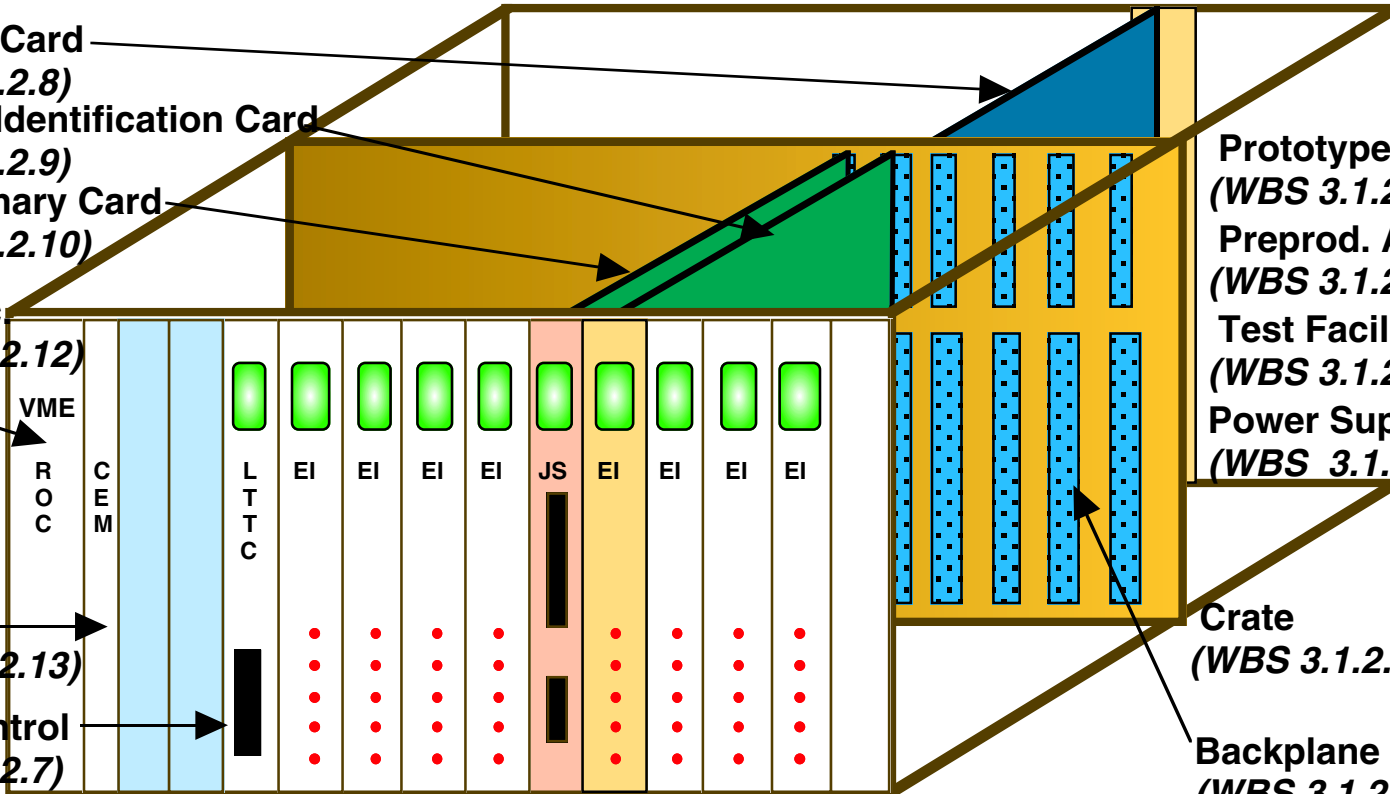
19 X

Monitor  
(WBS 3.1.2.13)

Clock/Control  
(WBS 3.1.2.7)

Crate  
(WBS 3.1.2.5)

Backplane  
(WBS 3.1.2.6)



**Data from calorimeter FE on Cu links @ 1.2 Gbaud (ptyp. tstd.)**

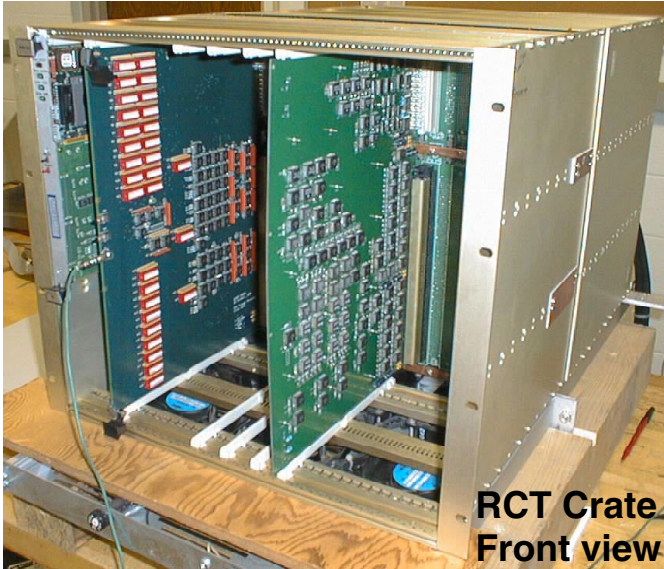
- Into 152 rear-mounted Receiver Cards (ptyp. tstd. w/ ASICs)

**160 MHz point to point backplane (ptyp. tstd.)**

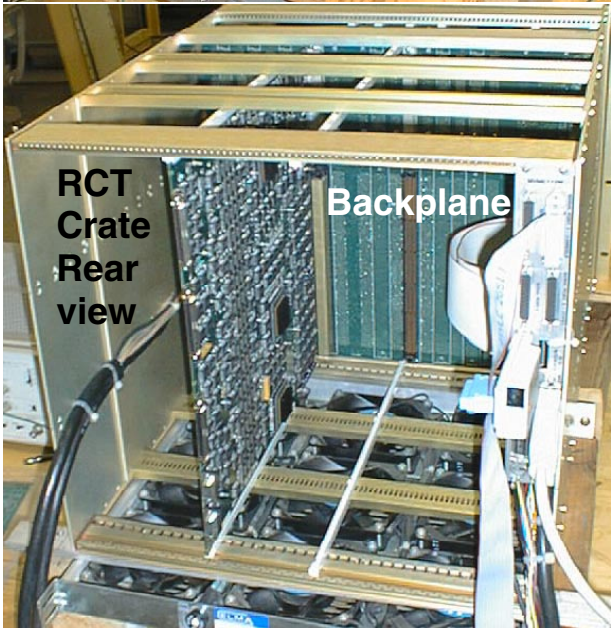
- 19 Clock&Control (ptyp. tstd.), 152 Electron ID (ptyp. tstd.)
- 19 Jet/Summary, Receiver Cards operate @ 160 MHz



# Regional Cal. Trig. Prototypes



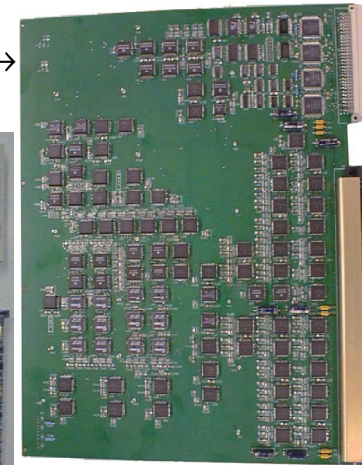
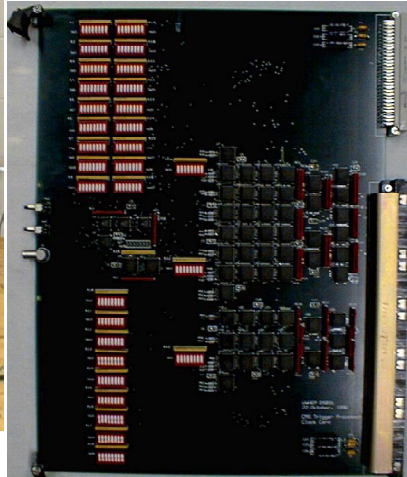
RCT Crate  
Front view



RCT  
Crate  
Rear  
view

Backplane

Electron ID Card →  
Clock & Control Card



Receiver  
Card ↓

All  
Tests  
Passed

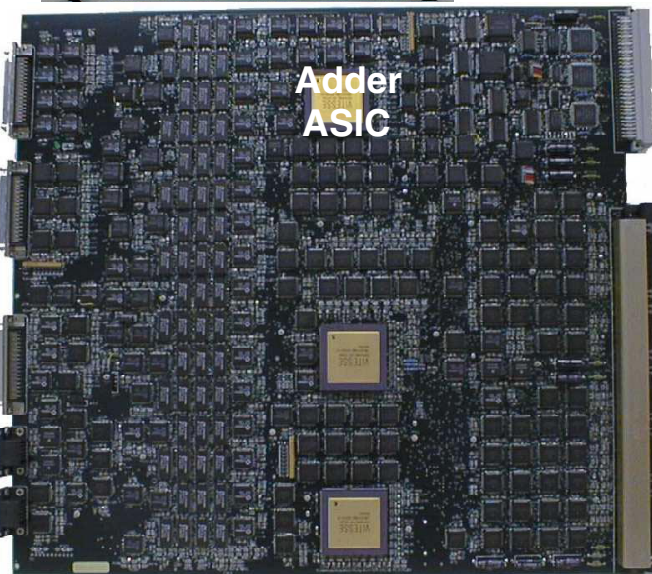
Intercrate  
sharing checked

Timing checked

Adder ASIC fully  
qualified for  
production

Full 160 MHz  
dataflow verified

VME checked



Adder  
ASIC



# Calorimeter Trigger Status

## Successful Prototyping Program

- Crate, 160 MHz Backplane & Clock Card
- Receiver & Electron Isolation Cards tested
- Adder ASIC tested & production finished
- Links: 4x1Gbit on Cu\* ECL x 20 m tested

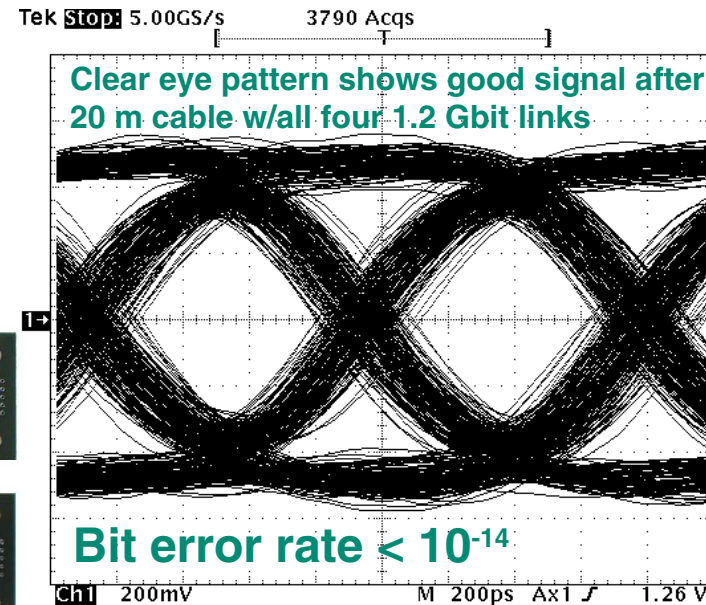
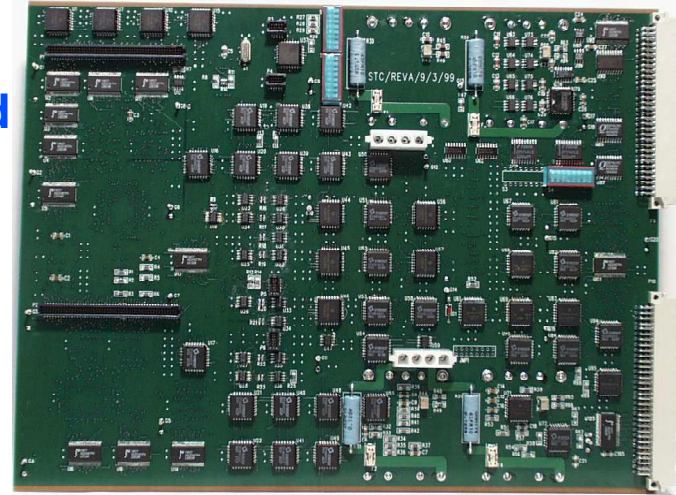
## ASIC prototype development finished

- Phase & Boundary Scan protos delivered
- Isolation & Sort protos manufactured

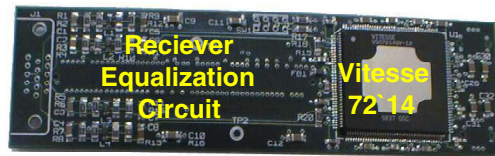
## Testing Program Plans

- Next generation Backplane finished
- Next generation Receiver, Elect. Iso.
- Test remaining ASIC prototypes

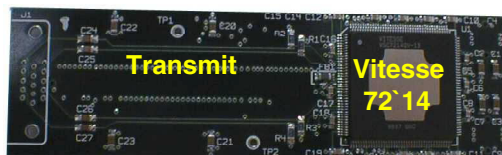
\*Gbit Serial Cu Link Cards & test results:

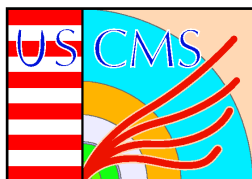


Mezzanine Card (Top view)



Mezzanine Card (Bottom view)

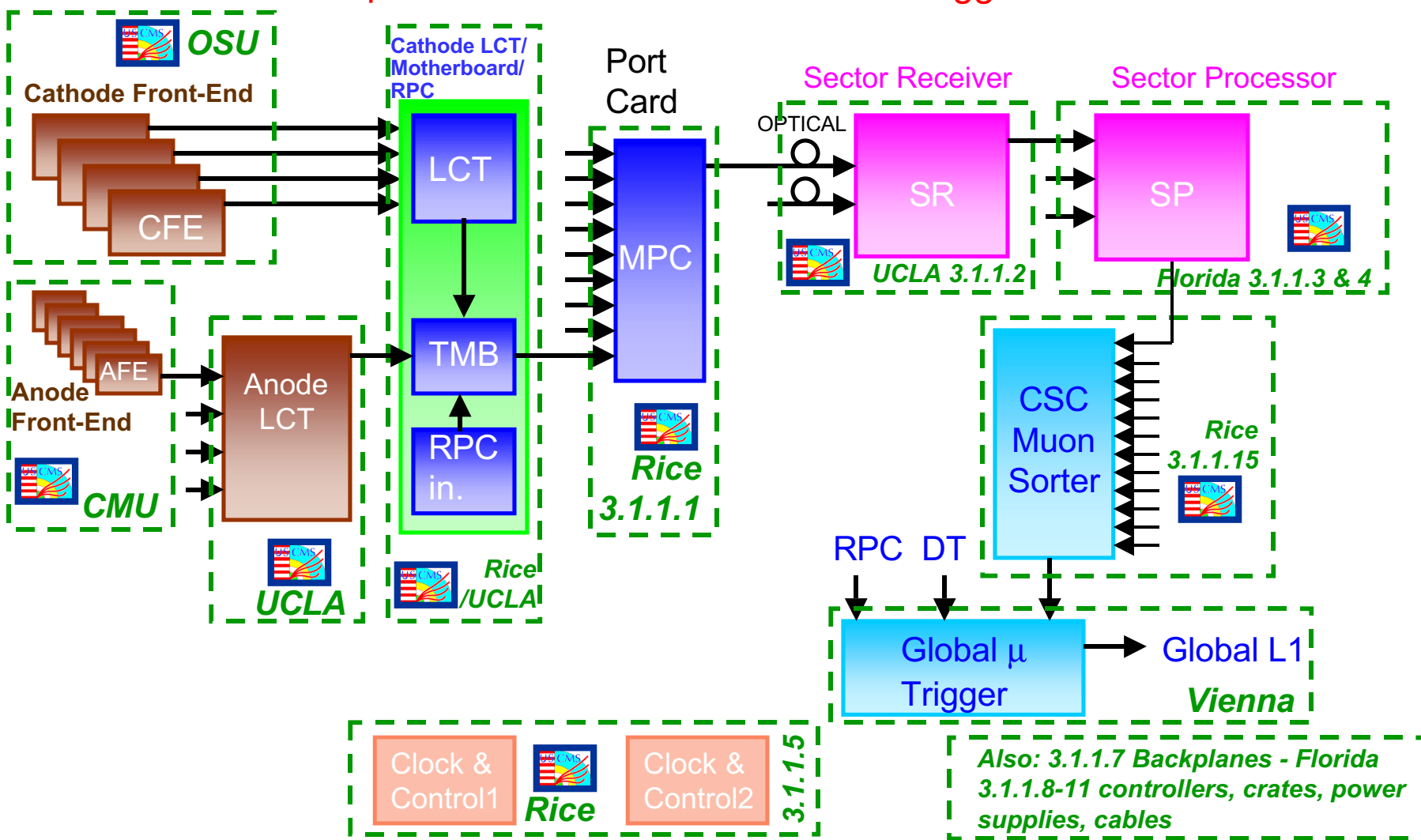


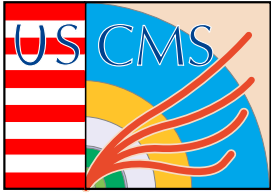


# CSC Muon Trigger

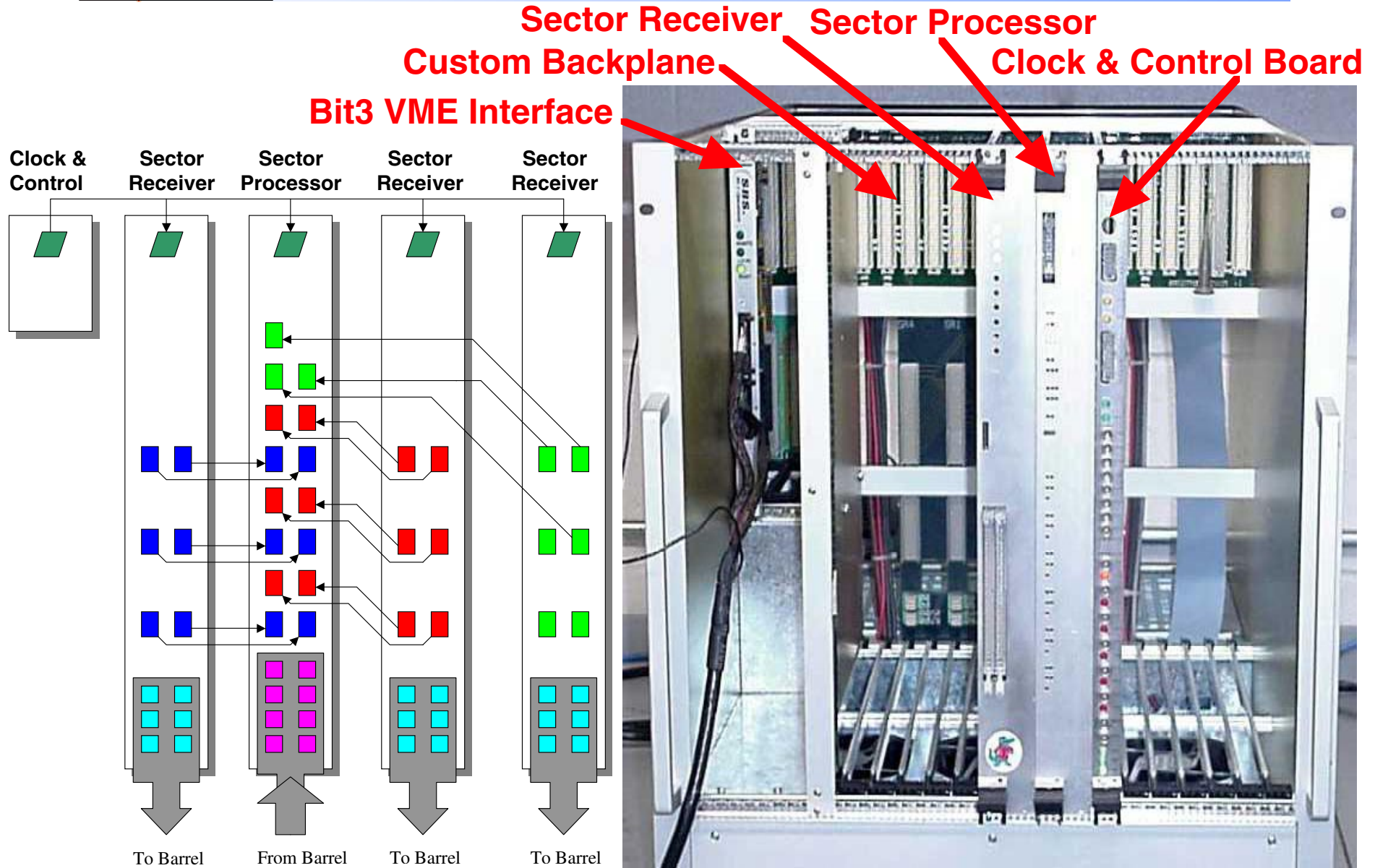
(WBS 3.1.1)

← USCMS Endcap Muon → ← USCMS Trigger/DAQ 3.1.1 →

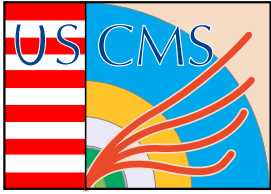




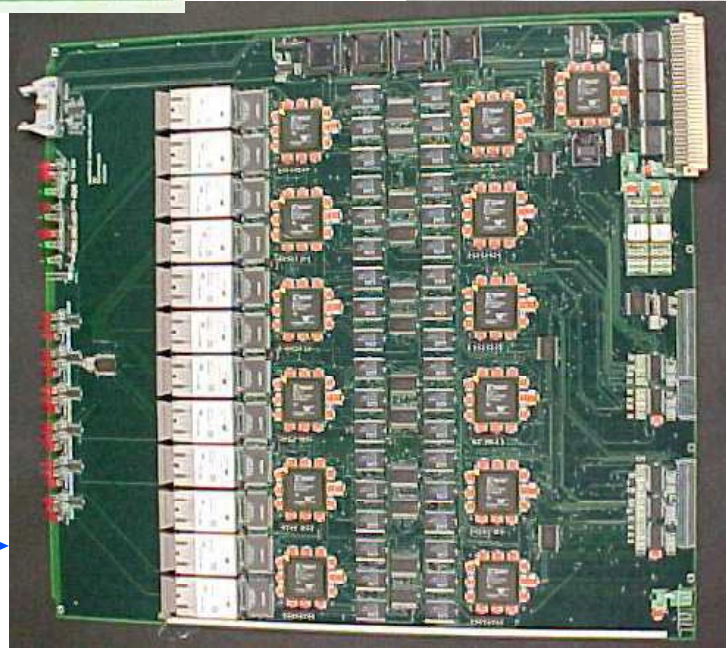
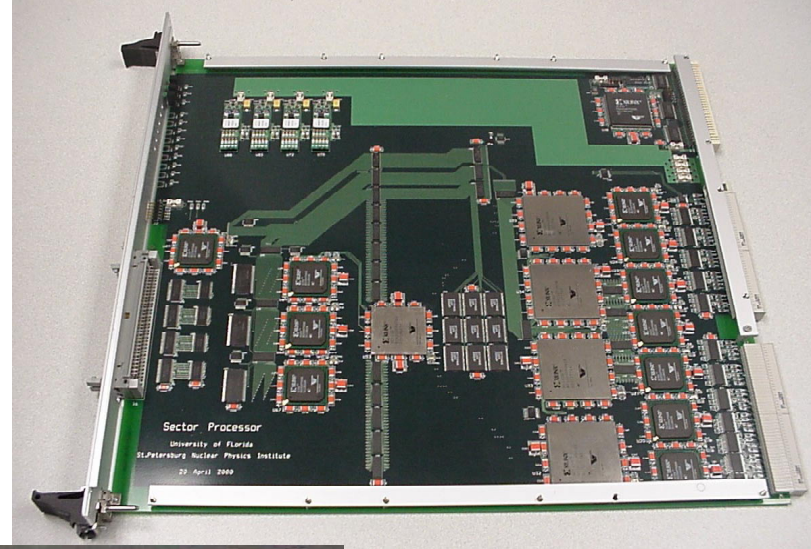
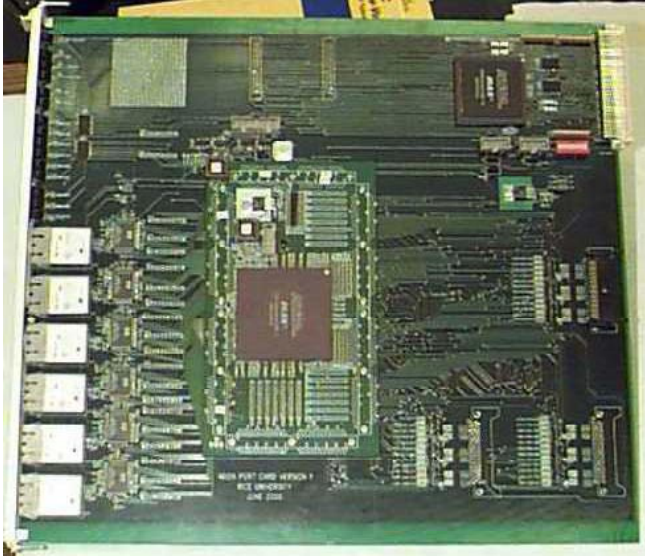
# CSC Track Finder Crate







# CSC Trigger Protos Tested



Muon Port Card (Rice)

Sector Processor (U. Florida)

Dataflow verified, incl. optical link

Sector Receiver (UCLA)

All logic tested & agrees with ORCA simulation



# CSC Trig. Conclusions & Plans

## Conclusions from Test

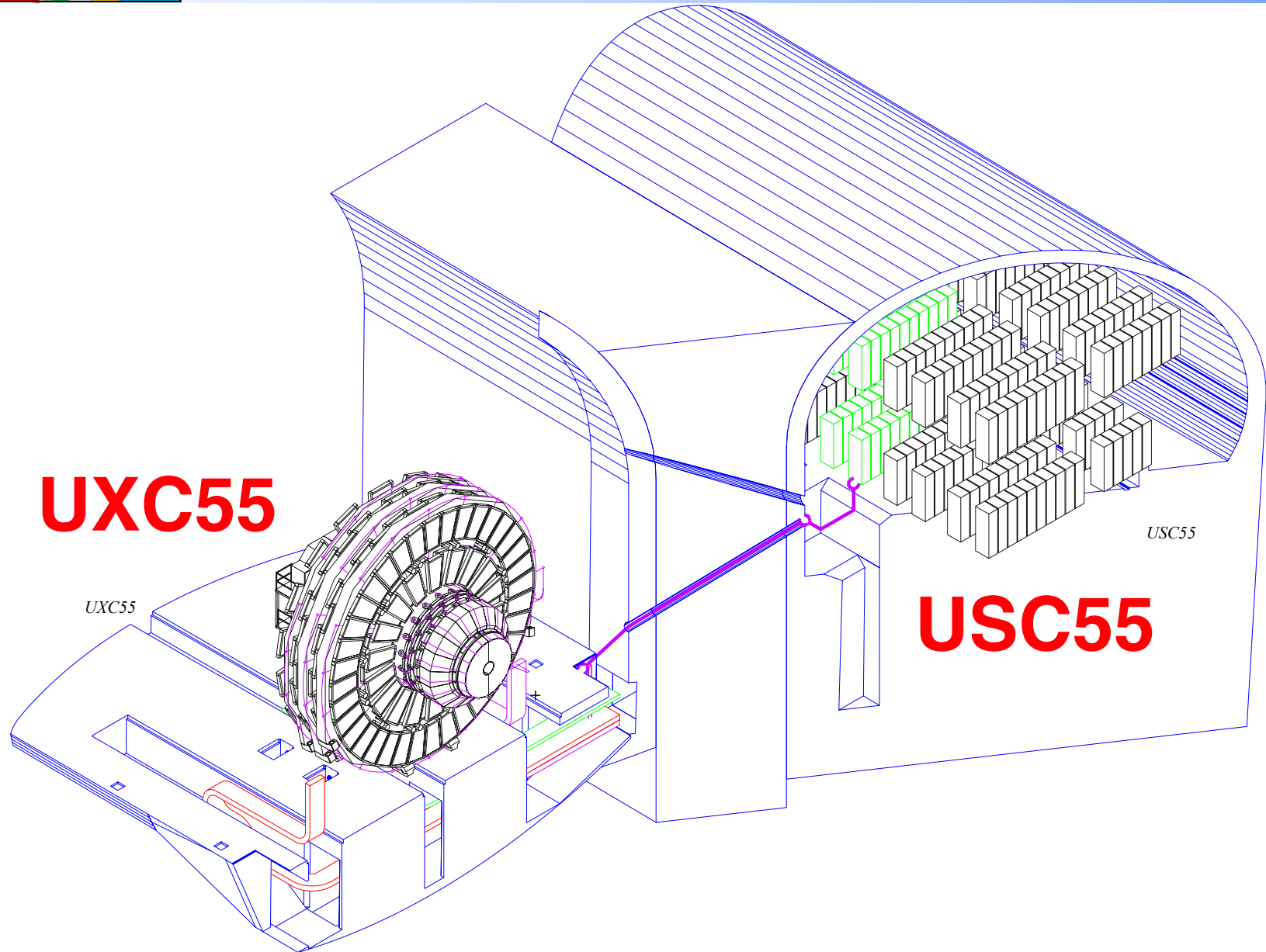
- Conceptually Sound Design
- Need to reduce latency

## Plans for This Year *(review at end of May)*

- **Replace Backplane technology with faster**
  - Channel Link -> GTLP at 80 MHz
  - New prototype backplane tested at Florida
- **New Compact Single Crate Design**
  - Merge all 17 FPGAs of baseline design into one
  - Possible due to new FPGA technology
  - Merge Sector Receiver & Sector Processor Boards
- **New Optical Link Technology**
  - Use new 1.6 Gbit/s links with 80 MHz clock
  - Tested at Rice and Works



# Trigger System Installation





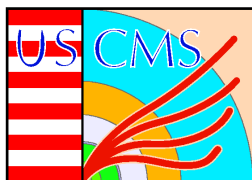


# Trigger Tasks

| Tasks                             | start | finish: |
|-----------------------------------|-------|---------|
| • Produce TDR                     | 8/00  | 12/00 ✓ |
| • Design Final Prototypes         | 11/00 | 12/01   |
| • Construct Final Prototypes      | 6/01  | 6/02    |
| • Test/Integrate Final Prototypes | 12/01 | 12/02   |
| • Pre-Production Design & Test    | 6/02  | 6/03    |
| • Production                      | 12/02 | 6/04    |
| • Production Test                 | 6/03  | 11/04   |
| • Trigger System Tests            | 5/04  | 5/05 ←  |
| • Trigger Installation            | 11/04 | 11/05 ← |
| • Integration & Test w/DAQ & FE   | 3/05  | 9/05 ←  |
| • Maintenance & Operations        | 10/05 | ----- ← |

## Impact of delayed access to USC55 & UXC55:

- US EDIA cost increased by \$200K -- CMS cost unchanged
  - 100K each for CSC & Regional Cal Trigger



# US CMS Trigger

## L1, L2, L3 Milestone Performance

| System | Level? | CMS ID | Milestone   | Variance | Baseline Start | Start      | 1998 | 1999 |     | 2000 |     | 2001 |     | 2002 |     |
|--------|--------|--------|---|----------|----------------|------------|------|------|-----|------|-----|------|-----|------|-----|
|        |        |        |   |          |                |            | Apr  | Oct  | Apr | Oct  | Apr | Oct  | Apr | Oct  | Apr |
|        |        |        | ☐ Trigger System (WBS 1.3.1)                                      | 0 days   | NA             | Nov 03 '98 |      |      |     |      |     |      |     |      |     |
| TRIG   | ML2    | D-001  | Complete Initial Muon, Calorimeter, & Global Trigger Design       | -19 days | Nov 30 '98     | Nov 03 '98 | ●    |      |     |      |     |      |     |      |     |
| TRIG   | ML3    | D-387  | CSC: Sector Receiver Initial System Design Document (UCLA)        | 0 days   | Mar 31 '99     | Mar 31 '99 |      | ●    |     |      |     |      |     |      |     |
| TRIG   | ML3    | D-331  | TK: Sector Processor Initial System Design Document (Florida)     | 0 days   | Mar 31 '99     | Mar 31 '99 |      | ●    |     |      |     |      |     |      |     |
| TRIG   | ML3    | D-388  | CSC: Muon Port Card Prototype Design (Rice)                       | 0 days   | May 31 '99     | May 31 '99 |      | ●    |     |      |     |      |     |      |     |
| TRIG   | ML3    | D-390  | CSC: Sector Receiver Prototype Design (UCLA)                      | -1 day   | Jun 30 '99     | Jun 30 '99 |      | ●    |     |      |     |      |     |      |     |
| TRIG   | ML3    | D-332  | TK: Sector Processor Prototype Design (Florida)                   | -22 days | Sep 30 '99     | Aug 31 '99 |      | ●    |     |      |     |      |     |      |     |
| TRIG   | ML3    | D-389  | CSC: Muon Port Card Prototype Delivery (Rice)                     | 59 days  | Sep 30 '99     | Dec 31 '99 |      | ●    |     |      |     |      |     |      |     |
| TRIG   | ML2    | D-002  | Complete Phase 1 Prototype Design                                 | -20 days | Nov 30 '99     | Nov 02 '99 |      |      | ●   |      |     |      |     |      |     |
| TRIG   | ML3    | D-212  | Review of Test of Trigger Primitives - 2 Tower Proto Board        | 0 days   | Nov 30 '99     | Nov 30 '99 |      |      | ●   |      |     |      |     |      |     |
| TRIG   | ML3    | D-221  | Review of Test of Regional Trigger - Proto Board and ASICs        | 0 days   | Nov 30 '99     | Nov 30 '99 |      |      | ●   |      |     |      |     |      |     |
| TRIG   | ML3    | D-240  | Review of Calorimeter Trigger Control and Readout Software        | 0 days   | Nov 30 '99     | Nov 30 '99 |      |      | ●   |      |     |      |     |      |     |
| TRIG   | ML3    | D-231  | Design of Final Sort ASIC   | 251 days | Nov 30 '99     | Nov 30 '00 |      |      | ●   |      |     |      |     |      |     |
| CMS1   | ML1    | D-004  | Submit Trigger Technical Design Report (TDR)                      | 0 days   | Nov 30 '00     | Nov 30 '00 |      |      |     | ●    |     |      |     |      |     |
| TRIG   | ML3    | D-250  | Review of Integration of Calorimeter Trigger Prototypes (Palaise) | 502 days | Nov 30 '99     | Nov 30 '01 |      |      |     |      | ●   |      |     |      |     |

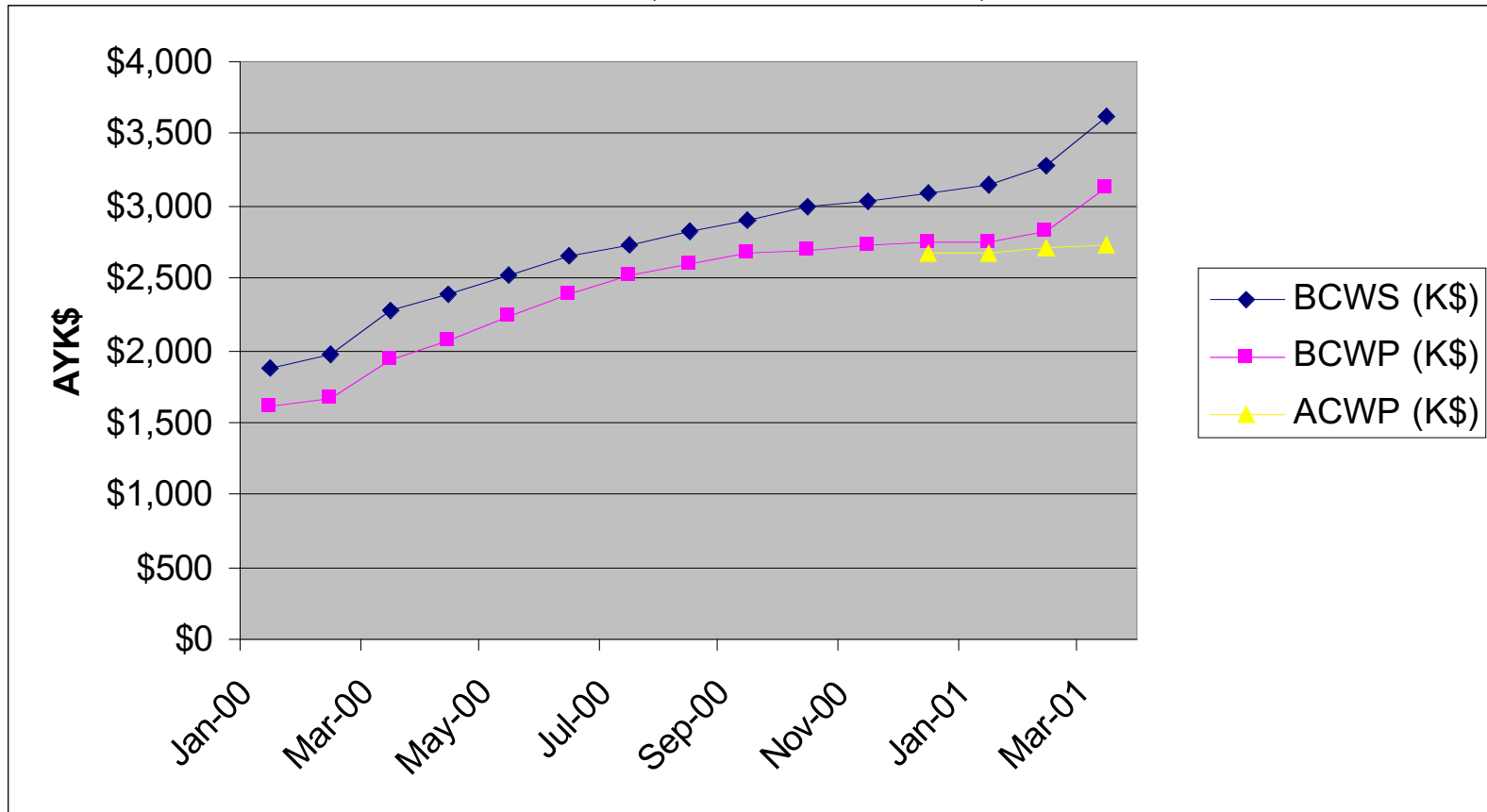
### Comments:

**Major L1 Milestone: Trigger TDR on Time!**

- Milestone for SORT ASIC start compensated by faster finish
- Integration waiting for ECAL electronics
- Extra slack in schedule due to delayed installation



# US CMS Trigger BCWS, BCWP, & ACWP



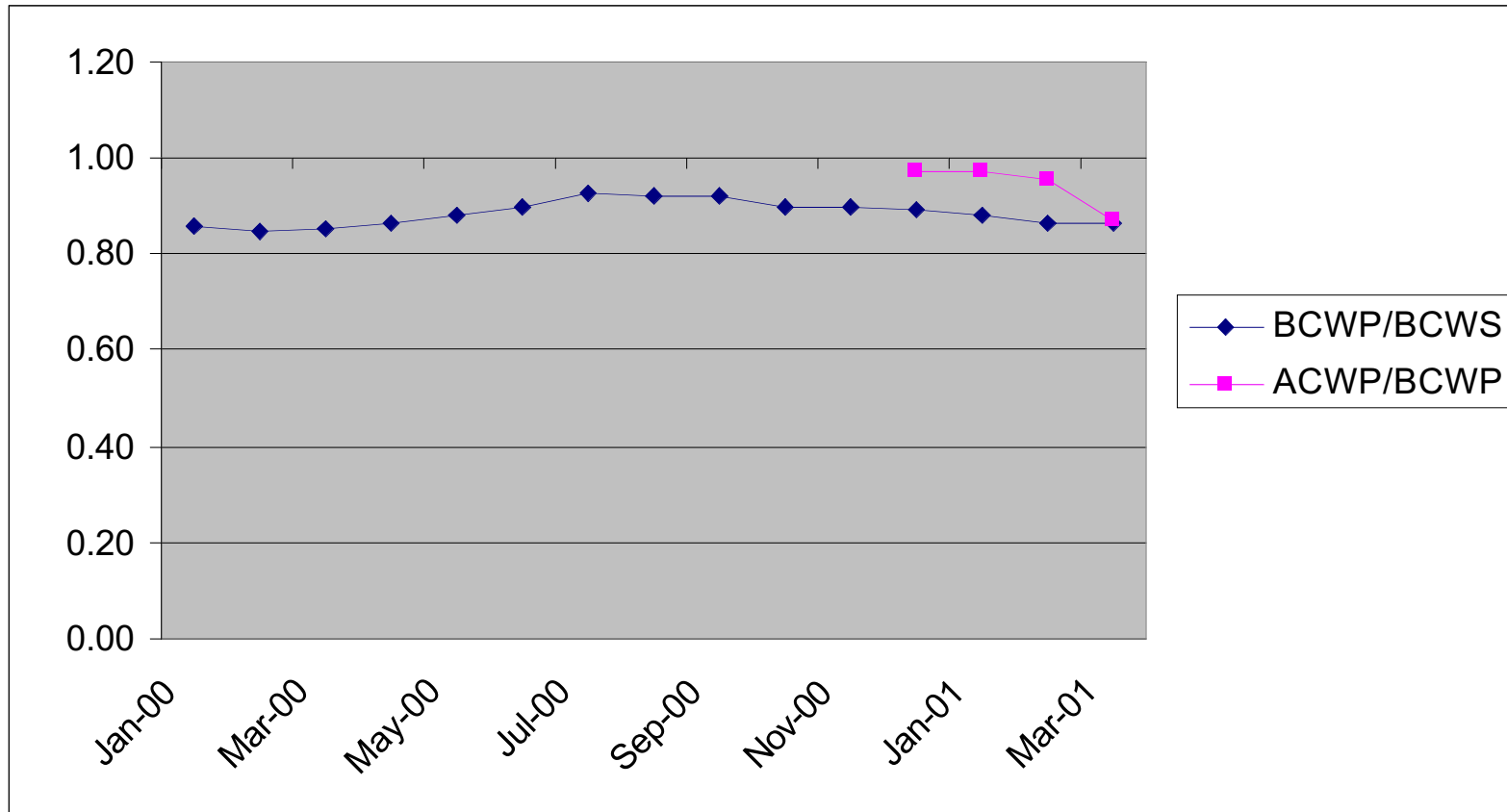
**Project tracking tools in place and in use**

**Consistent with overall schedule picture**

(see next slide)



# US CMS Trigger Sch. & Cost Performance

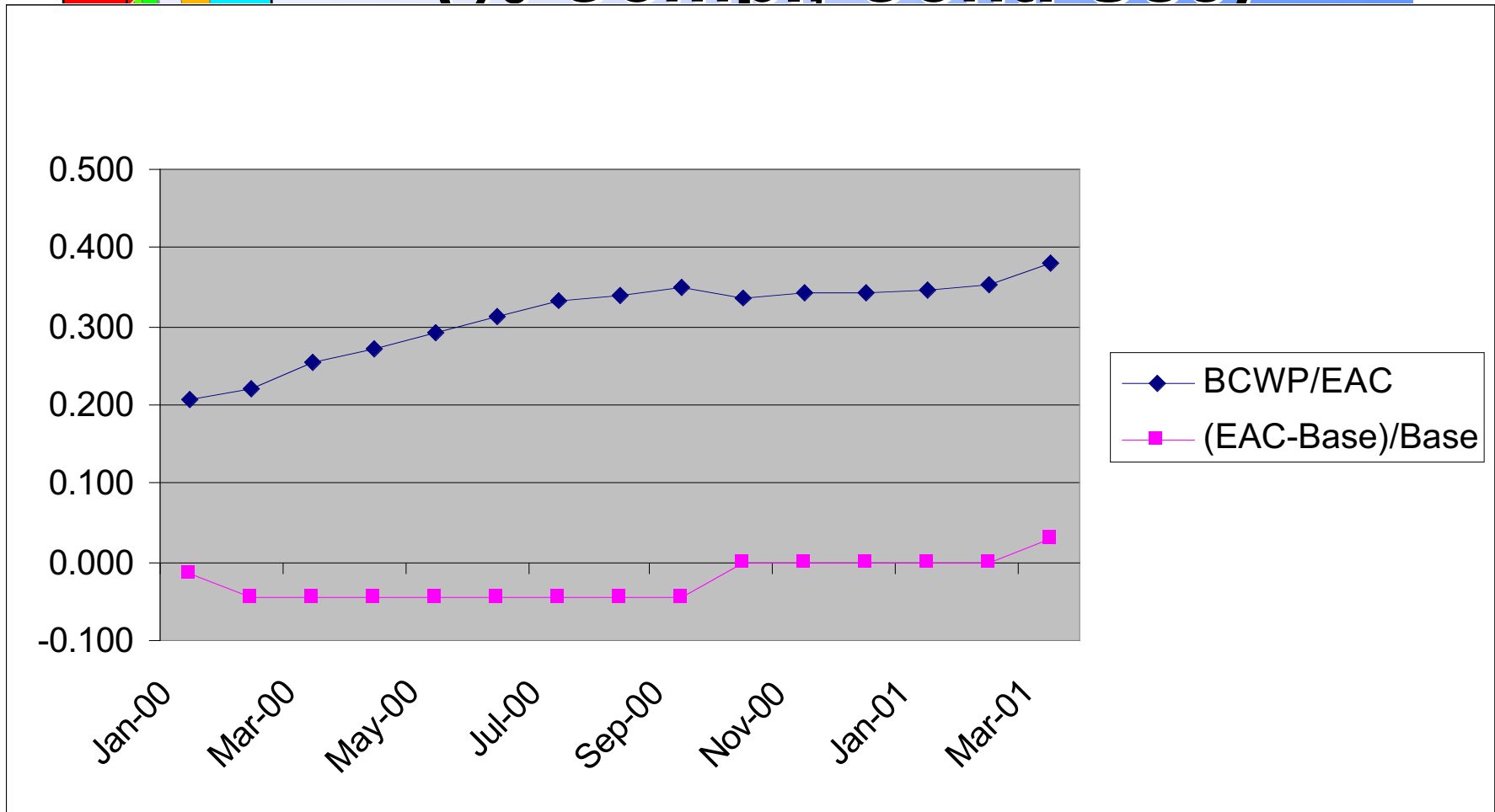


- **New Compact Muon track-finder design**
  - Will be built faster
- **Need for new Serial Link Design**
  - Replace Vitesse 7214 with 7216 -- Done





# US CMS Trigger (% Comp., Cont. Use)



**Negligible contingency use thus far**

- **Some ASICs purchased early**



# Concerns

## Installation Schedule

- New schedule has reduced installation time
- Significant time needed for integration in a synchronous pipelined system.

## Base Program Manpower

- Major effort on trigger software required
  - Tasks include monitoring/controls, diagnostics, configuration downloading and documentation, modeling, physics simulation, etc.
- Major effort on testing & installation
  - Planned as activity of base program manpower



# Plans for this year

## Muon Trigger:

- Assuming successful review of new technology:
  - Excellent results from all tests thus far
- Develop new compact single crate design
- Design 2nd generation prototype boards based on successful prototype boards already tested.

## Calorimeter Trigger

- Next generation Receiver, Elect. Iso. Cards
- Test with already built next generation backplane
- Test remaining ASIC prototypes
  - Mounted on Receiver, Elect. Iso. Cards



# Conclusions - Trigger

## Calorimeter Trigger Prototype Program

- Serial Link tests successful and final serial link card designed
- New Backplane built for revised algorithms
- New Clock Board & Receiver Card Designed

## Muon Trigger Prototype Program

- Successfully tested Port Card, Sector Receiver, Sector Processor, Backplane, Clock Board
- Track-finder integration test works with all the above boards using detailed CMS simulation data