Calorimeter Trigger

Technical Overview

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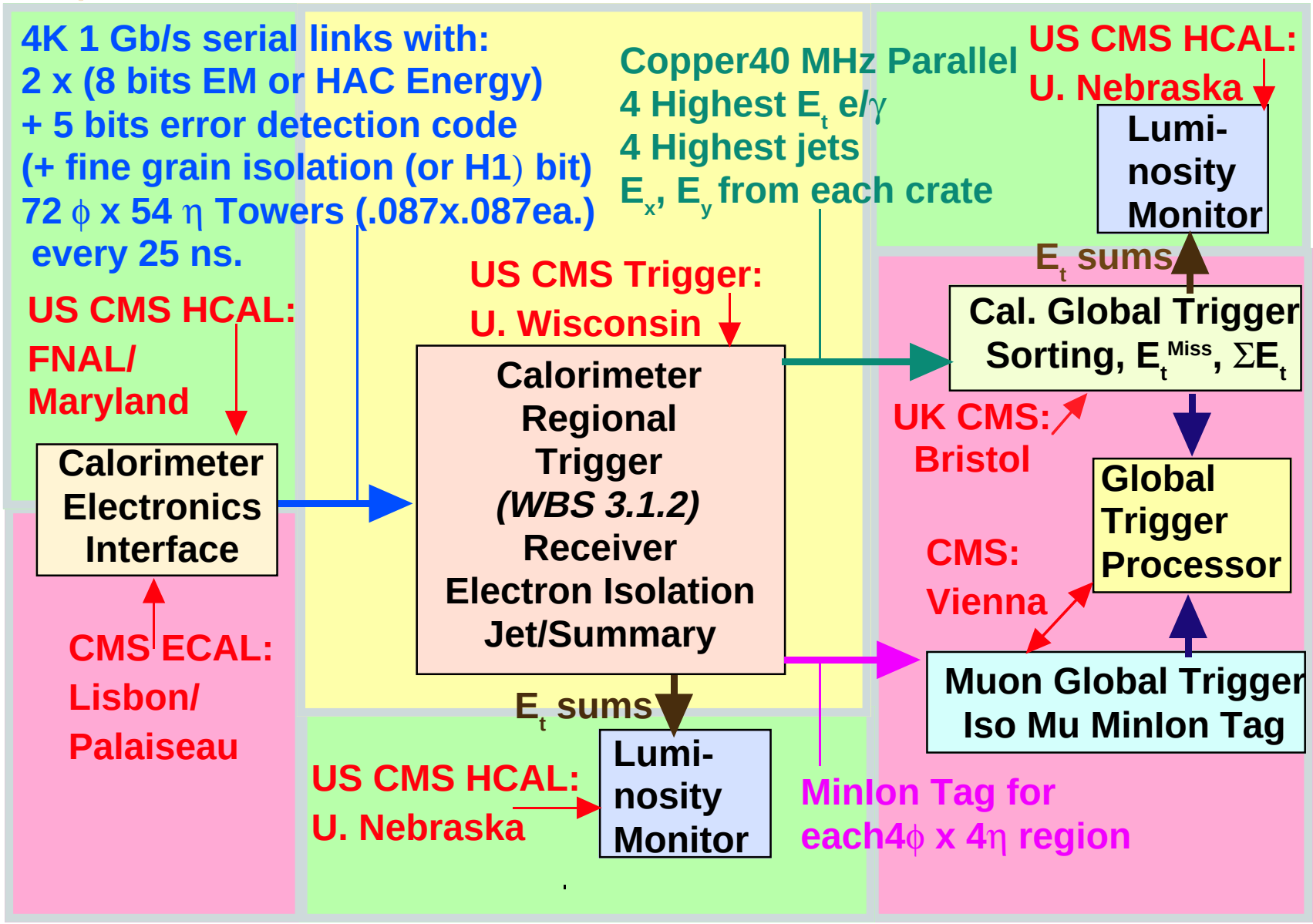
CMS Trigger Project Manager

Outline:

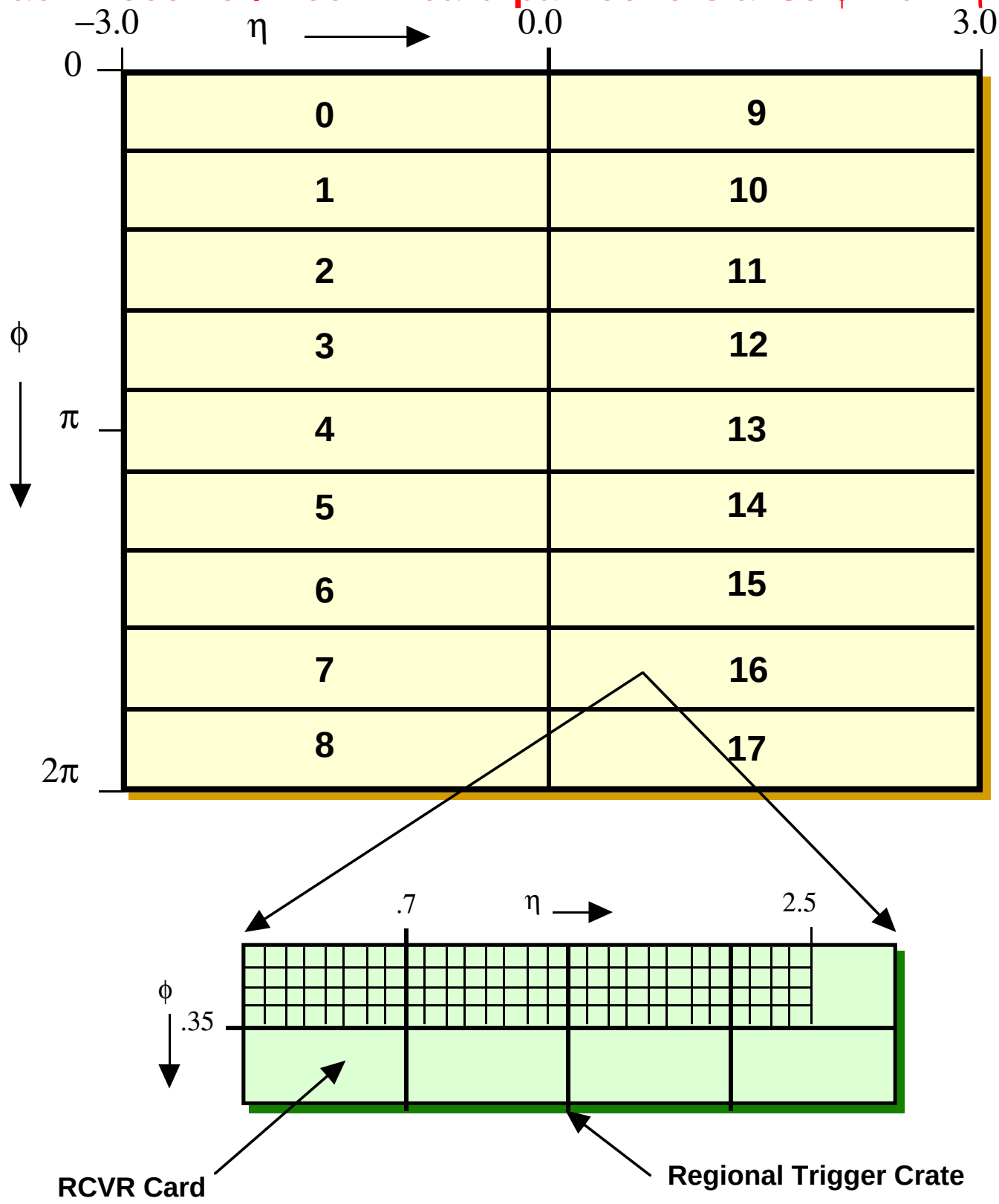
- Overview
- Description of Major Components
- Prototypes & Test Results
- Basis of Estimate
- WBS
- Schedule

Calorimeter Trigger Overview



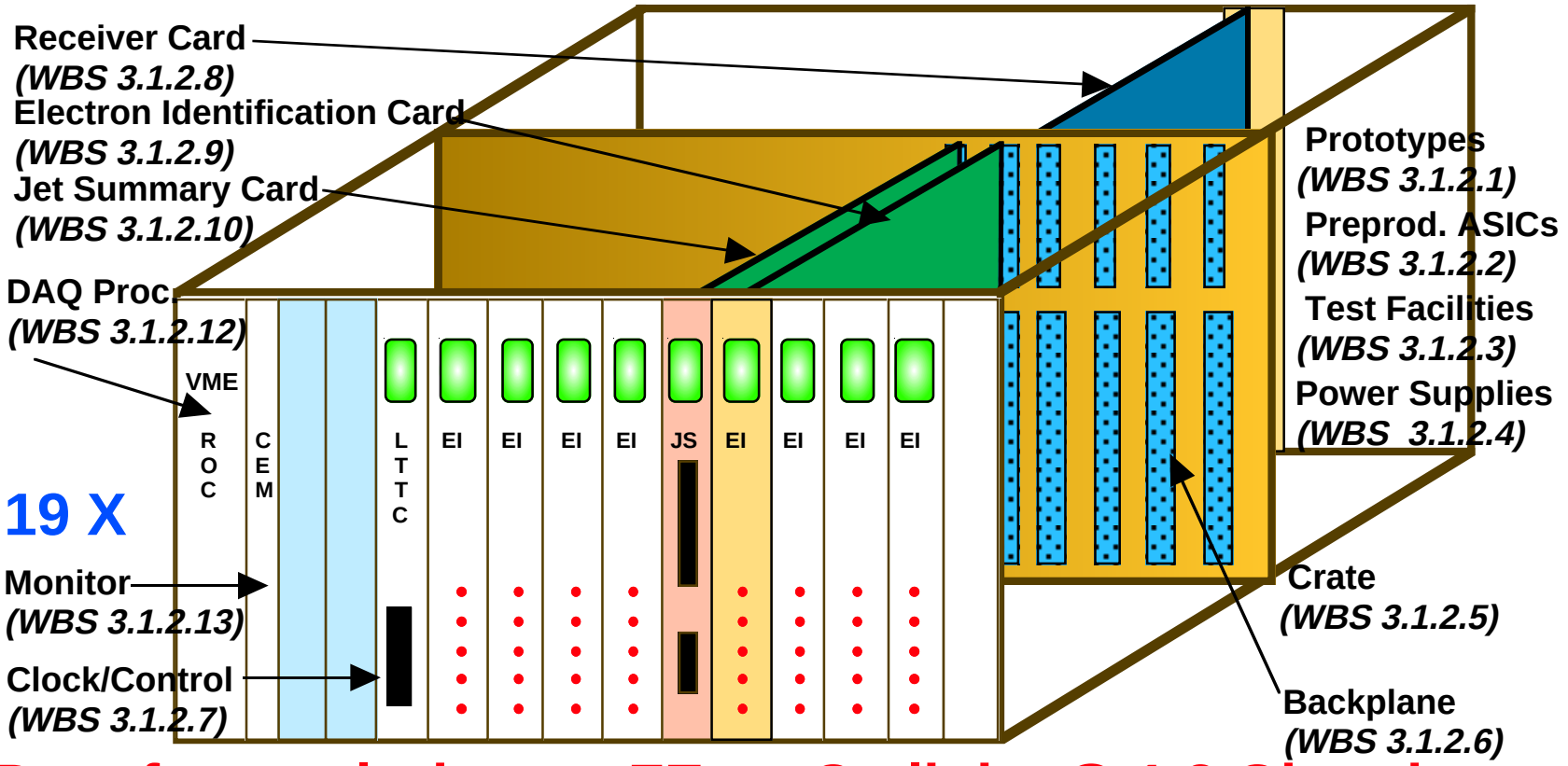
Calorimeter mapping

18 crates for barrel & endcap calorimeters + 1 for v. forward
Each crate processes 0.7 ϕ x 3.0 η region w/ 'spare' channels
Each Receiver/Elec. ID card pair covers a .35 ϕ x 0.7 η region



Regional Calorimeter Crate

(WBS 3.1.2)



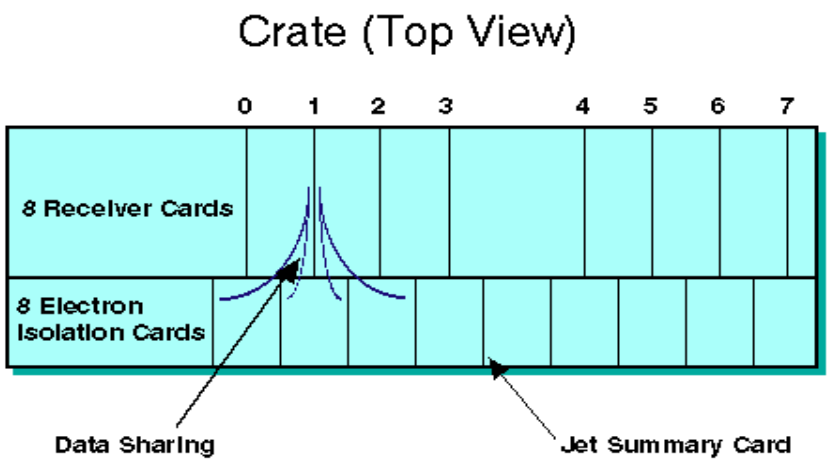
Data from calorimeter FE on Cu links @ 1.2 Gbaud

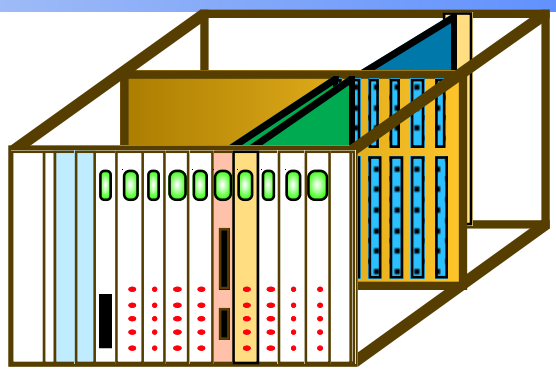
- Into 152 rear-mounted Receiver Cards **(proto. being built)**

160 MHz point to point backplane (proto. built)

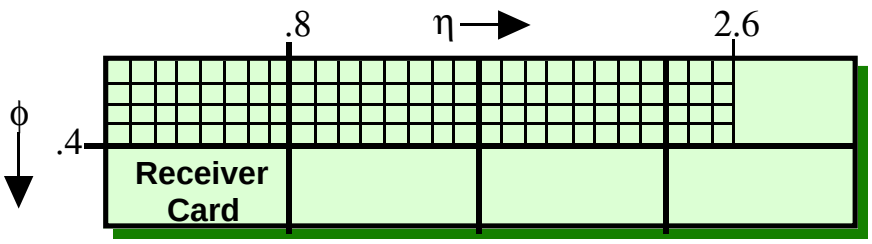
- 19 Clock&Control **(proto. built)**, 152 Electron Identification, 19 Jet/Summary, Receiver Cards operate @ 160 MHz

Receiver Card Function





Trigger Tower Mapping in Crate

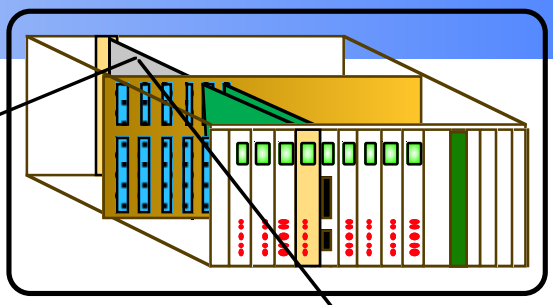


Design optimized to forward data for further processing only at appropriate resolution and only on need-to-know basis.

Receiver card

- Receives 8-bit non-linear E_t + 1-bit ID data from 32 ECAL & corresponding HCAL trigger towers.
- Linearizes ECAL & HCAL E_t & prepares data for subsequent processing by Electron ID Card.
- Stages this & neighbor tower data to Elec. ID card.
- Linearizes ECAL and HCAL E_t on 8-bit scale and uses Adder ASIC to make 4x4 sums for jet and missing E_t triggers.
- ORs ECAL fine-grain EM ID and HCAL Muon ID bits separately for each 4x4 region.
- Stages 4x4 region data to Jet/Summary cards.

Receiver Card - Rear



32 Channels = 4 Ch. x 8 daughter cards
1.2 GBaud copper receivers
18 bit (2x9) data + 5 bit error det. codes
Vitesse 4-channel Interconnect Chip
On-board cable/connector equalization
Output signals on 340-pin AMP Stripline
VME control on 128-pin DIN

Input Connector

9U x 400 mm

VME Control

DC/DC 3.3V

DC-to-DC Converter

Daughter Card

Vitesse Interconnect Chip

AMP Stripline High Density Connector

power

Cable Equalization (2 circuits on front & back)

Under-board connectors

V 7214

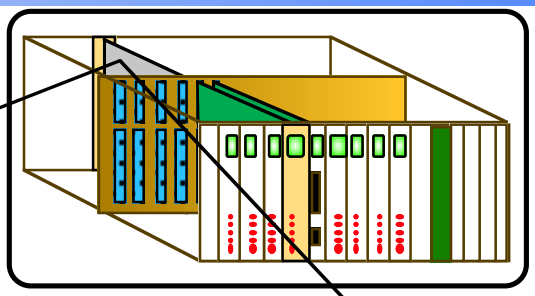
EQ

signals

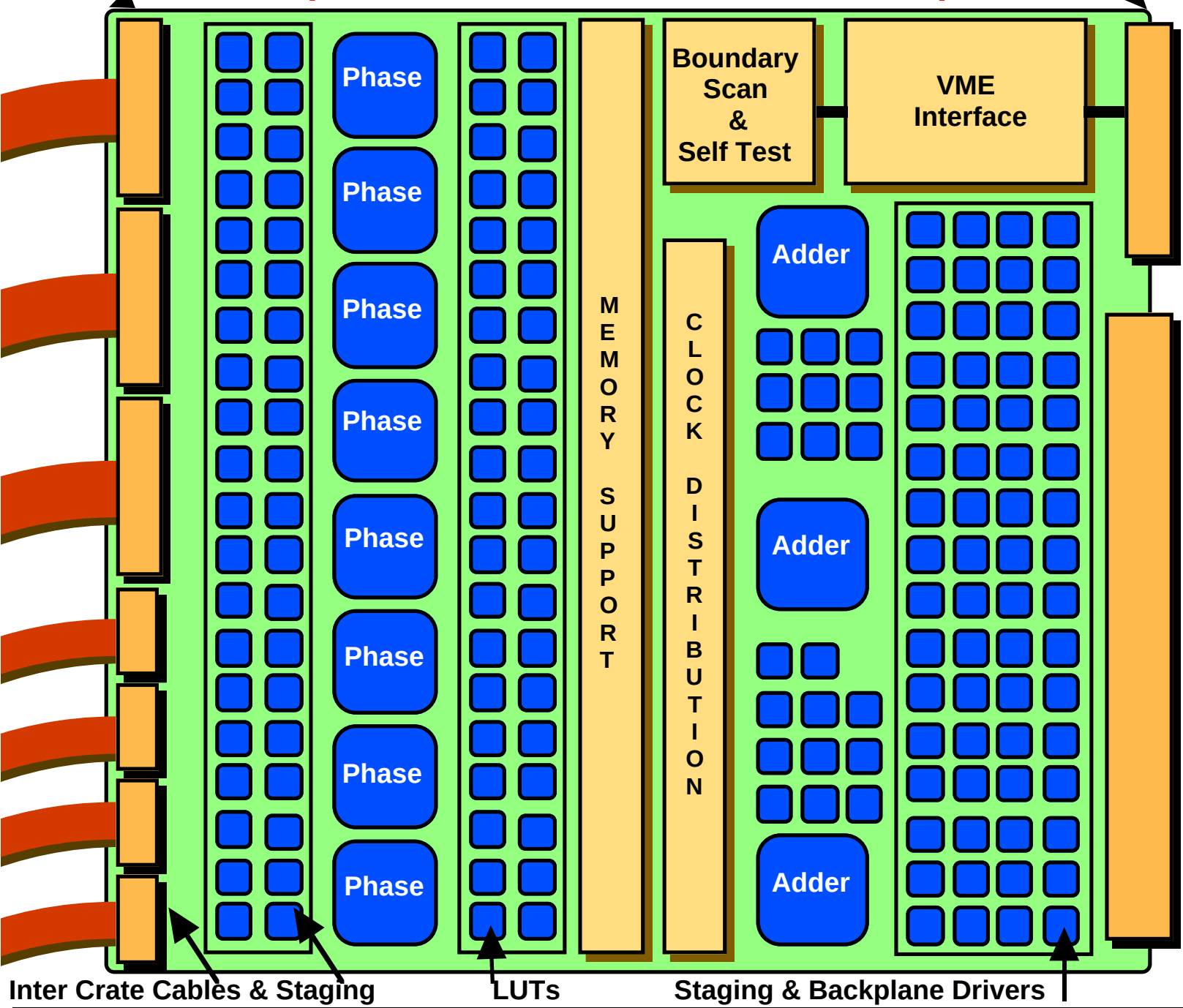
design by J. Lackey

Receiver Card - Front

Data from Rear @ 120 MHz TTL
Phase ASIC: Deskew, EDC,
Mux @ 160MHz ECL, Test vectors
Error logic bit for each 4x4
Memory Lookup tables @ 160 MHz
Adder ASIC: 8 operands @ 160 MHz
Differential Outputs @160 MHz: 340 Pin AMP Stripline conn.

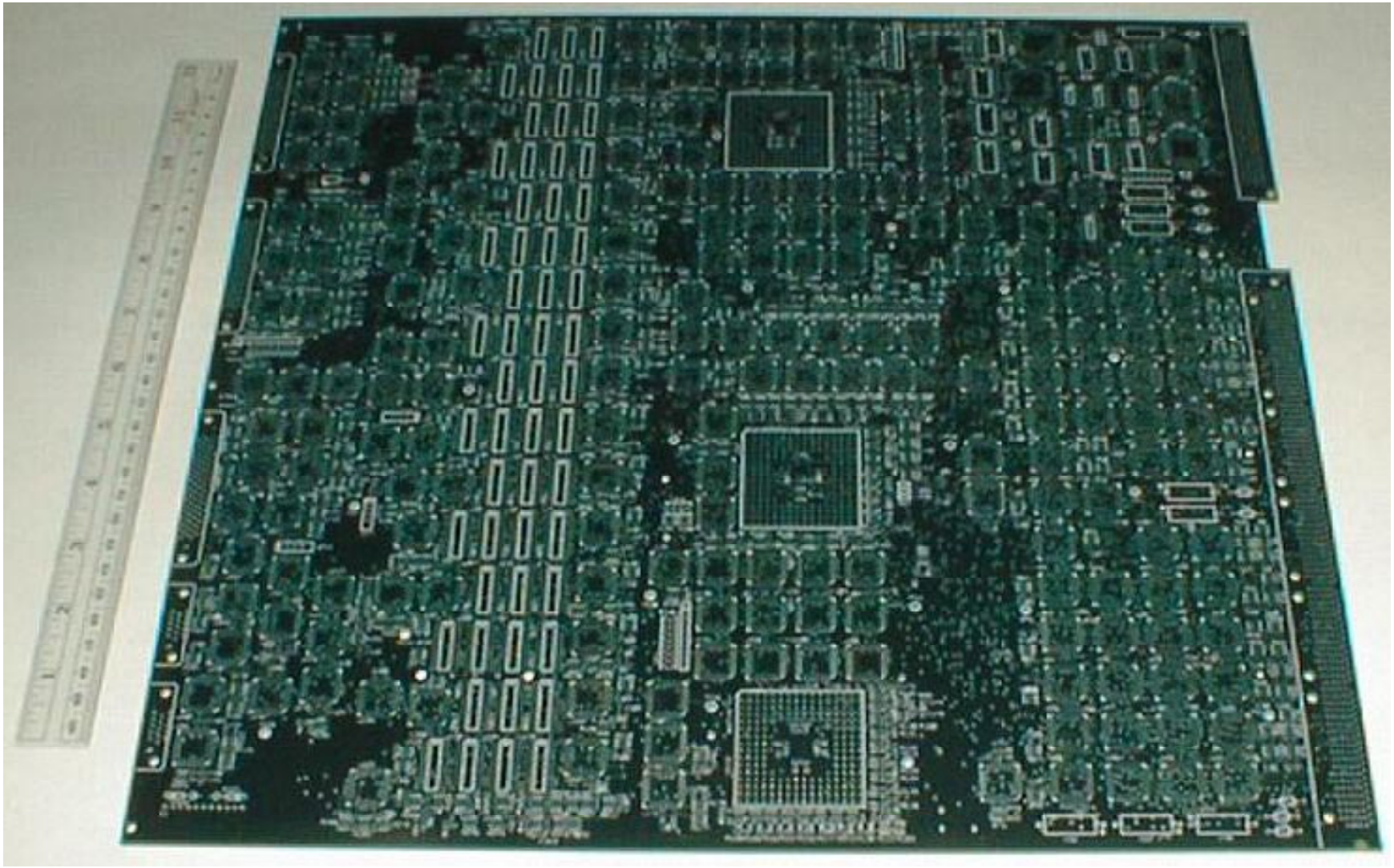


design by J. Lackey



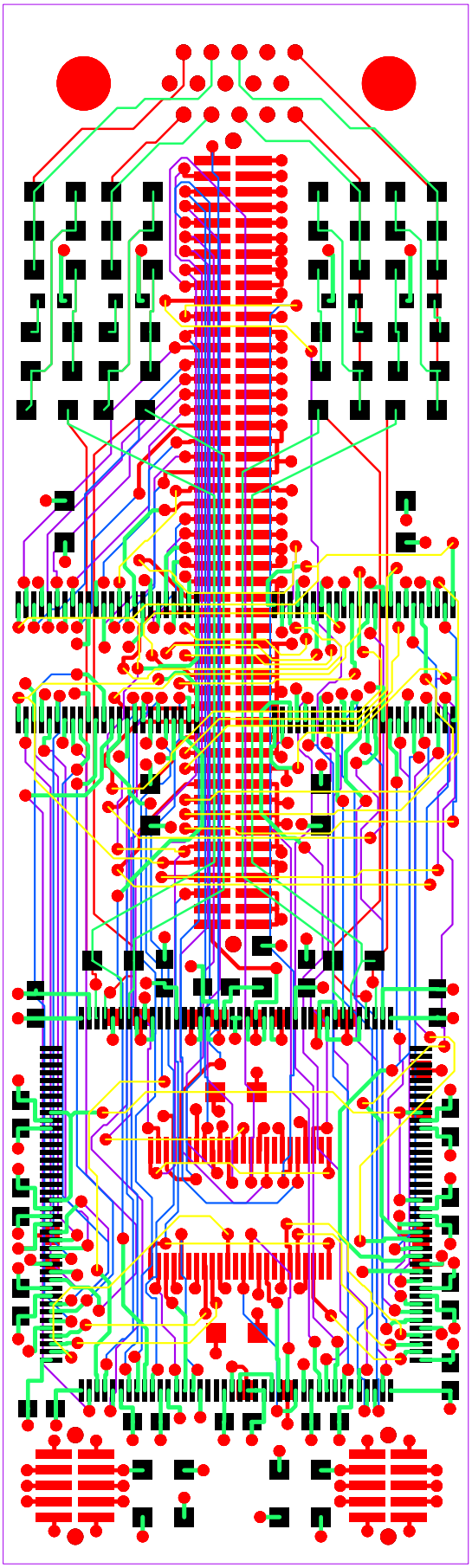
Receiver Card Prototype

Card built, assembly next



Receiver Daughter Card

Layout Complete

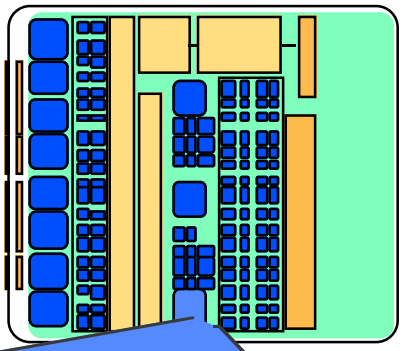


8 x 13-bit 160 MHz Adder ASIC

Vitesse 0.6μ H-GaAs Process: ECL I/O

- 13 bits per operand x 8 operands
- Single thirteen bit output
- Latency: 25 ns @ 160 MHz
- Full Boundary Scan support

Receiver Card:

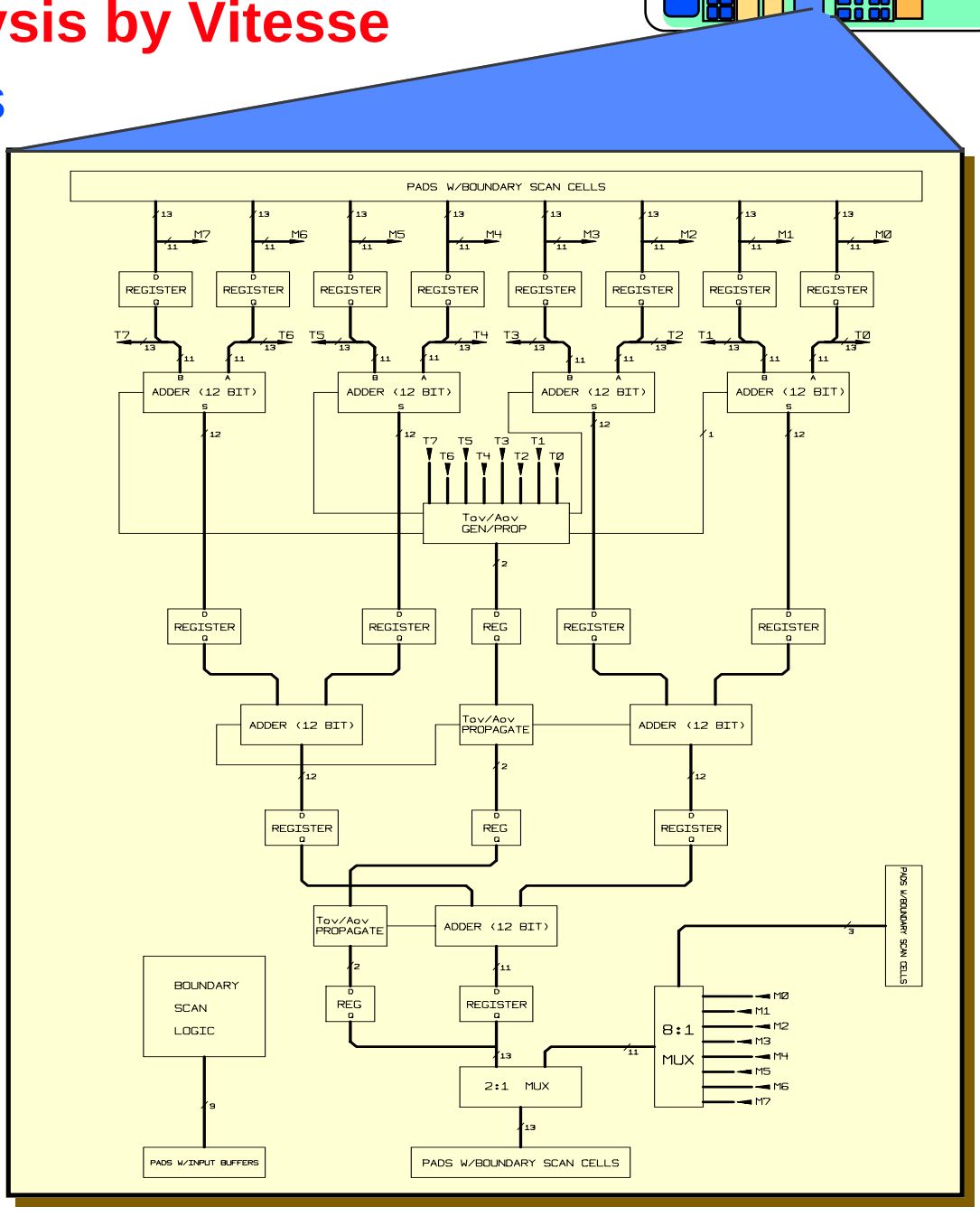


Technical analysis by Vitesse

- ~11,000 cells
- 4 Watts
- 308 MHz

Status:

- 5 tested devices delivered
- select nets exceed simulation speed by 10%

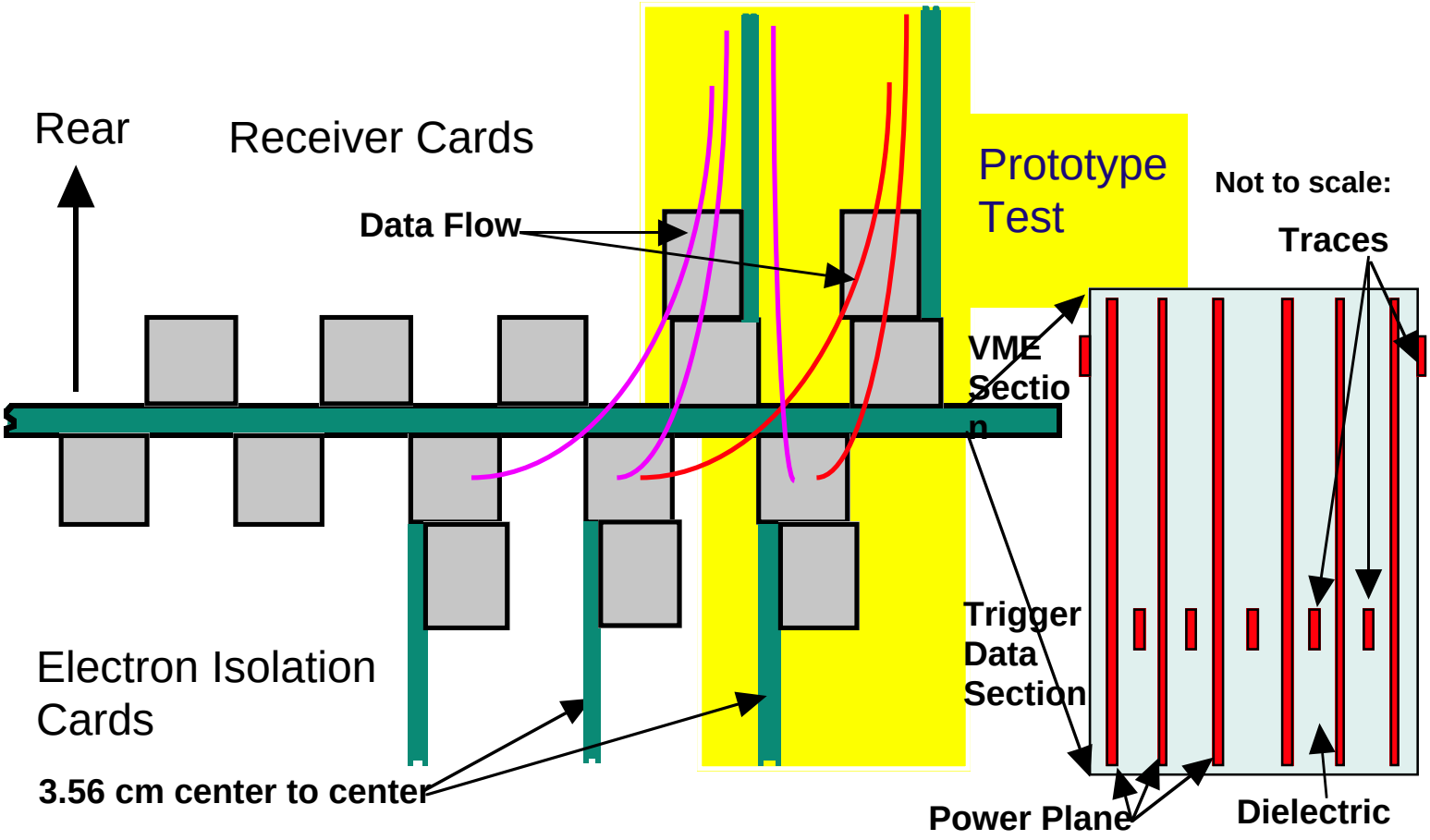


- J. Lackey

160 MHz Backplane

Monolithic 9U High Backplane

- Incorporates std. 32 bit VME in top connector position
  - Single 128 pin DIN in Trigger Processor Card area
  - Two 96 pin DIN connectors in left most slot positions
- Data sharing on backplane
  - Reduces the number of receivers, serial to parallel convertors, and synchronizing circuits
- Stripline construction w/ five ground and power planes
  - 50 Ω impedance to match connectors and boards
  - 1 oz. copper with multiple power points
- Five signal layers
  - Handles routing density thru connector pins
  - Differential pairs are held to the same layer
  - Point to point on high speed data paths @ 160 MHz



Prototype electronics

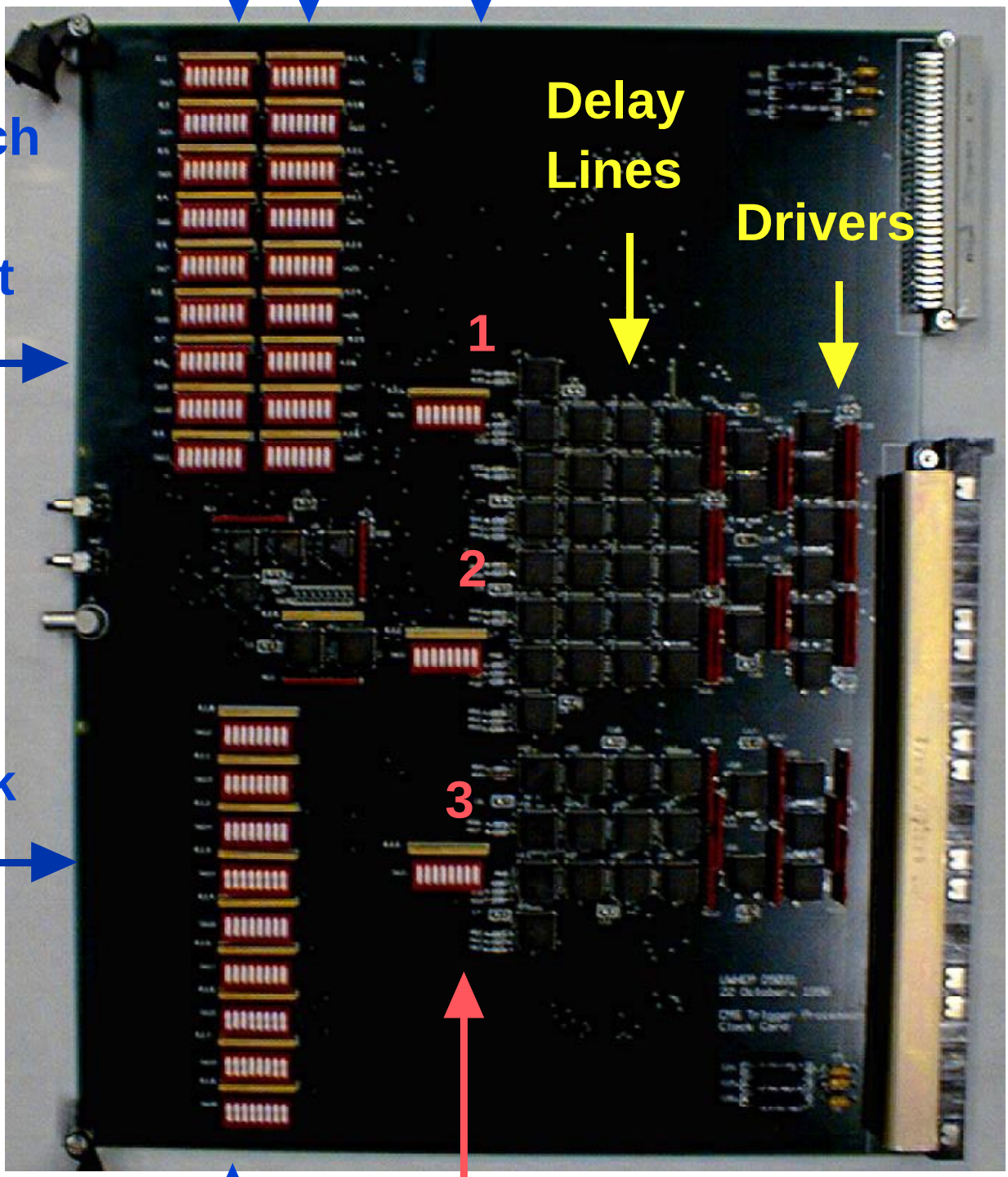
The critical components that need to be tested before final design are:

- **Backplane with differential point-to-point 160 MHz links**
  - Already built. Clock lines have been tested with a prototype clock card (built). Rise and fall times = 0.8 ns for 20-80% signal change.
  - Detailed tests with multiple data links operating are awaited
- **ASICs running at 160 MHz**
  - Built Adder ASIC. Tested by Vitesse.
  - Tests, in circuit & using boundary scan, will be made on the prototype receiver card
- **Receiver Card**
  - Test Input Serial Data on Separate Daughter Card
  - Test Adder Chips
  - Test Dataflow in/out of backplane
  - Card submitted for manufacture

Prototype Clock Board

switches to set delay lines

- J. Lackey & M. Jaworski
U. Wisconsin

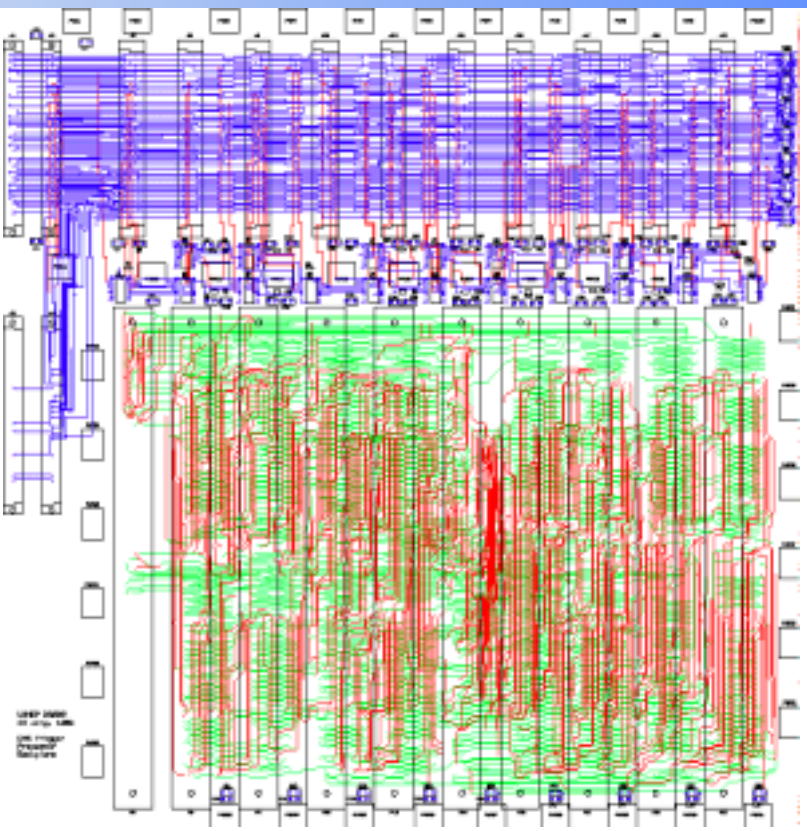


4 Recvr Cards, 4 Electron Iso, 1Jet/Sum

160 MHz Backplane Prototype

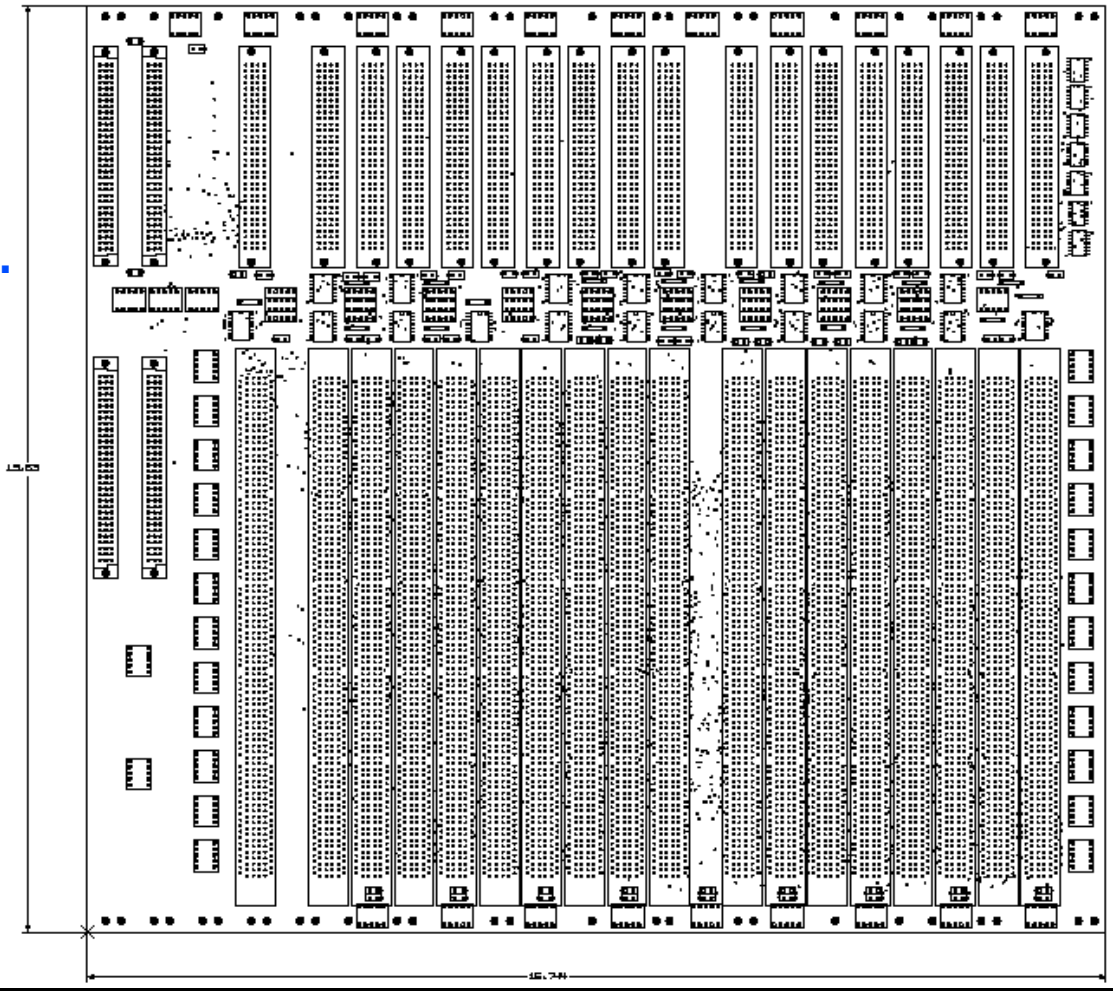
Display 3 of 5 signal layers:

(most signals are hidden by top layer)



Board layout:

(Alternate connectors on opposite sides)



std. 2 conn. VME area

single VME connector

trigger processing area

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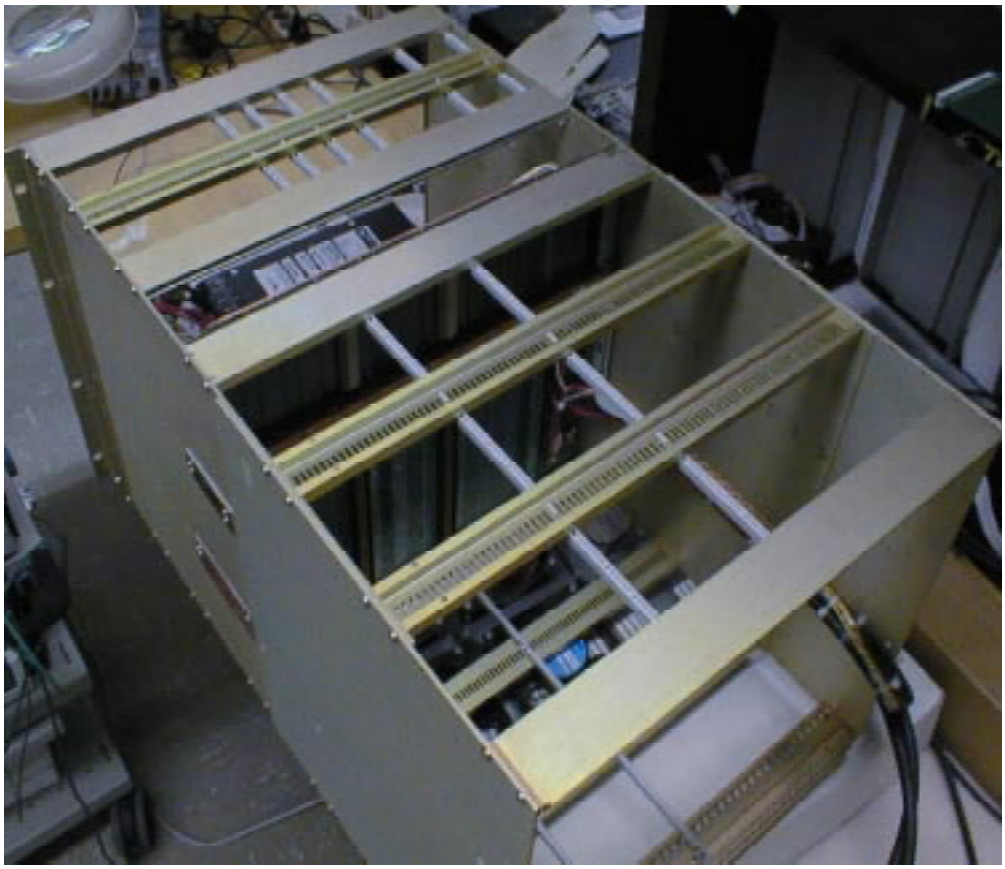
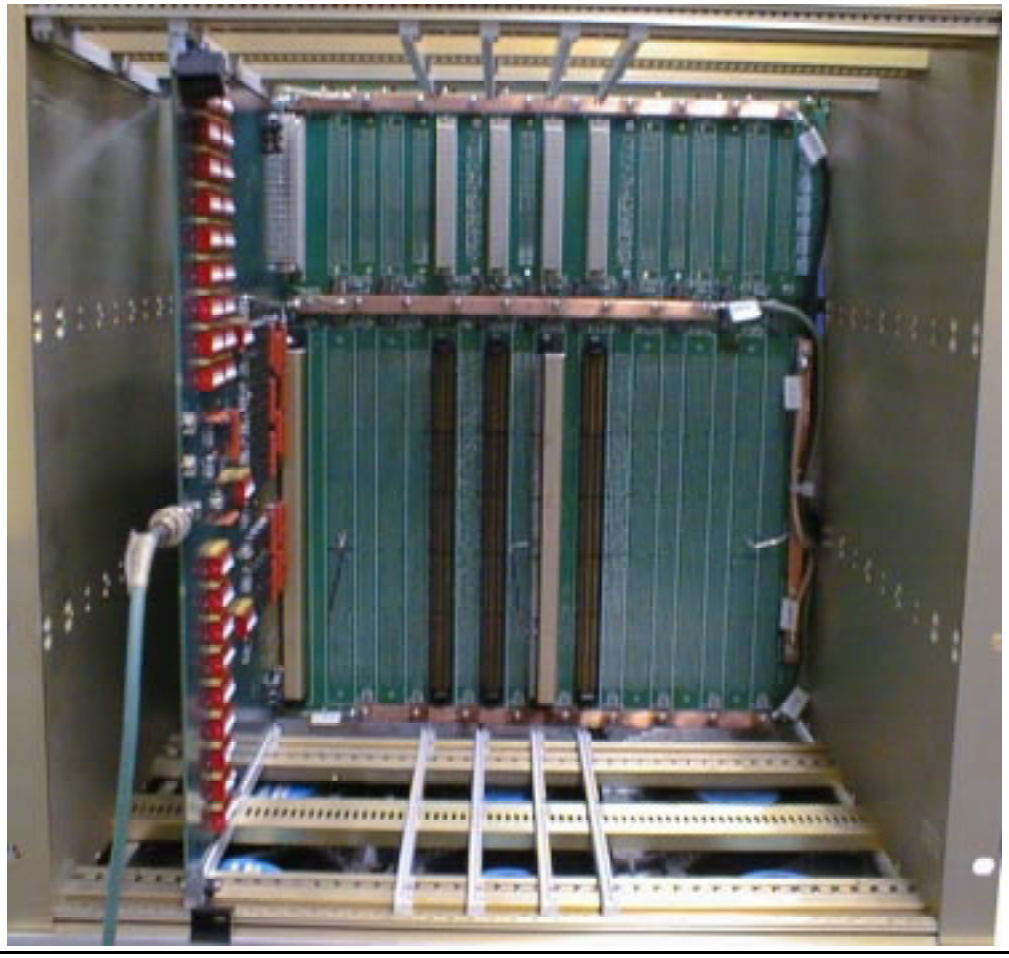
Backplane Test Setup

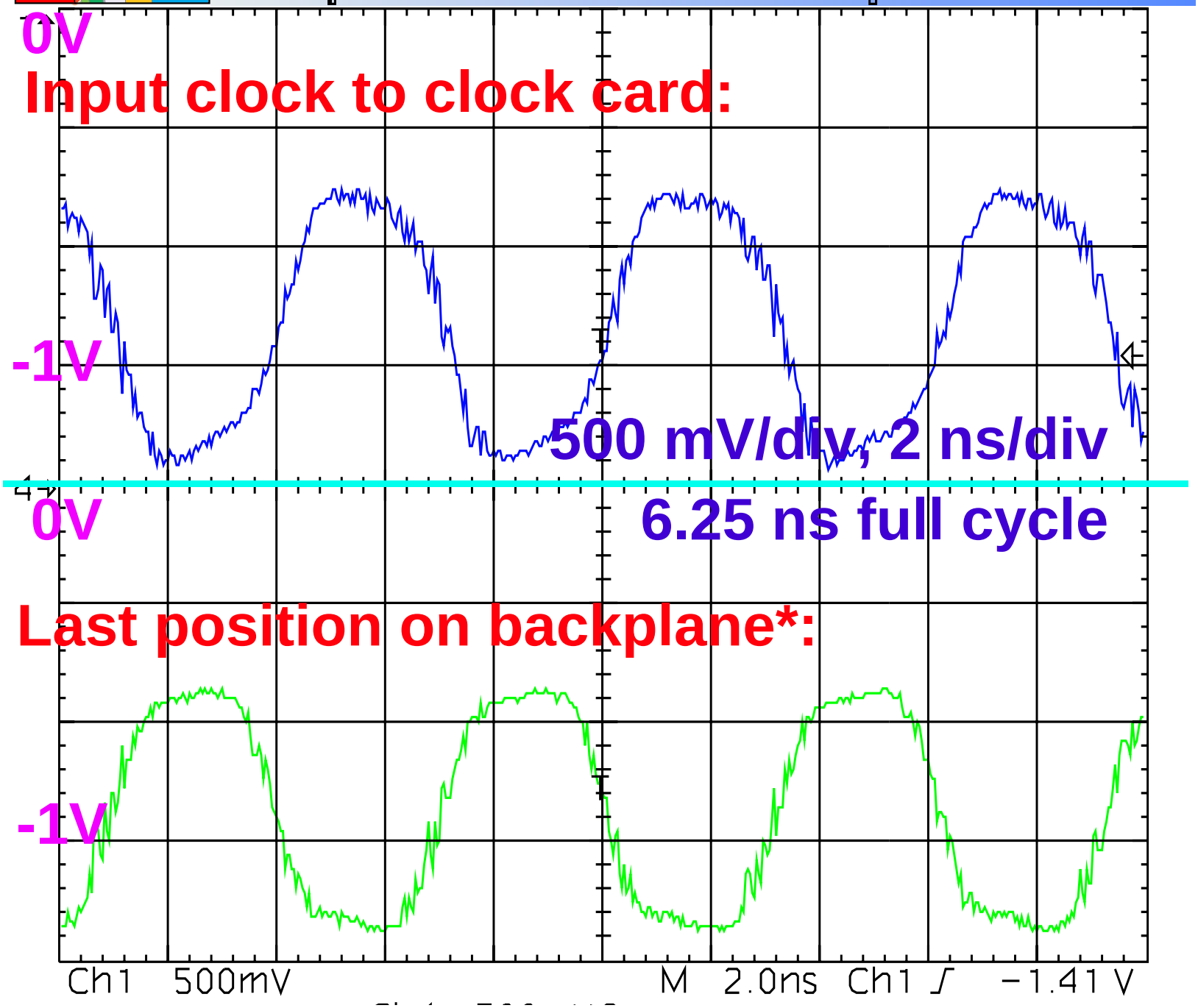


Top rear view of crate & backplane with power supplies



Front view of crate & backplane with clock board installed

Backplane Test Results



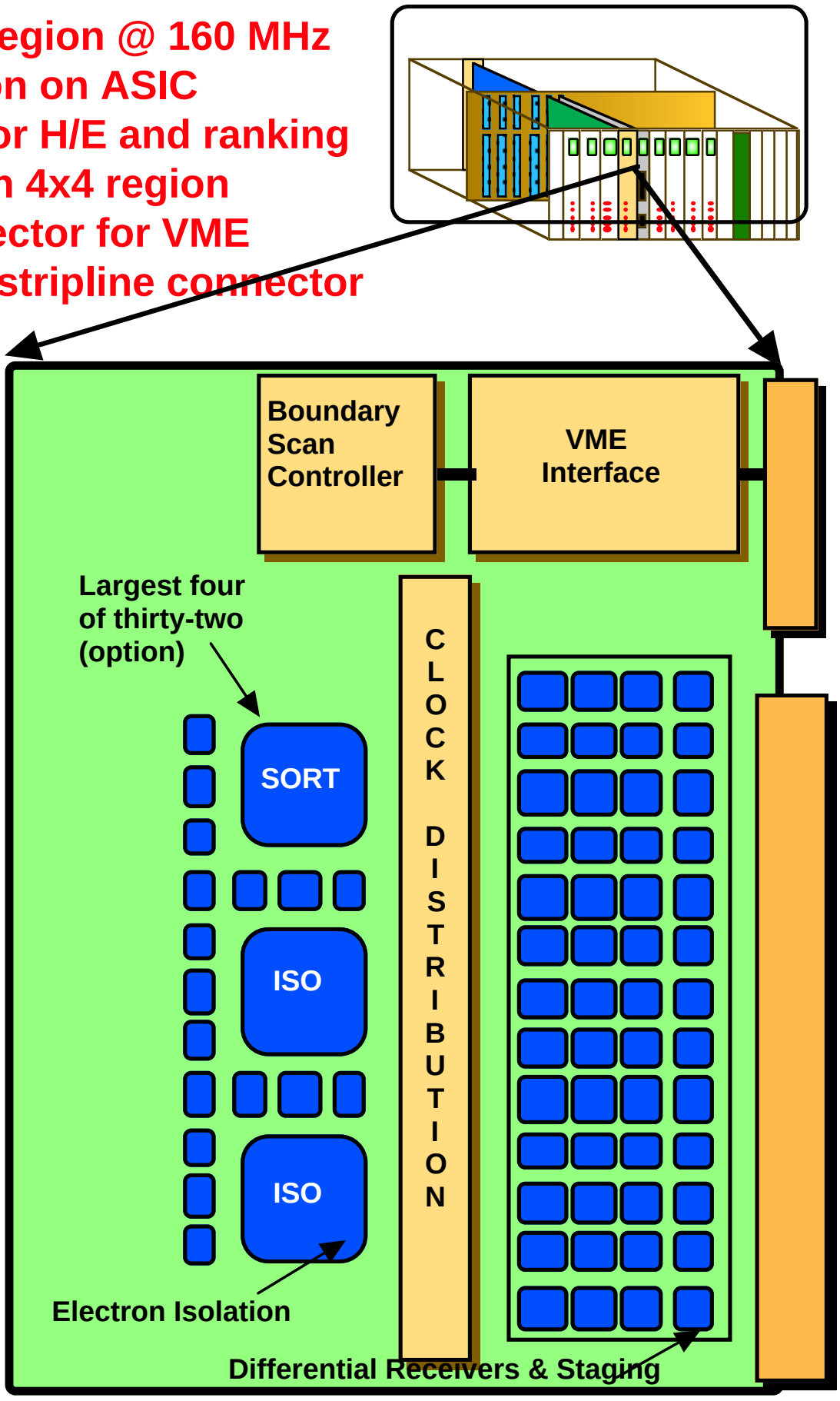
*one side of differential pair

Conclusions:

- Output of backplane rise 820 ps
- Output of backplane fall 840 ps
- Measured 20% to 80%

Electron Identification Card

Processes 4x8 region @ 160 MHz
Electron isolation on ASIC
Lookup tables for H/E and ranking
Find Max in each 4x4 region
4-row DIN connector for VME
340 signal AMP stripline connector for dataflow
9U x 280 mm



Electron Isolation ASIC

Each ASIC handles a 4 x 4 region

Two ASICs per card handle a 4 x 8 region

There are 20 nearest neighbor towers for each 4 x 4 region

Inputs - EM @ 160 MHz

Four EM energies per cycle
1st cycle: 4 top nearest neighbors
Next 4: Left edge and Right edge
6th cycle: 4 bottom nearest neighbors

Inputs - HAD @ 160 MHz

Each cycle: 4 HAD
1st cycle:
6 Top nearest neighbors
Next 4:
Left edge & Right edge
6th cycle:
Bottom nearest neighbors

Outputs - EM per 160 MHz cycle

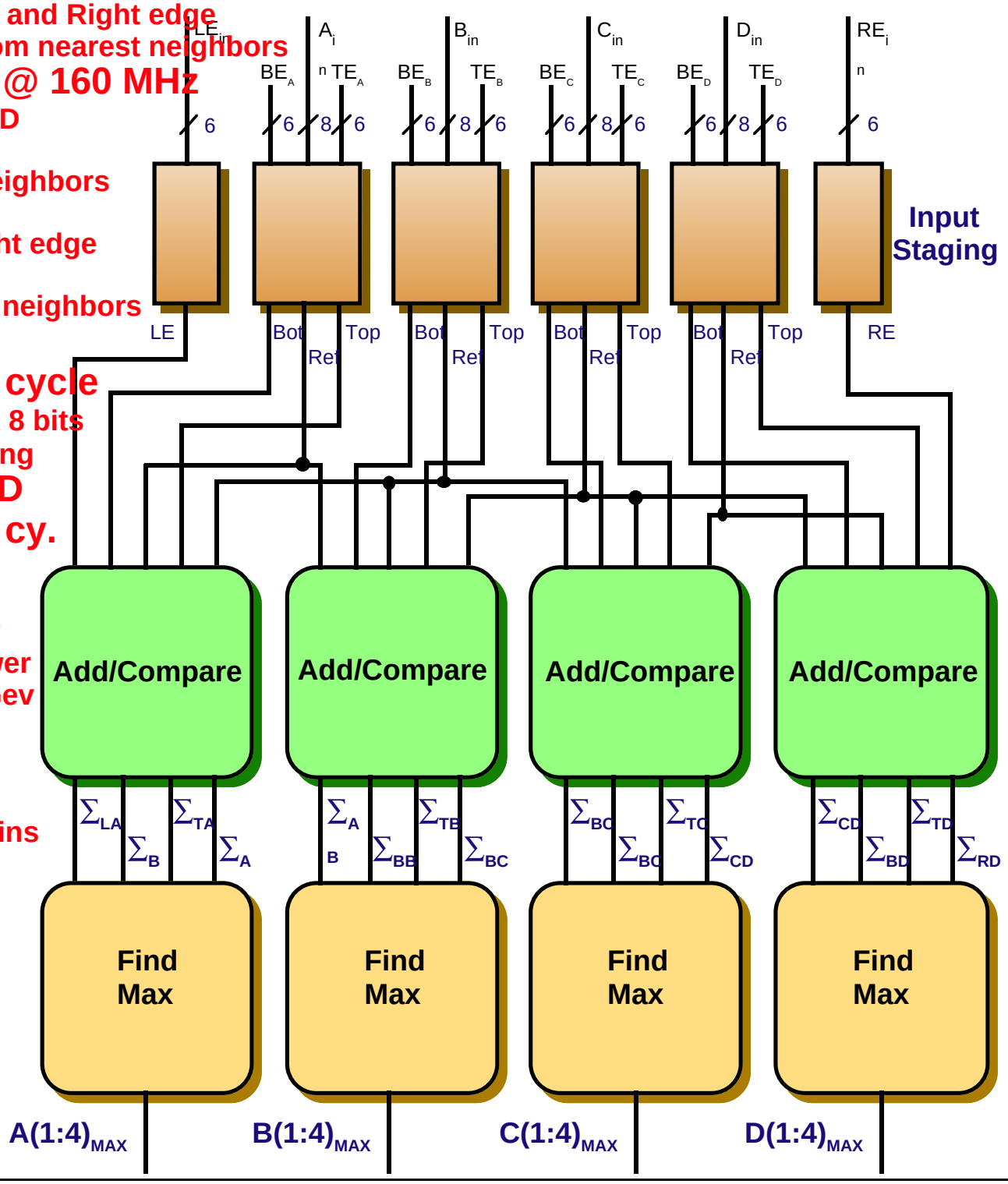
4 2-tower sums x 8 bits
no double counting

Outputs - HAD per 160 MHz cy.

Four 1 bit results indicating eight nearest neighbor sum for each tower is less than 1.5 Gev

Package:

256 pin LDCC
with 180 signal pins
FX100K
Vitesse array



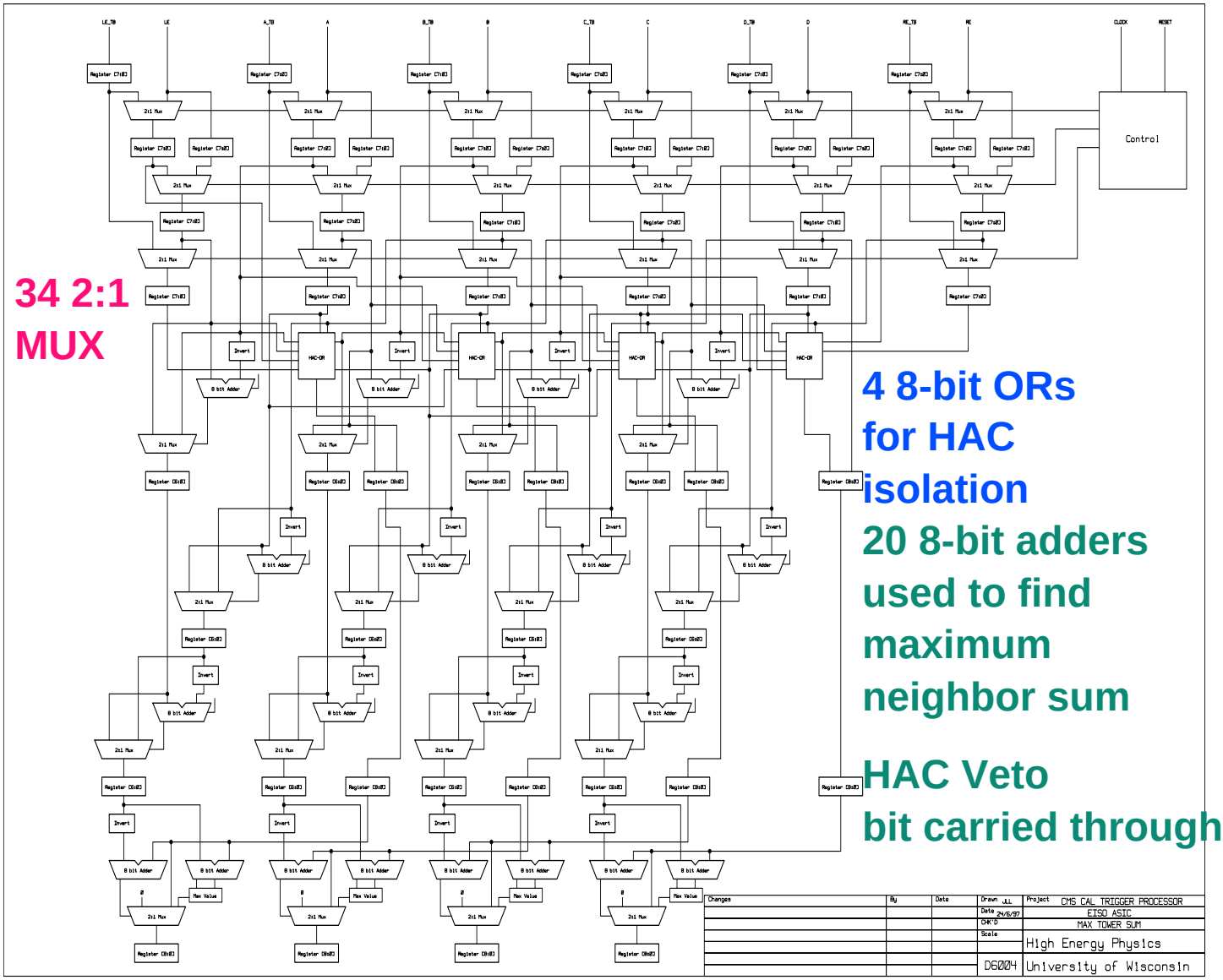
- J. Lackey

Electron isolation ASIC status

Generated a detailed design for the EI ASIC
Produced a cell count, pin count and power estimate (5 Watts)
Size, power and cost considerations produced a refinement in electromagnetic isolation algorithm
Request for bids is ready -- on hold for Receiver Card tests (uses data)

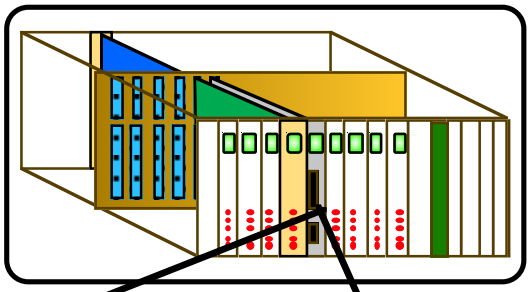
160MHz 4x4 channel EI ASIC

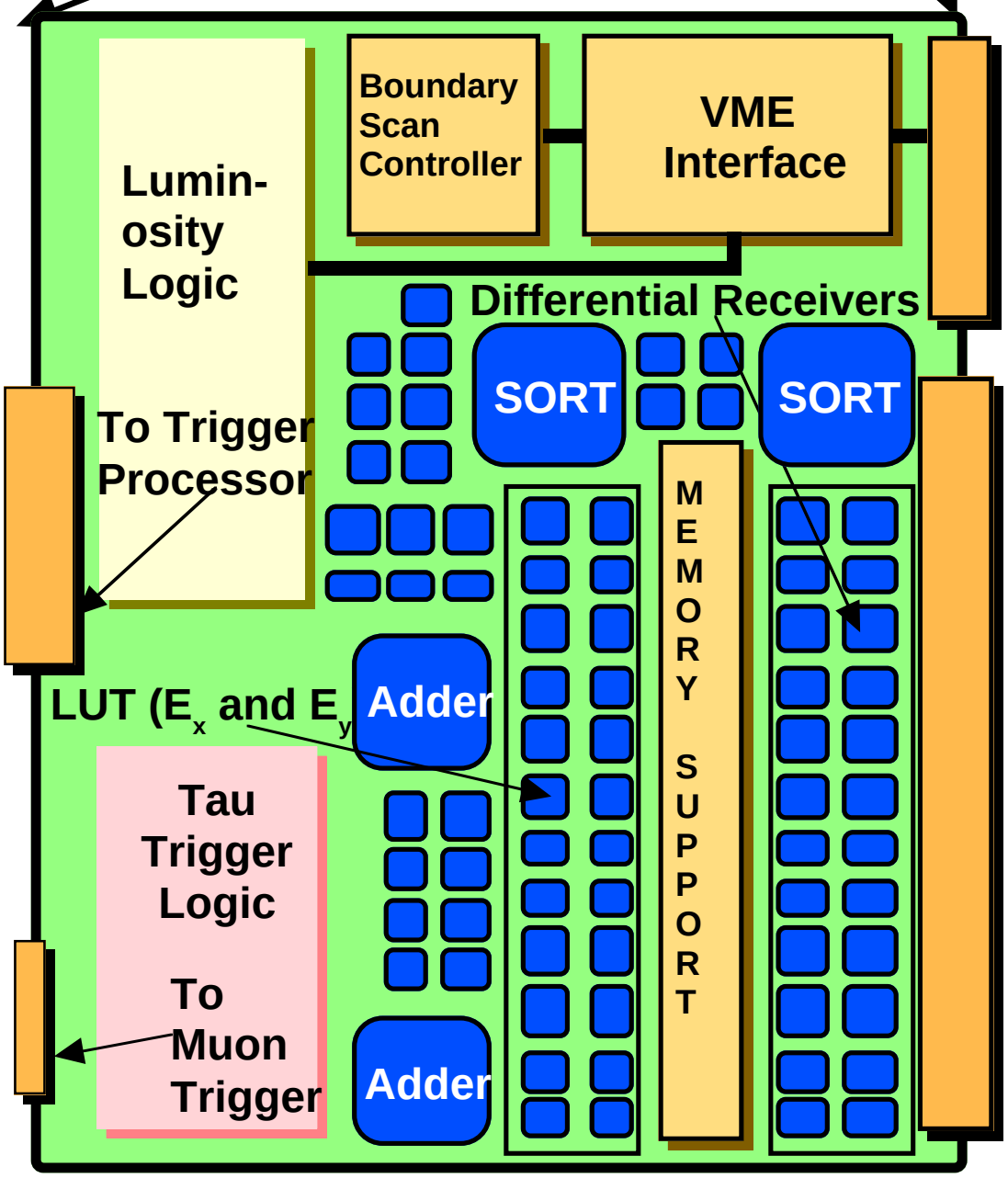
Max tower sum, HAC Veto and HAC isolation circuit.



Jet/Summary Card

- 9U x 280 mm card summarizes full crate
- Sorts 32 electron ranks to find top 4 in crate
- Sorts 32 4x4 E_t sums to find top 4 jets in crate
- LUTs generate E_x & E_y from E_t for 4x4 region
- Adder tree for crate E_t, E_x and E_y sums
- Quiet/MinI bits for each 4x4 region
- Reserved space for Tau and Lumi sums
- 40 MHz output to global and muon systems





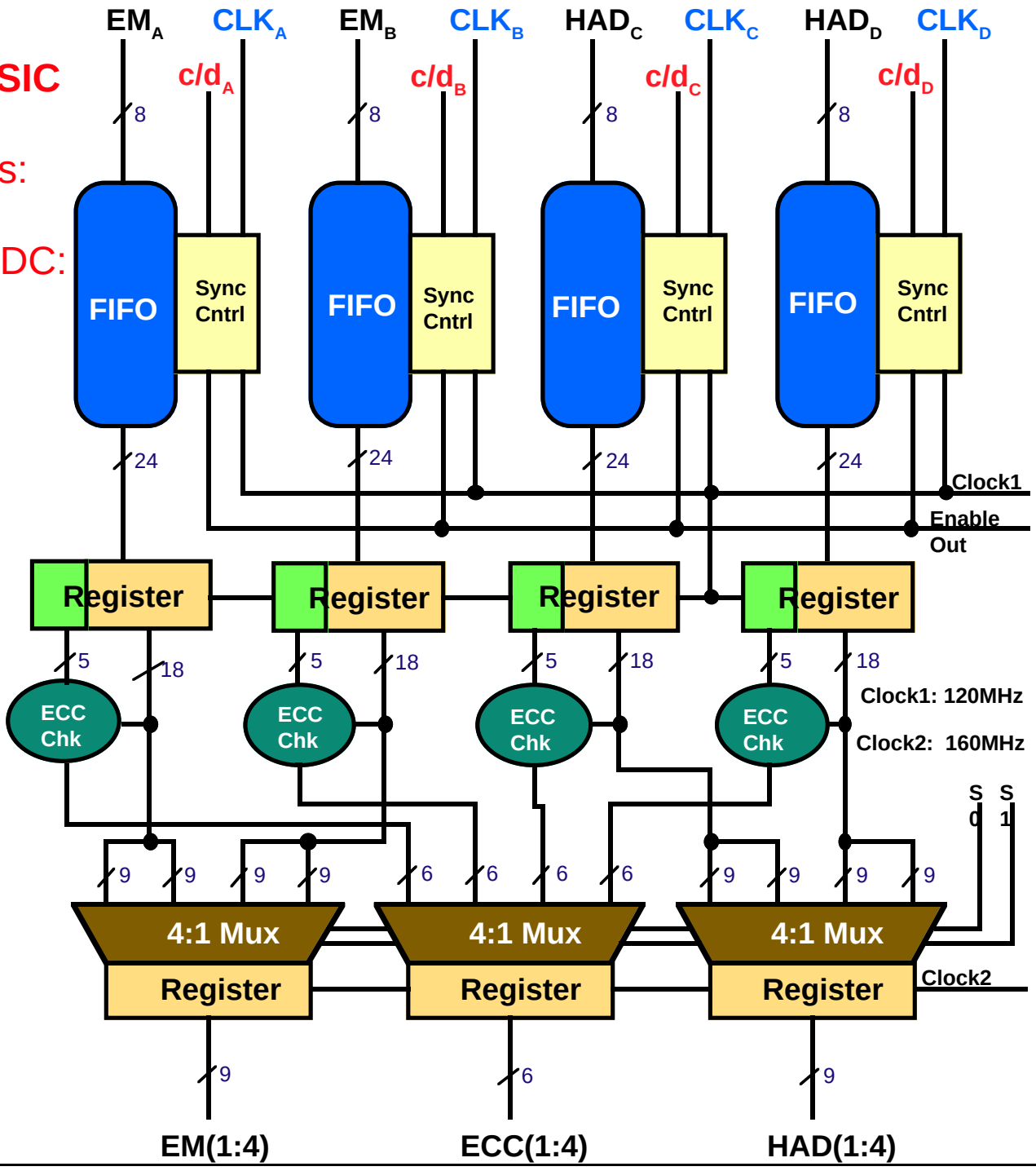
Phase ASIC Design

Each ASIC takes 4 EM or HAD inputs:

Input - Data arrives @ 120MHz: 8 bits wide x 3 cycles
24-bit frame: 18-bit data + 5-bit error detection code
8-bit energy + 1-bit fine-grain ID per channel + 1 spare
The input clock for each channel is derived from the Vitesse Receiver

Output -
Data leaves ASIC @ 160MHz:
2 data channels:
9 bits each
One channel EDC:
1 bit error
5 bits parity

Technology
GaAs
w/ECL I/O
& TTL input



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Sort ASIC Design

Finds the 4 largest of thirty-two values

Sorts electrons by rank

Finds the 4 largest E_T from sixteen 4 x 4 regions

Inputs

Eight 10-bit ECL inputs @ 160 MHz. Four cycles to read in thirty-two values

Each input has 5 bits added:

3: which input of eight

2: which cycle of four

Outputs

Four 15-bit ECL outputs are produced @ 40 MHz

Five bits added to each 10-bit result:

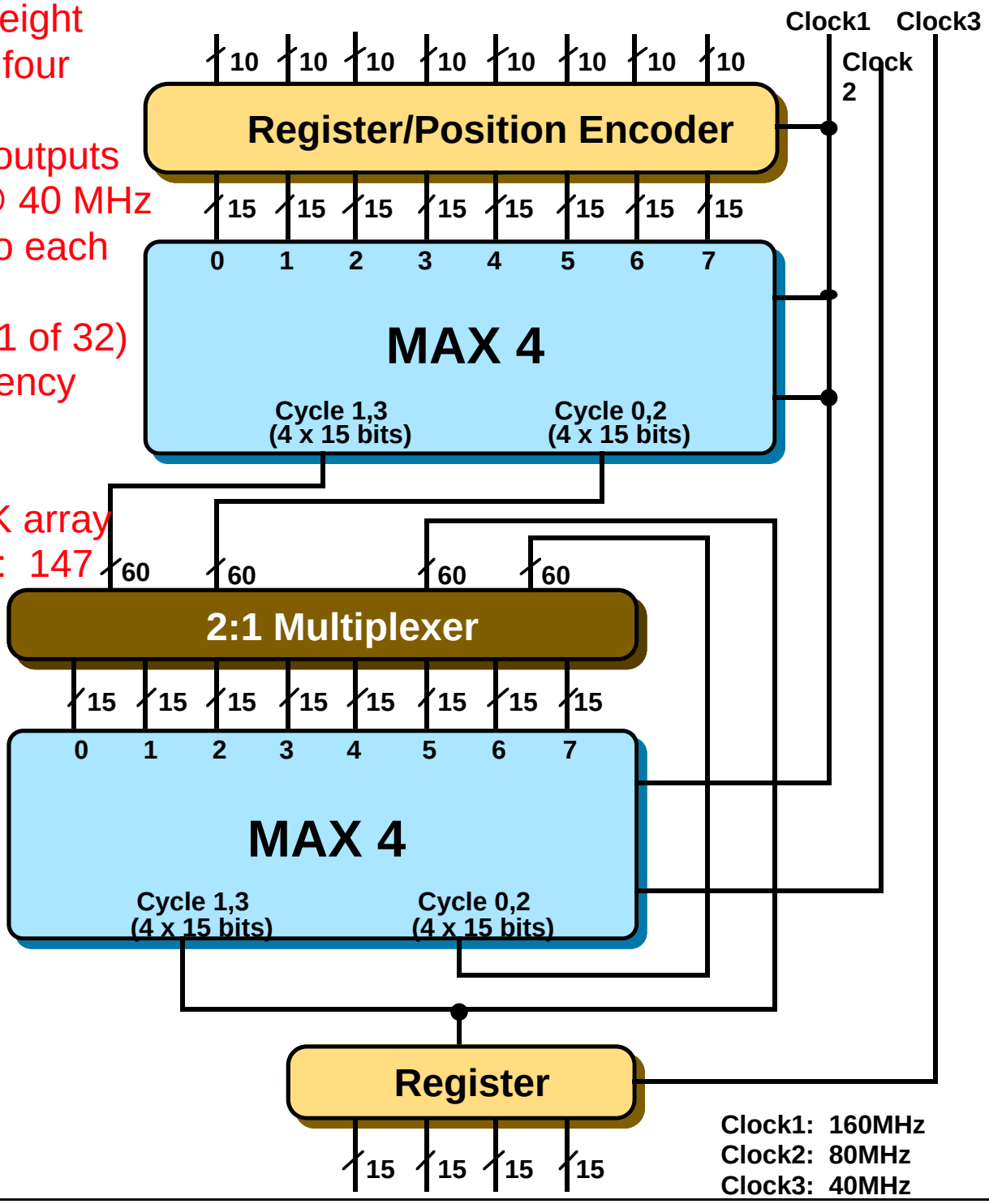
tower address (1 of 32)

Four crossing latency

Package:

Vitesse's FX100K array

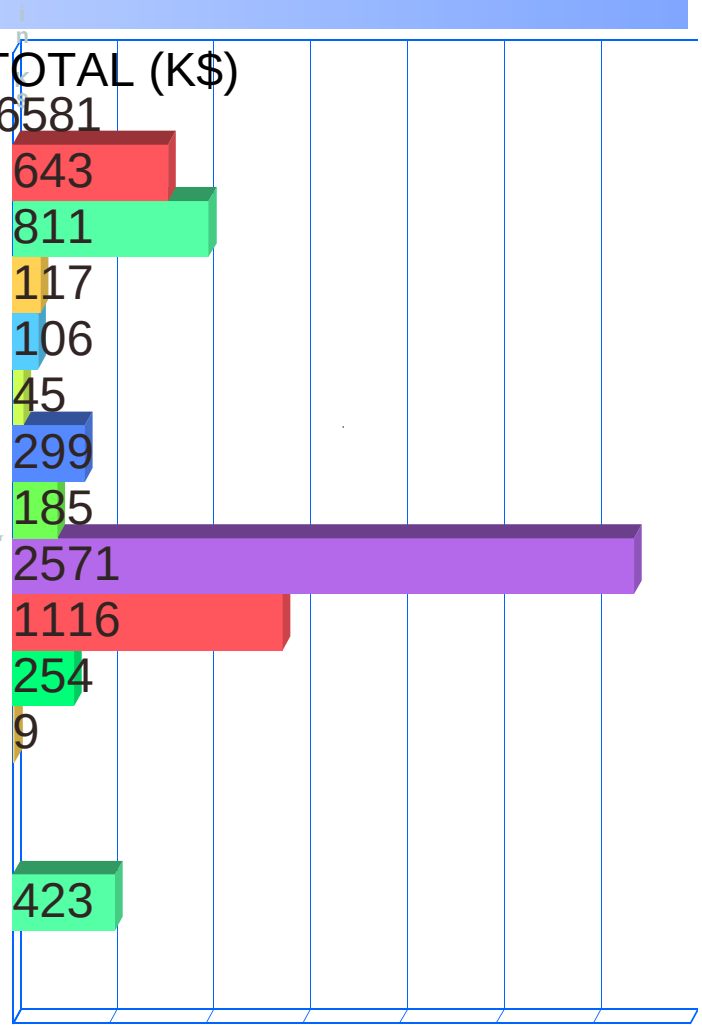
Signal Pin Count: 147



- J. Lackey

Calorimeter Trig. Costs at L4

WBS	ITEM	BASE(K$)	Cont(%)	TOTAL (K$)
3.1.2	Cal.Regional Trigger	4,388	50	6581
3.1.2.1	Prototypes	441	46	643
3.1.2.2	Preproduction ASICs	553	47	811
3.1.2.3	Test Facilities	78	50	117
3.1.2.4	Power Supplies	82	30	106
3.1.2.5	Crates	35	30	45
3.1.2.6	Backplane	194	54	299
3.1.2.7	Clock & Control Card	132	40	185
3.1.2.8	Receiver Card	1,670	54	2571
3.1.2.9	Electron ID Card	744	50	1116
3.1.2.10	Jet Summary Card	170	50	254
3.1.2.11	Cables	7	30	9
3.1.2.12	DAQ Processor			
3.1.2.13	Crate Monitor Card			
3.1.2.14	Trigger Tests	282	50	423
3.1.2.15	Project Management			



Changes since last May 1997 Review:

- Contingency analysis performed at lowest level (increased from 39->50%)
- Bottoms-up recosting & new WBS (no substantial *net* cost change)
- Cost profile pushed back 6 months on average

WBS Number	Description	EDIA (k$)	M&S (k$)	Base (k$)	Cont (%)	Total (k$)
3.1.2	Calorimeter Regional Trigger	1,247	3,141	4,388	50	6,581
3.1.2.1	Prototypes	301	140	441	46	643
3.1.2.1.1	Proto. Receiver Card	89	18	106	32	140
3.1.2.1.2	Proto. Electron ID Card	65	7	72	50	108
3.1.2.1.3	Proto. Phase ASIC		50	50	50	75
3.1.2.1.4	Proto. BScan ASIC	14	50	64	50	96
3.1.2.1.5	Proto. Jet Summary Card	99	9	108	50	162
3.1.2.1.6	Proto. Clock & Control Card	35	6	41	50	62
3.1.2.1.7	Proto. Crate Monitor Card					
3.1.2.2	Preproduction ASICs	243	310	553	47	811
3.1.2.2.1	Electron ID ASIC	53	80	133	50	199
3.1.2.2.2	Adder ASIC	42	50	92	30	120
3.1.2.2.3	Sort ASIC	42	80	122	50	183
3.1.2.2.4	Phase ASIC	53	50	103	50	154
3.1.2.2.5	Boundary Scan ASIC	53	50	103	50	154
3.1.2.3	Test Facilities	18	60	78	50	117
3.1.2.3.1	Design Test Facil.	13		13	50	19
3.1.2.3.2	Procure Test Facil.		60	60	50	90
3.1.2.3.3	Assemble Test Facil.	5		5	50	8
3.1.2.4	Power Supplies	3	79	82	30	106
3.1.2.4.1	Select Power Supplies	3		3	30	3
3.1.2.4.2	Power Supply Procure		79	79	30	103
3.1.2.5	Crates	21	13	35	30	45
3.1.2.5.1	Design Crate	18		18	30	23
3.1.2.5.2	Procure Crates		13	13	30	17
3.1.2.5.3	Test Crates	4		4	30	5
3.1.2.6	Backplane	64	130	194	54	299
3.1.2.6.1	Design Backplane	57		57	54	88
3.1.2.6.2	Backplane Procure	1	130	131	54	202
3.1.2.6.3	Test Bkpl	5		5	54	8

WBS Number	Description	EDIA (k$)	M&S (k$)	Base (k$)	Cont (%)	Total (k$)
3.1.2.7	Clock & Control Card	67	65	132	40	185
3.1.2.7.1	Design CCC	57		57	40	80
3.1.2.7.2	CCC Procure	2	65	67	40	94
3.1.2.7.3	Test CCC	8		8	40	11
3.1.2.8	Receiver Card	109	1,561	1,670	54	2,571
3.1.2.8.1	Design RC	63		63	54	98
3.1.2.8.2	RC Procure	4	1,561	1,565	54	2,410
3.1.2.8.3	Test RC	41		41	54	64
3.1.2.9	Electron Identification Card	95	649	744	50	1,116
3.1.2.9.1	Design EIC	57		57	50	86
3.1.2.9.2	EIC Procure	2	649	652	50	978
3.1.2.9.3	Test EIC	35		35	50	53
3.1.2.10	Jet Summary Card	67	103	170	50	254
3.1.2.10.1	Design JSC	57		57	50	86
3.1.2.10.2	JSC Procure	2	103	105	50	157
3.1.2.10.3	Test JSC	8		8	50	12
3.1.2.11	Cables		7	7	30	9
3.1.2.13	Crate Monitor Card					
3.1.2.14	Trigger Tests	260	22	282	50	423
3.1.2.14.1	Trigger Subsystem Tests	106		106	50	158
3.1.2.14.2	Trigger System Installation	155	22	177	50	265
3.1.2.15	Trigger Project Management					
3.1.2.15.1	Tracking & Reporting					

Cal Trig basis of estimate: Zeus

Zeus first level trigger requirements:

- Beam crossing every 96 nsec
- Background rate <100 kHz
- Max Level 1 Rate < 0.5 kHz

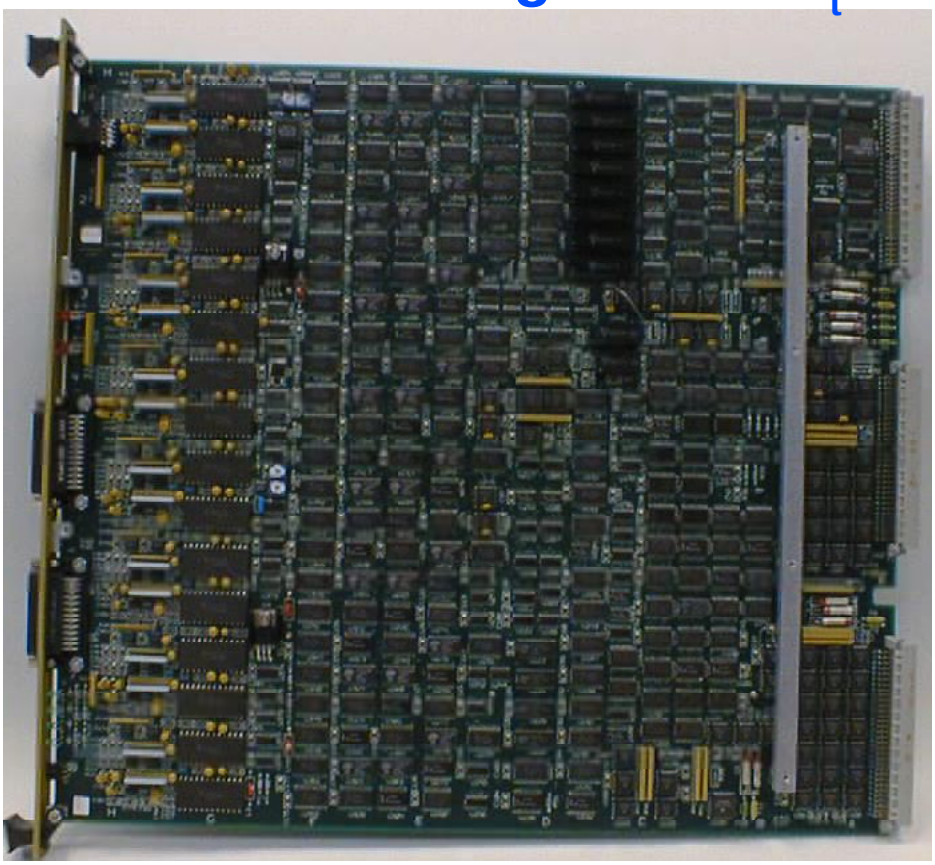
Zeus calorimeter trigger processing:

- Trigger decision total time = 5 μsec
- Data from13K Phototubes
- Dynamic range of 4096:1
  - EMC: μ: 300 MeV to 400 GeV

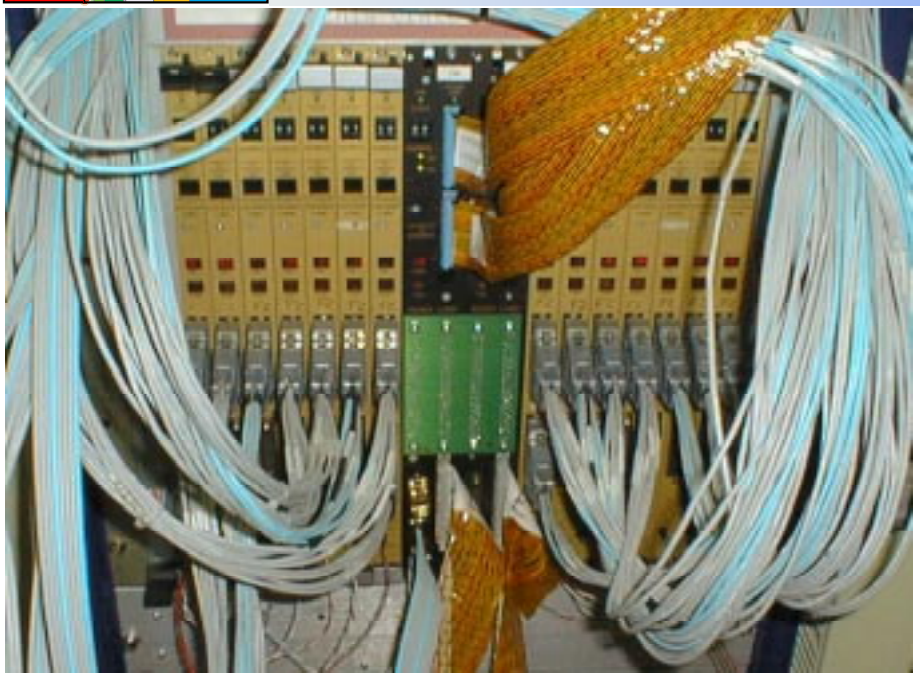
Zeus calorimeter trigger functions

- Identify e, μ., jets & sum missing & total E_t

270 9Ux400 mm Encoder Cards digitize w/12-bit range every 12 ns , test for E v. H, MIP, Quiet & sum energies. Output at 80 MHz to Adders.

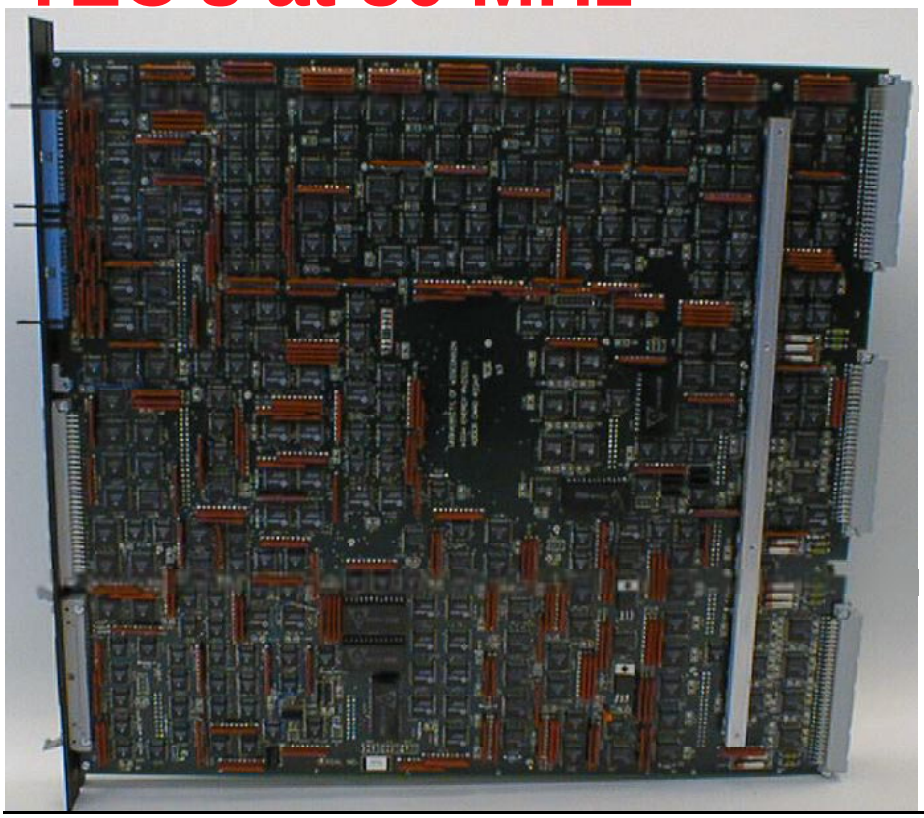


Zeus Calorimeter Trigger



16 crates send results to Global Cal Trigger

2 double-board Adder Cards/crate receive & process data from 14 TEC's at 80 MHz



Adder Cards find Isolated e's & μ's, and sum energies

Information from Zeus

Board Costs:

- **Zeus Trigger Encoder Card Features**
  - 9U x 400mm
  - 270 Made
  - 80 MHz Clock
  - Includes Analog front end digitization at 13 bits/10 MHz
  - 4 HAC & 4 EMC inputs/card = 8 total
- **Zeus Trigger Encoder Card Costs (in 1991-1992)**
  - Board: $300
  - Assembly: $350
  - Parts: $2,000
  - Engineering: 2 MY (incl. analog)
  - Costs verified in 1995 manufacture of 30 spares

Calorimeter Trigger M&S

M&S for Crates, Boards & Cables:

WBS	Item	Unit Cost	Number	Total
3.1.2.4	Power Supplies	3,600	22	79,200
3.1.2.5	Crates	600	22	13,200
3.1.2.6	Backplane	5,910	22	130,020
3.1.2.7	Clock & Control Card	2,960	22	65,120
3.1.2.8	Receiver Card	8,870	176	1,561,120
3.1.2.9	Electron ID Card	3,690	176	649,440
3.1.2.10	Jet Summary Card	4,670	22	102,740
3.1.2.11	Cables	$1/ft	7,300	7,300

Detail for Boards:

Card	Size	Board	Assmbl.	Parts	Total
Backplane	crate	1,000	300	4,610	5,910
Clock & Control	9Ux280mm	600	400	1,960	2,960
Receiver	9Ux400mm	800	650	7,420	8,870
Electron ID	9Ux280mm	400	300	2,990	3,960
Jet Summary	9Ux280mm	600	500	3,570	4,670

Detail for ASICS (WBS 3.1.2.2):

ASIC	NRE	Cst/Prt	#/RC	#/EIC	#/JSC	Tot.#
Adder (GaAs)	50,000	179	3	0	2	520
Phase (GaAs)	50,000	360	8	0	0	1,280
Sort (GaAs)	80,000	300	0	1	2	200
Electron ID(GaAs)	80,000	300	0	2	0	320
Bndry. Scan(GaAs)	50,000	150	1	1	1	340

(costs per part are included in board parts costs above)

Cal. Trigger Contingency

Factors

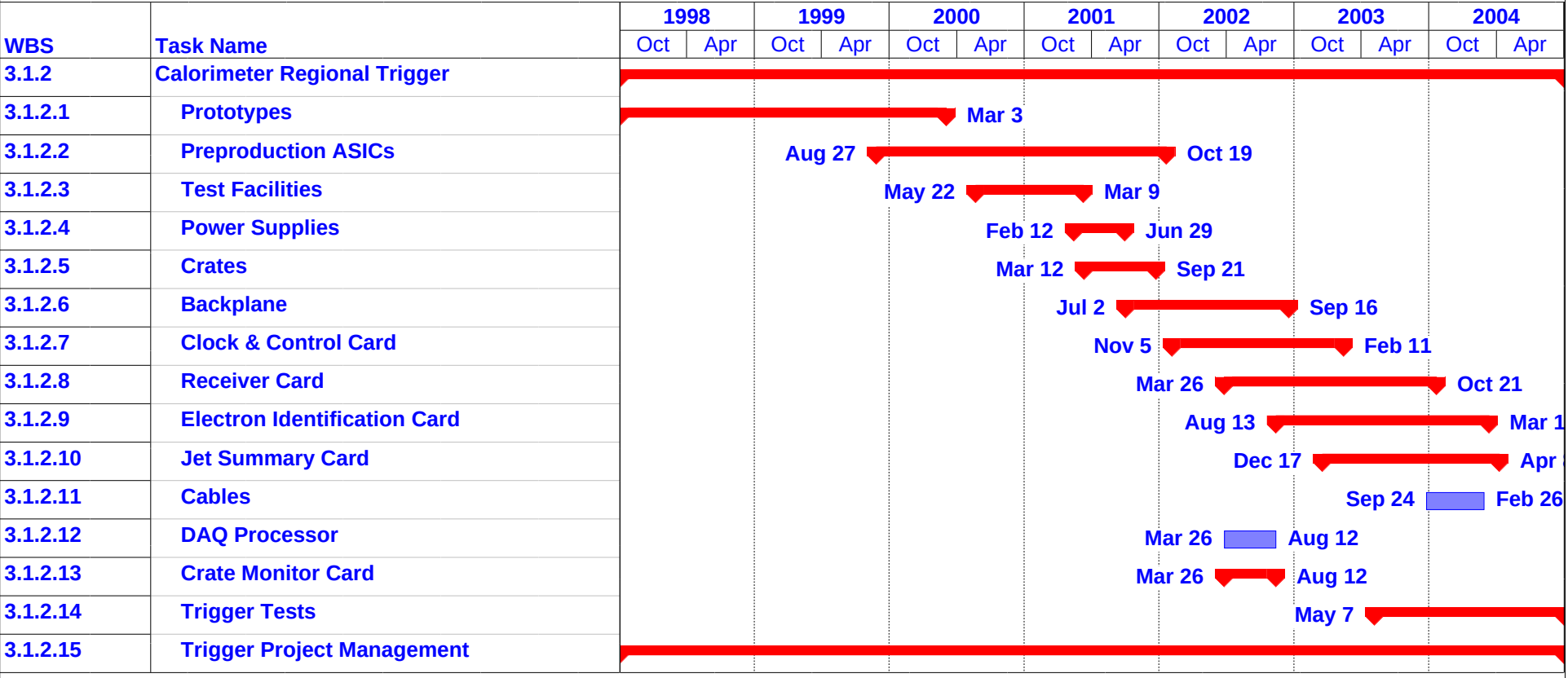
- **In-house experience**
  - Zeus Trigger System
- **Existing technology**
  - CMS Prototype Boards, Backplane & ASIC's

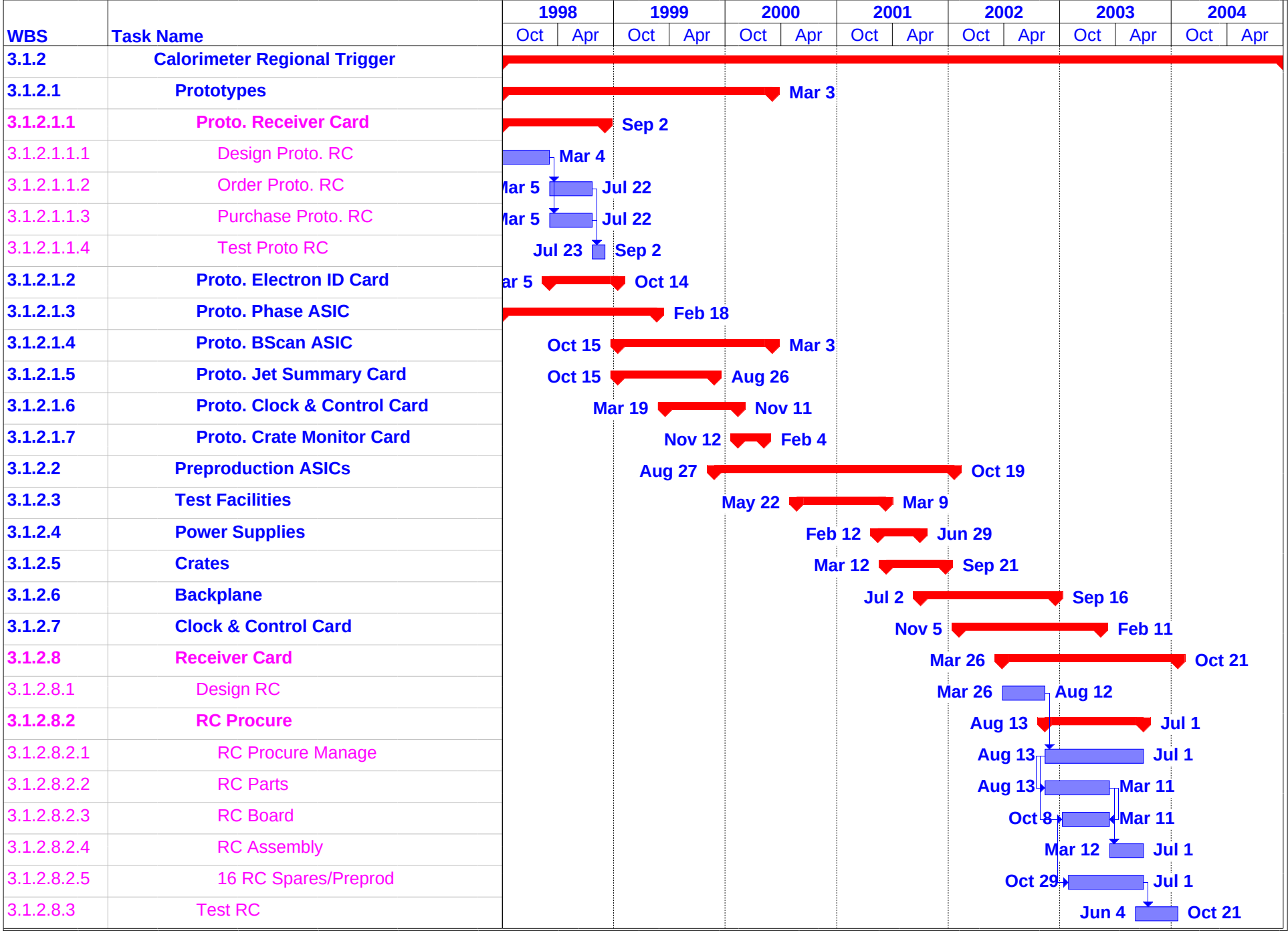
Calculation (item by item):

- **Use Zeus Cal Trigger**
- **Judgement of Difficulty (multiplication factor)**
  - Difficult: ≥ 1.1
  - Average: 1.0
- **Design Maturity (multiplication factor)**
  - Conceptual Design = 1.5
  - RFI with engineering sketches = 1.4
  - Engineering Design = 1.3
  - Quote or bid package = 1.2
  - Catalog = 1.1

Conclusion:

- **Overall = 50%**


WBS
Task Name
1998
1999
2000
2001
2002
2003
2004
Oct
Apr
3.1.2
Calorimeter Regional Trigger
3.1.2.1
Prototypes
Mar 3
3.1.2.2
Preproduction ASICs
Aug 27
Oct 19
3.1.2.3
Test Facilities
May 22
Mar 9
3.1.2.4
Power Supplies
Feb 12
Jun 29
3.1.2.5
Crates
Mar 12
Sep 21
3.1.2.6
Backplane
Jul 2
Sep 16
3.1.2.7
Clock & Control Card
Nov 5
Feb 11
3.1.2.8
Receiver Card
Mar 26
Oct 21
3.1.2.9
Electron Identification Card
Aug 13
Mar 1
3.1.2.10
Jet Summary Card
Dec 17
Apr
3.1.2.11
Cables
Sep 24
Feb 26
3.1.2.12
DAQ Processor
Mar 26
Aug 12
3.1.2.13
Crate Monitor Card
Mar 26
Aug 12
3.1.2.14
Trigger Tests
May 7
3.1.2.15
Trigger Project Management


WBS
Task Name
1998
1999
2000
2001
2002
2003
2004
Oct
Apr
3.1.2 Calorimeter Regional Trigger
3.1.2.1 Prototypes
Mar 3
3.1.2.1.1 Proto. Receiver Card
Sep 2
3.1.2.1.1.1 Design Proto. RC
Mar 4
3.1.2.1.1.2 Order Proto. RC
Mar 5
Jul 22
3.1.2.1.1.3 Purchase Proto. RC
Mar 5
Jul 22
3.1.2.1.1.4 Test Proto RC
Jul 23
Sep 2
3.1.2.1.2 Proto. Electron ID Card
Mar 5
Oct 14
3.1.2.1.3 Proto. Phase ASIC
Feb 18
3.1.2.1.4 Proto. BScan ASIC
Oct 15
Mar 3
3.1.2.1.5 Proto. Jet Summary Card
Oct 15
Aug 26
3.1.2.1.6 Proto. Clock & Control Card
Mar 19
Nov 11
3.1.2.1.7 Proto. Crate Monitor Card
Nov 12
Feb 4
3.1.2.2 Preproduction ASICs
Aug 27
Oct 19
3.1.2.3 Test Facilities
May 22
Mar 9
3.1.2.4 Power Supplies
Feb 12
Jun 29
3.1.2.5 Crates
Mar 12
Sep 21
3.1.2.6 Backplane
Jul 2
Sep 16
3.1.2.7 Clock & Control Card
Nov 5
Feb 11
3.1.2.8 Receiver Card
Mar 26
Oct 21
3.1.2.8.1 Design RC
Mar 26
Aug 12
3.1.2.8.2 RC Procure
Aug 13
Jul 1
3.1.2.8.2.1 RC Procure Manage
Aug 13
Jul 1
3.1.2.8.2.2 RC Parts
Aug 13
Mar 11
3.1.2.8.2.3 RC Board
Oct 8
Mar 11
3.1.2.8.2.4 RC Assembly
Mar 12
Jul 1
3.1.2.8.2.5 16 RC Spares/Preprod
Oct 29
Jul 1
3.1.2.8.3 Test RC
Jun 4
Oct 21

Cal. Trig. Milestones

Prototype Design Finished	May '99
Proto. test w/ECAL Proto. Elect.	Jun '99
Proto. Boards & Tests Finished	Nov '99
Begin ASIC Preproduction	May '00
Proto. test w/HCAL Proto. Elect.	Jun '00
Begin Backplane & Crate Production	May '01
ASIC Development Complete	Jun '01
Finish ASIC Preproduction	Oct '01
Begin Trigger Board Production	Mar '02
Begin Tests w/Final ECAL Elect.	Jul '02
Begin ASIC Production	Aug '02
Begin Tests w/Final HCAL Elect.	Sep '02
Crate & Backplane Complete	Sep '02
Begin Production Board Tests	Jan '03
Designs Finished	May '03
Finish ASIC Production	Nov '03
Finish Trigger Board Production	Feb '04
Finish Production Board Tests	Apr '04
Begin Trigger Installation	Apr '04
Begin Final System tests w/E,HCAL	May '04
Trigger Installation Finished	Sep '04

Conclusions

CMS Regional Calorimeter Trigger

- **Inputs on 1.2 Gbaud Cu serial links**
  - 8-bits energy & 1 bit fine grain/trigger tower
  - Careful mapping of calorimeter towers into trigger logic
- **Receiver Card scales, sums, preprocesses**
  - Prototype being manufactured
  - Designed to receive data from serial links
  - Designed to operate @ 160 MHz
  - 13 x 8 bit Adder ASIC tested > 160 MHz
- **Backplane for VME & trigger data**
  - Prototype constructed/tested
  - Prototype Clock Card constructed/tested
  - Signal performance excellent @ 160 MHz
  - Confirmation of design feasibility
- **Electron Isolation & Jet Summary Cards**
  - Receive data from Backplane
  - Algorithms matched to data & physics
- **Documented Cost, Schedule, Milestones**