Trigger Overview

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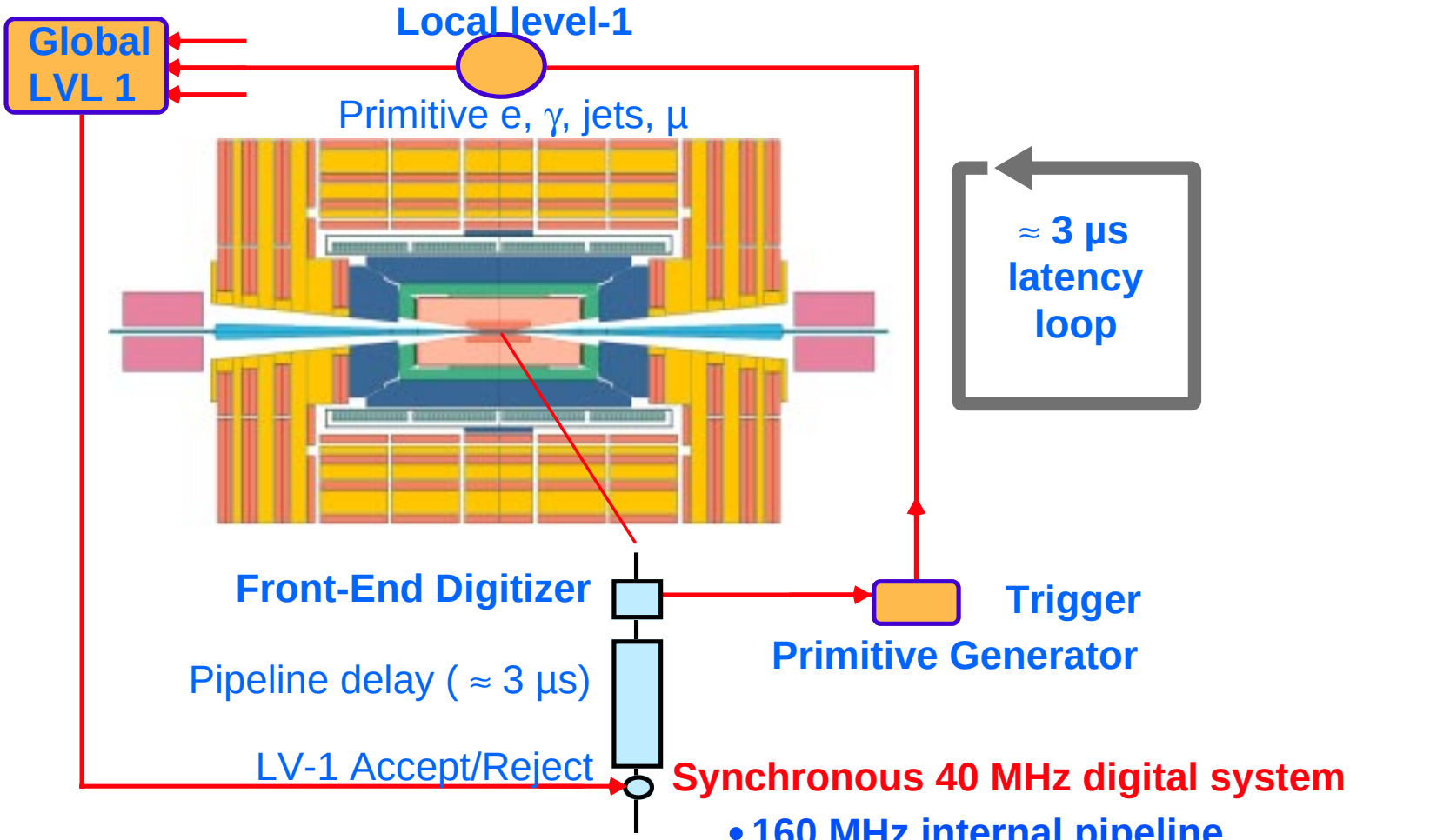
CMS Trigger Project Manager

DOE/NSF Review
February 18, 1999

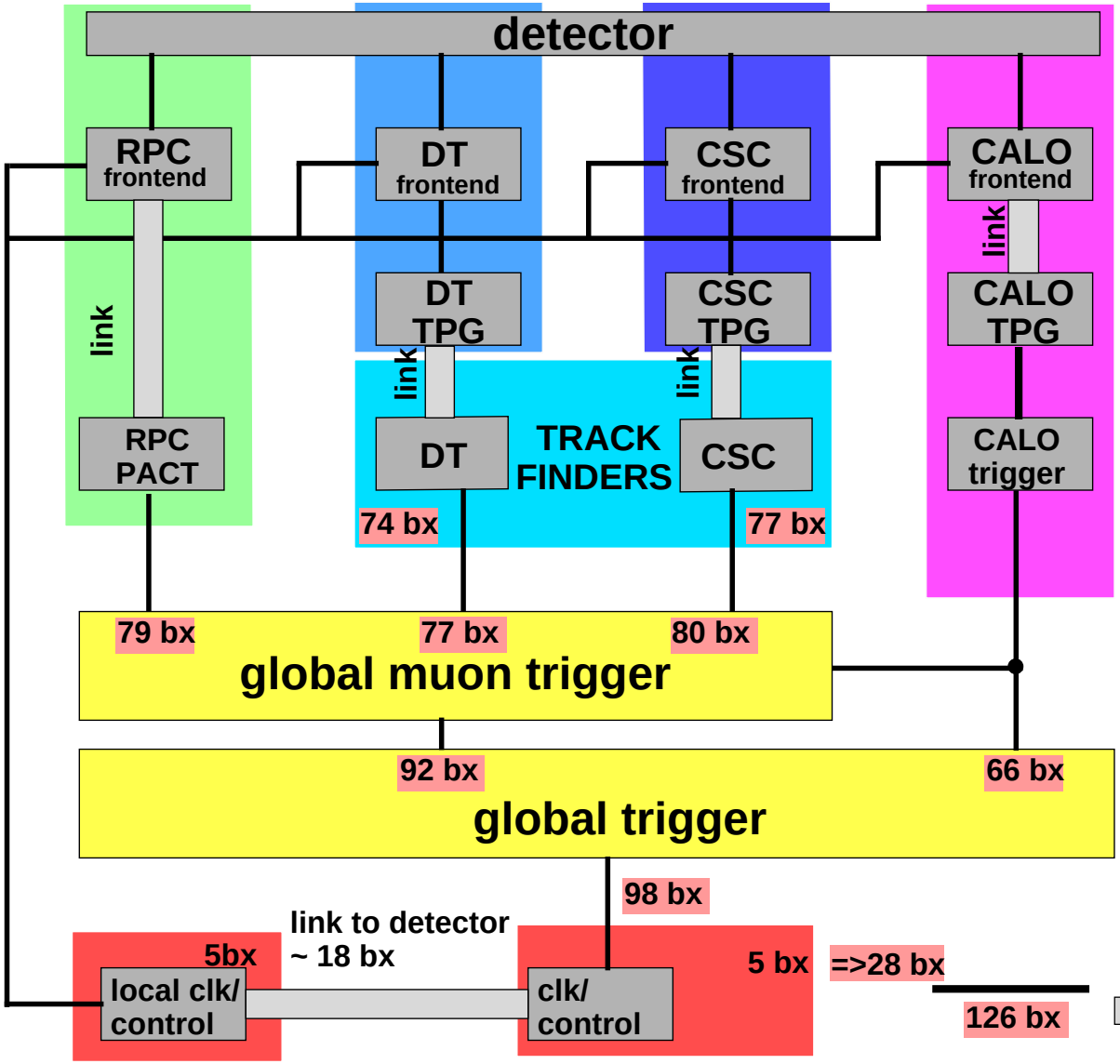
CMS Level 1 Pipeline



Synchronous 40 MHz digital system

- **160 MHz internal pipeline**
- **Readout & processing latency < 1μs**
- **Signal distribution latency ≈ 2 μs**

CMS Level 1 Latency



Target is 128 bunch crossings

- 3 μsec

Reviewed in detail once/year

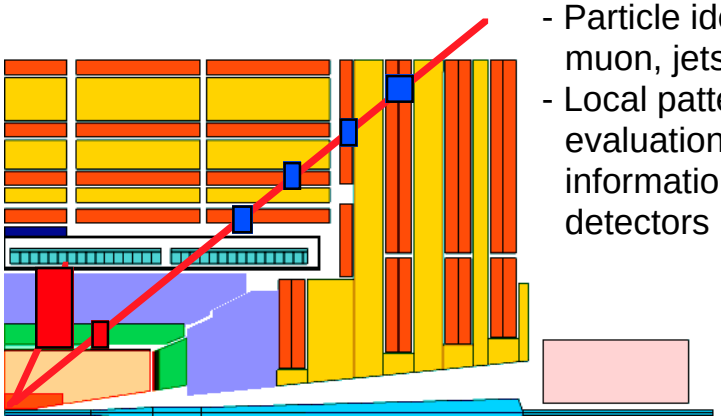
- Last Review in November

Number shown are latency budgets

- Units are bunch crossings
- Include contingency

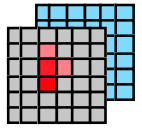
CMS Level 1 Trigger

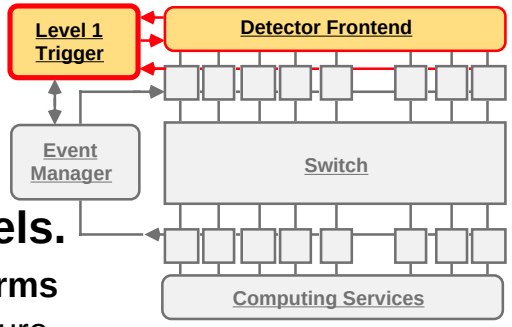
40 MHz



Level-1. Specialized processors

- Particle identification: high p_T electron, muon, jets, missing E_T
- Local pattern recognition and energy evaluation on prompt macro-granular information from calorimeter and muon detectors



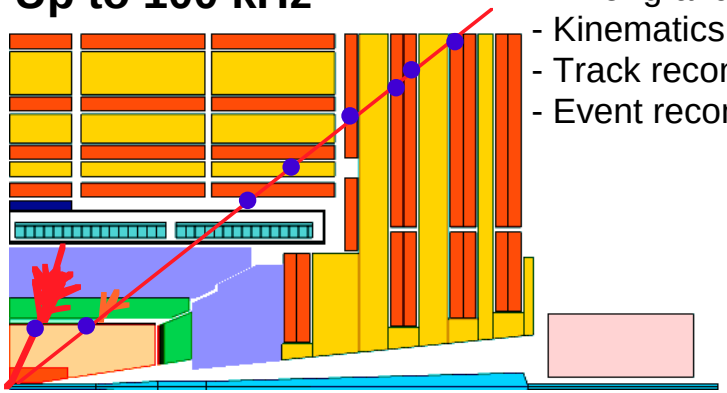


High trigger levels.

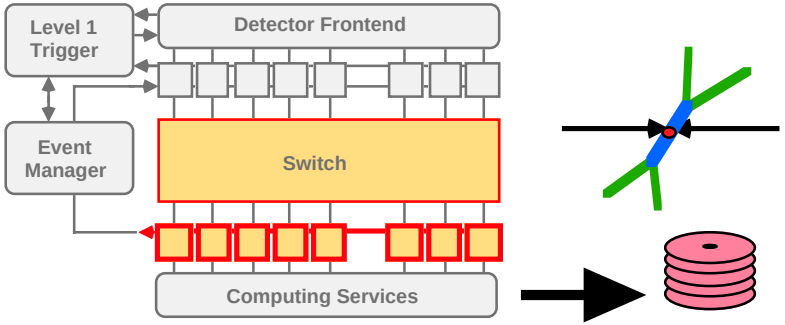
Network and CPU farms

- Clean particle signature
- Finer granularity precise measurement
- Kinematics. effective mass cuts & event topology
- Track reconstruction and detector matching
- Event reconstruction and analysis

Up to 100 kHz



≈ 100 Hz



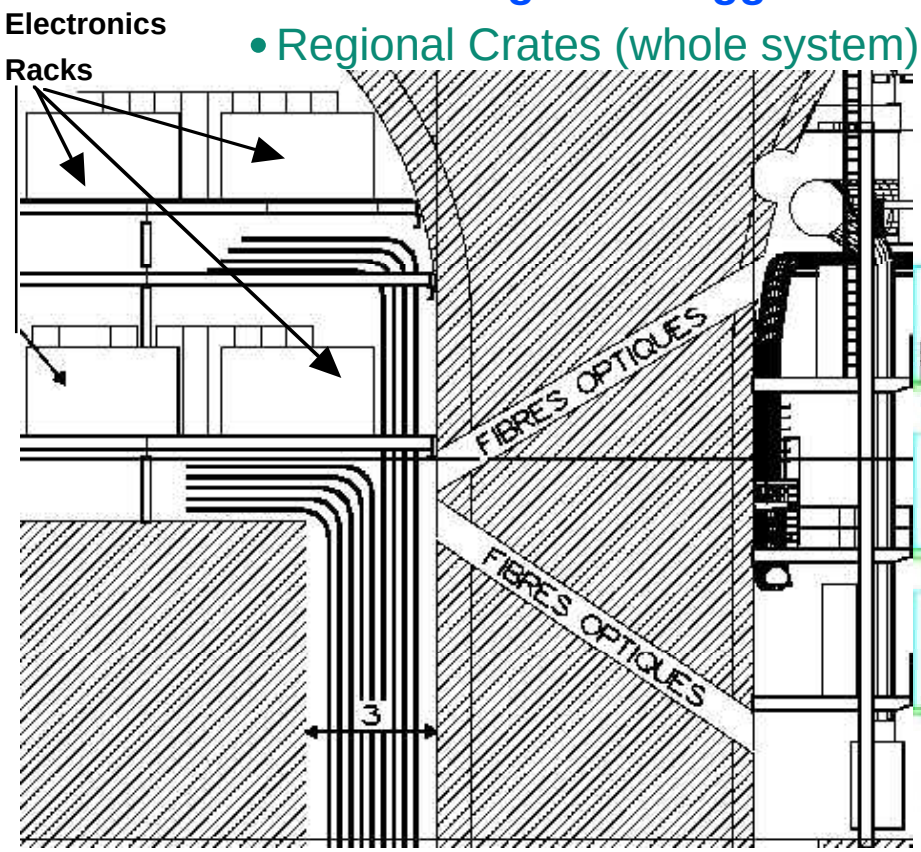
Trigger Electronics Locations

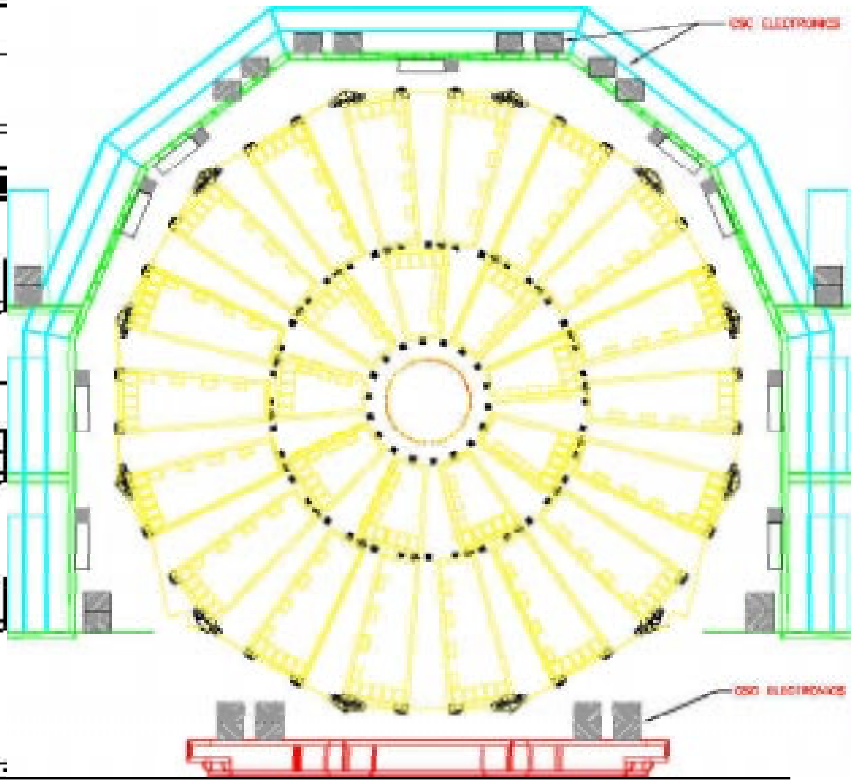
In Underground Shielded Room:

- **CSC Muon Trigger Track Finder**
  - Sector Receiver & Processor
  - Clock & Control Boards
- **Calorimeter Regional Trigger**
  - Regional Crates (whole system)

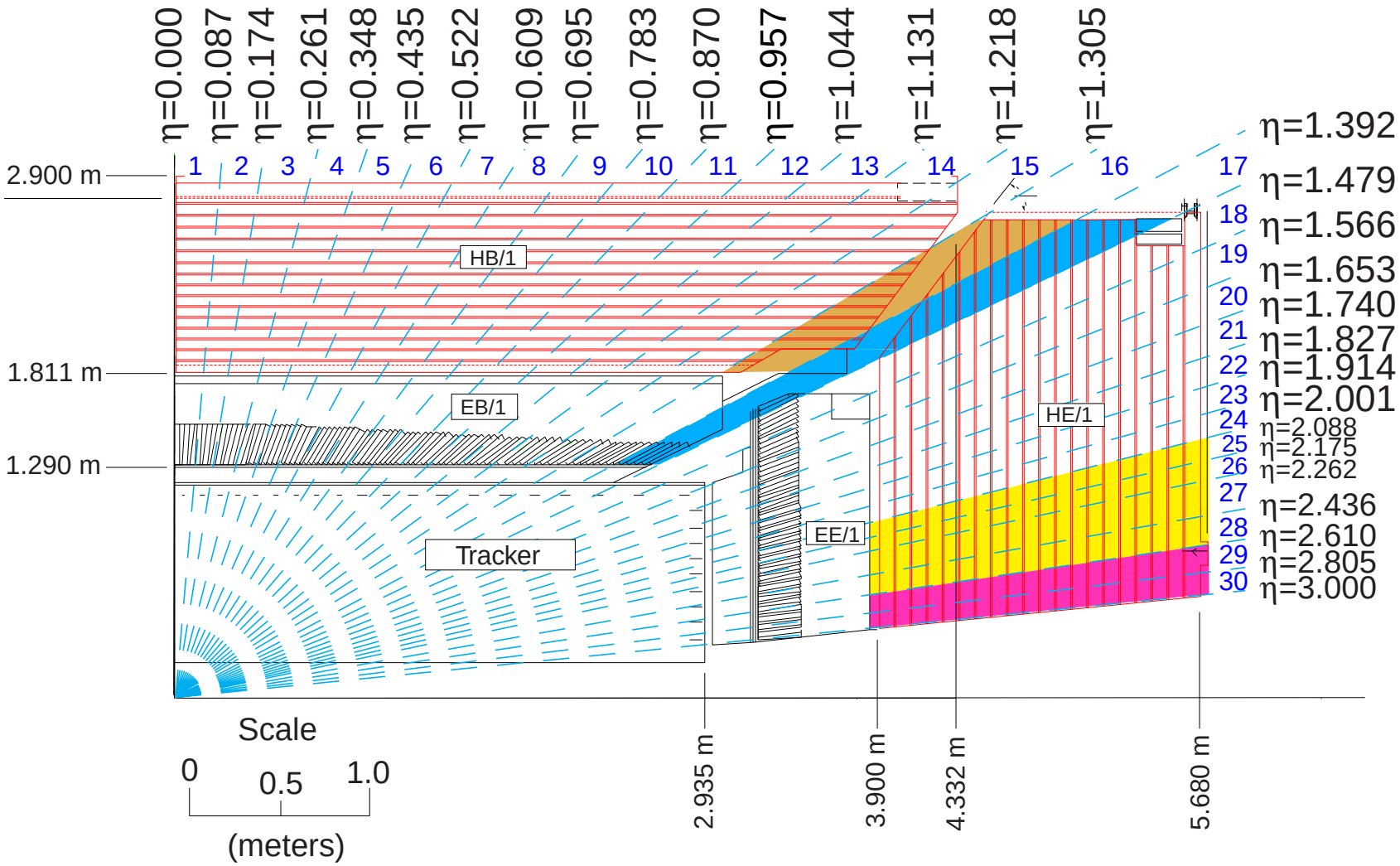
In Peripheral Crates on Iron Disks:

- **CSC Muon Trigger**
  - Muon Port Cards
  - Clock & Control Boards

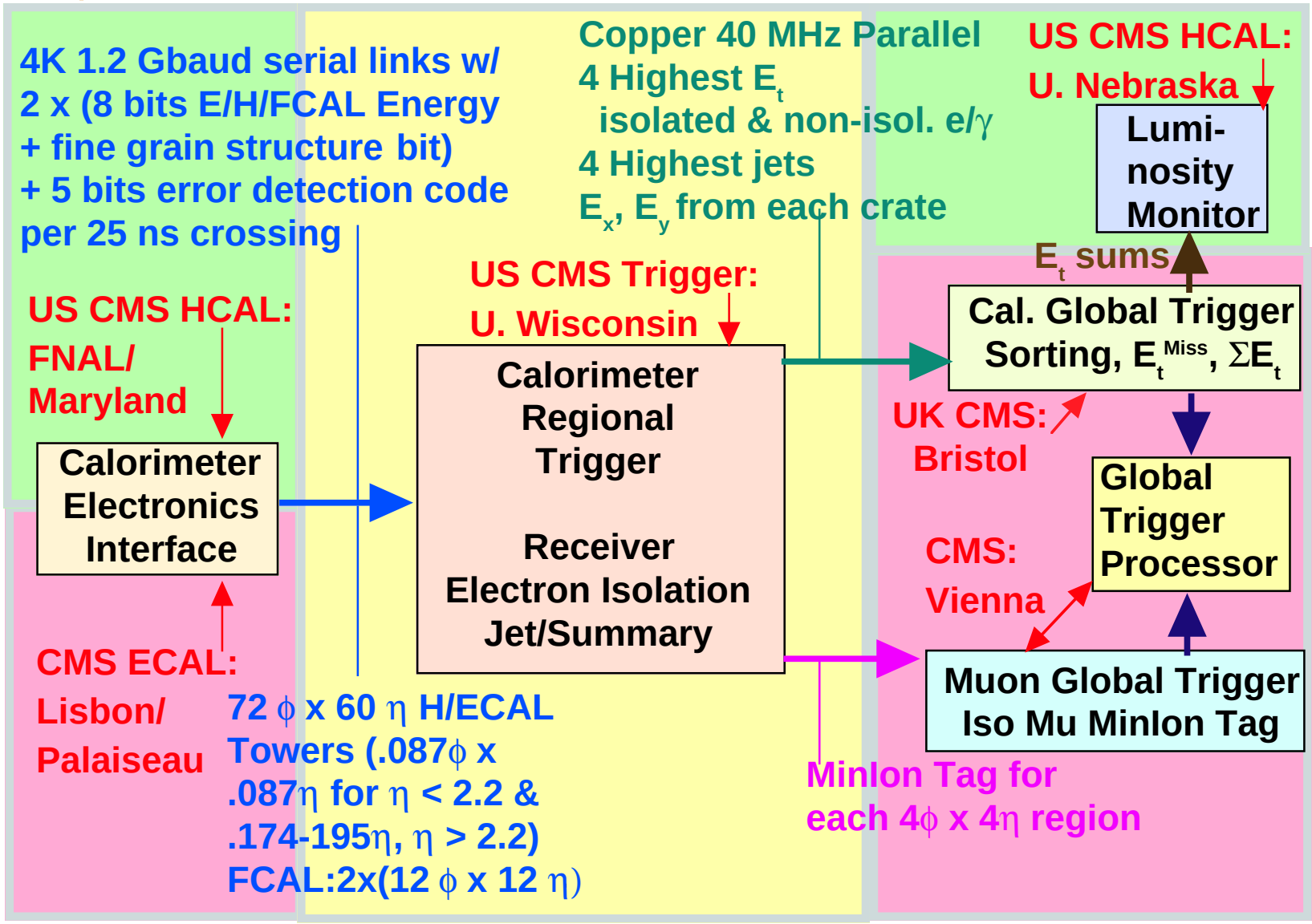




Calorimeter Trigger Geometry

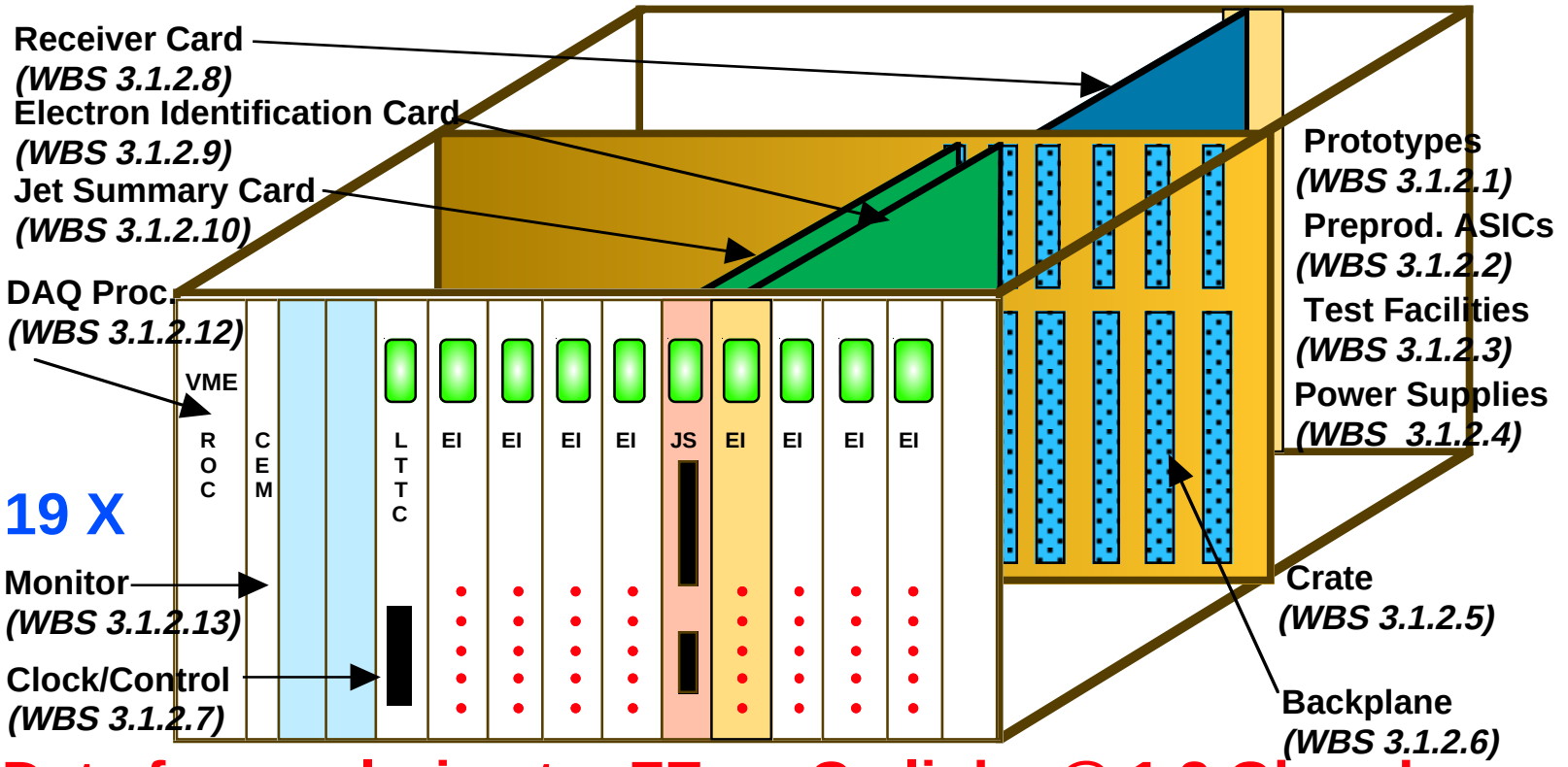


Calorimeter Trigger Overview



Regional Calorimeter Crate

(WBS 3.1.2)



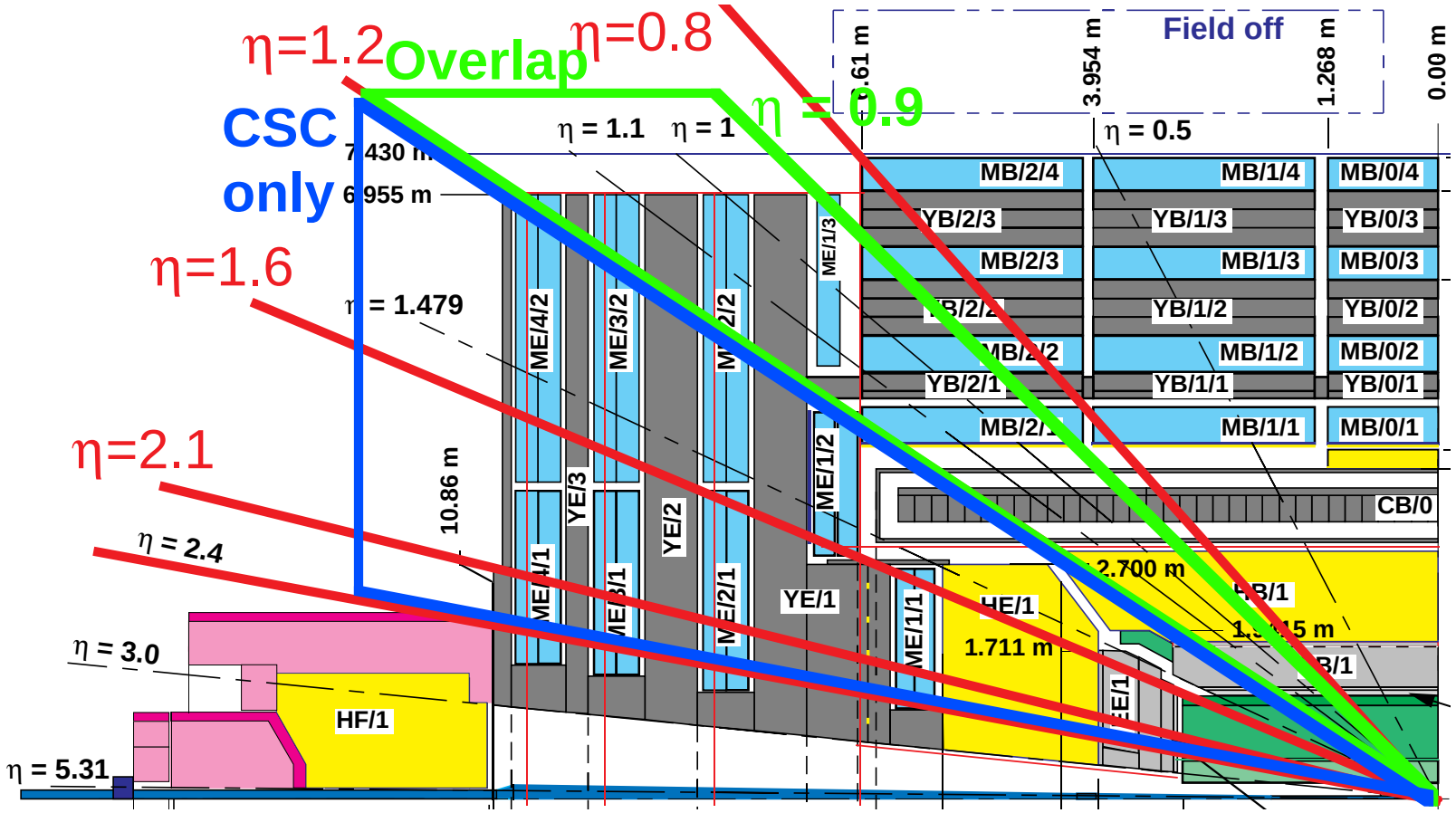
Data from calorimeter FE on Cu links @ 1.2 Gbaud

- Into 152 rear-mounted Receiver Cards **(ptyp. built)**

160 MHz point to point backplane **(ptyp. built)**

- 19 Clock&Control **(ptyp. built)**, 152 Electron ID **(ptyp. built)**
  19 Jet/Summary, Receiver Cards operate @ 160 MHz

CSC Muon Trigger Geometry

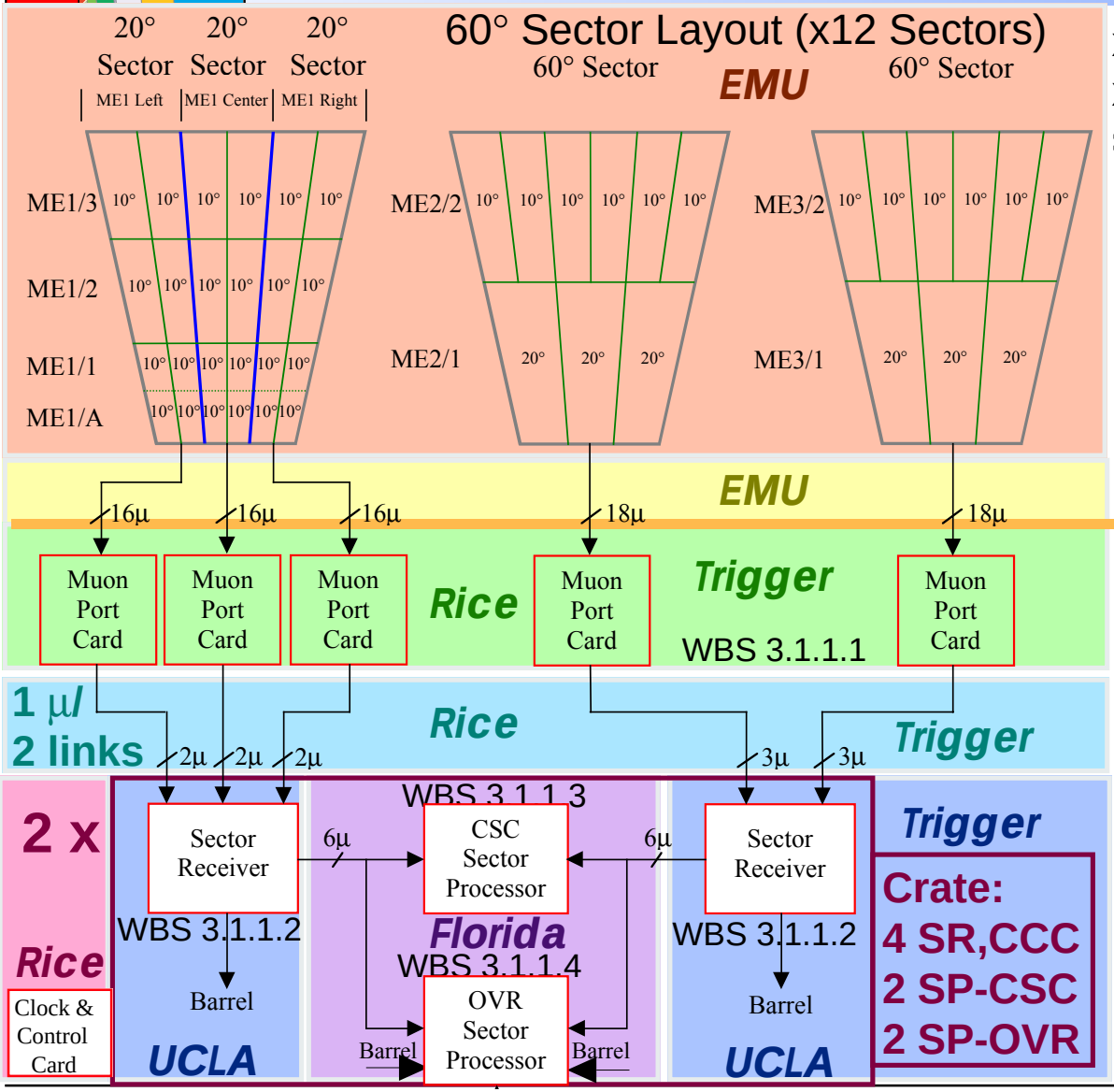


CSC Track-finding:

- **Two Types of 60° Sector Processors:**
  - **12 SP-Overlap: 0.9 > |η| > 1.2** :CSC's & Barrel DT's
  - **12 SP-CSC: 1.2 > |η| > 2.4** :CSC's only

CSC Trigger Layout

(WBS 3.1.1)



x 6 = 360°
x 2 Ends
= x 12

Trigger Mother Boards in 8 Iron Disk Peripheral Crates

Backplane, Crate Interconnects *EMU* / *Trigger*

5 Muon Port Cards x 12

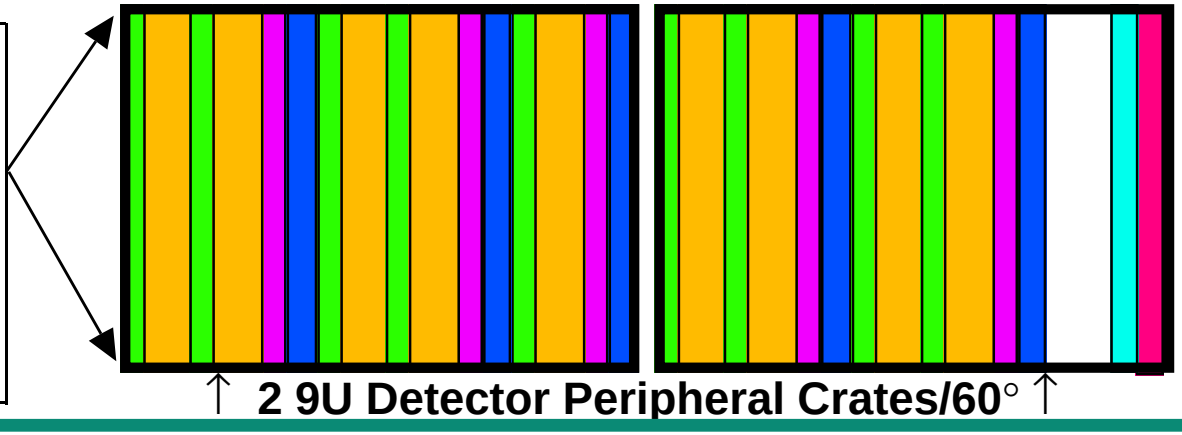
24 Optical Links x 12

6 Track Finder Crates in Counting Room (total). Sort output *(Rice)* to Global Muon Trigger *(Vienna)*

Endcap Muon Crates

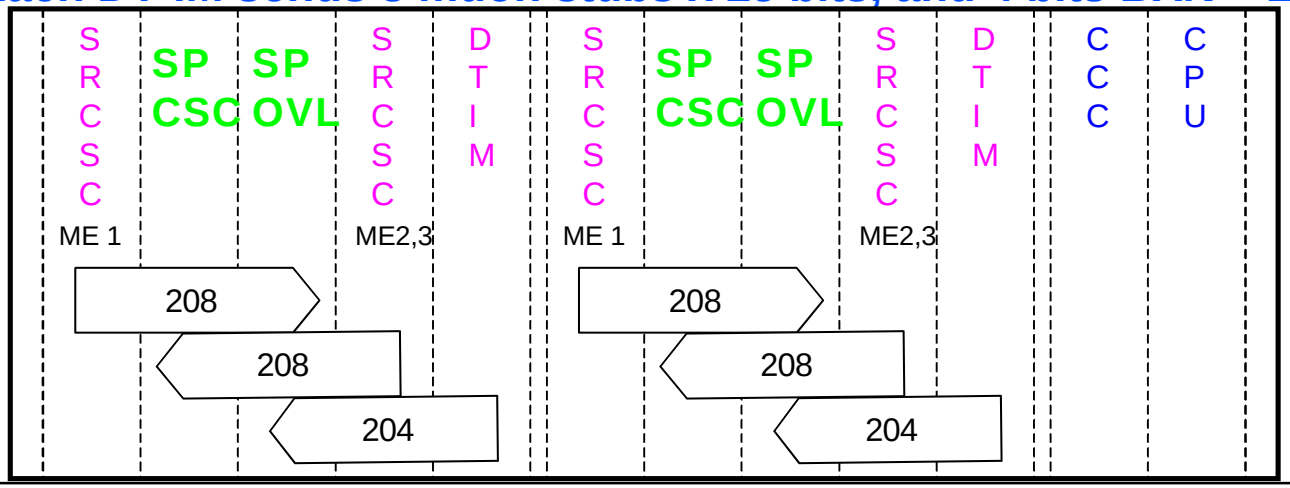
(Detector & Counting Room)

Type	Board	Slots
CLCT	9	9
ALCT	9	18
MBT	5	5
MBD	5	5
MPC	1	1
CCC	1	1
Total	30	39

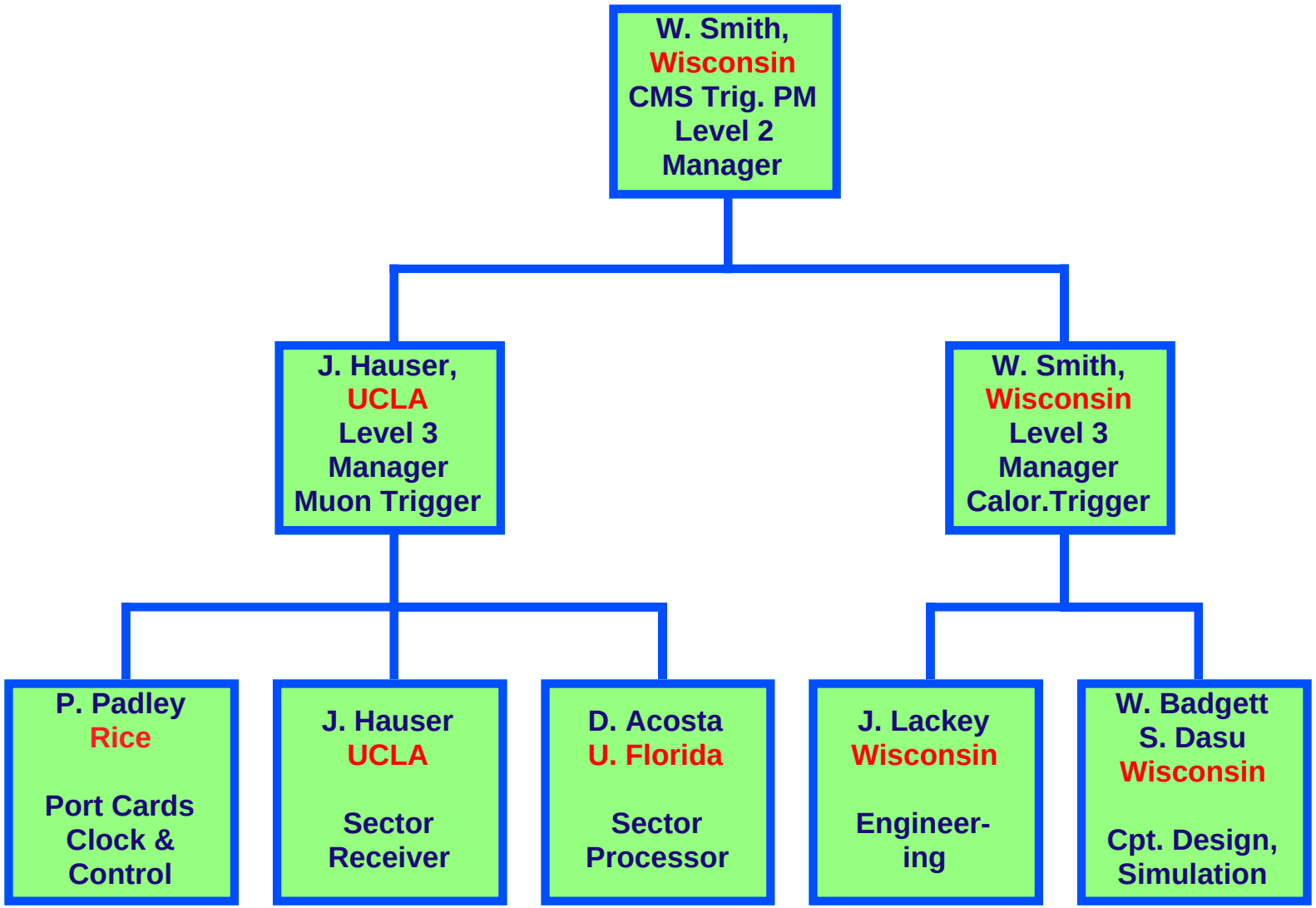


6 Counting Room 9U VME Track Finder Crates with custom backplanes:

- Each SR-CSC sends 6 muon stubs x 34 bits, and 4 bits BXN = 208 bits
- Each SP sends to the CSC sorter 3 best muons x 22 bits = 66 bits
- Each DT-IM sends 8 muon stubs x 25 bits, and 4 bits BXN = 204 bits



U. S. Trigger Organization



Trigger Program

Simulation

- Check final geometry influence on trigger performance
- Validate final algorithms as implemented in hardware

Calorimeter Trigger

- Validate 160 MHz dataflow & processing
- Design & test prototype Boards
- Design & test prototype ASICs
- Design & test high speed Cu serial Link system

Muon Trigger

- Design & test prototype Boards
- Design & test prototype FPGA circuits
- Design & test high speed optical serial link system
- Test interface with CSC FE electronics

Talks - Trigger

February 18, 1999

Introduction	W. Smith	11:00 - 11:20
Trigger Simulation Update	S. Dasu	11:20 - 11:40
Cal. Reg.Trig.Status & Plan	W. Badgett	11:40 - 12:10
Muon Trigger Overview	J. Hauser	12:10 - 12:30
LUNCH		12:30 - 1:30
Mu Trig. Elect. in Cavern	P. Padley	1:30 - 1:50
Mu Tr. Elect. in Count. Rm	D. Acosta	1:50 - 2:10
Cost and Schedule: Status	W. Smith	2:10 - 2:30
DISCUSSION		2:30 - 3:00