



# CMS

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Compact Muon Solenoid

## Calorimeter & Muon Trigger:

- **Highlights**
- **Milestones**
- **Concerns**
- **Near-term Activities**



# Calorimeter Trigger

## Highlights, Milestones, Activities:

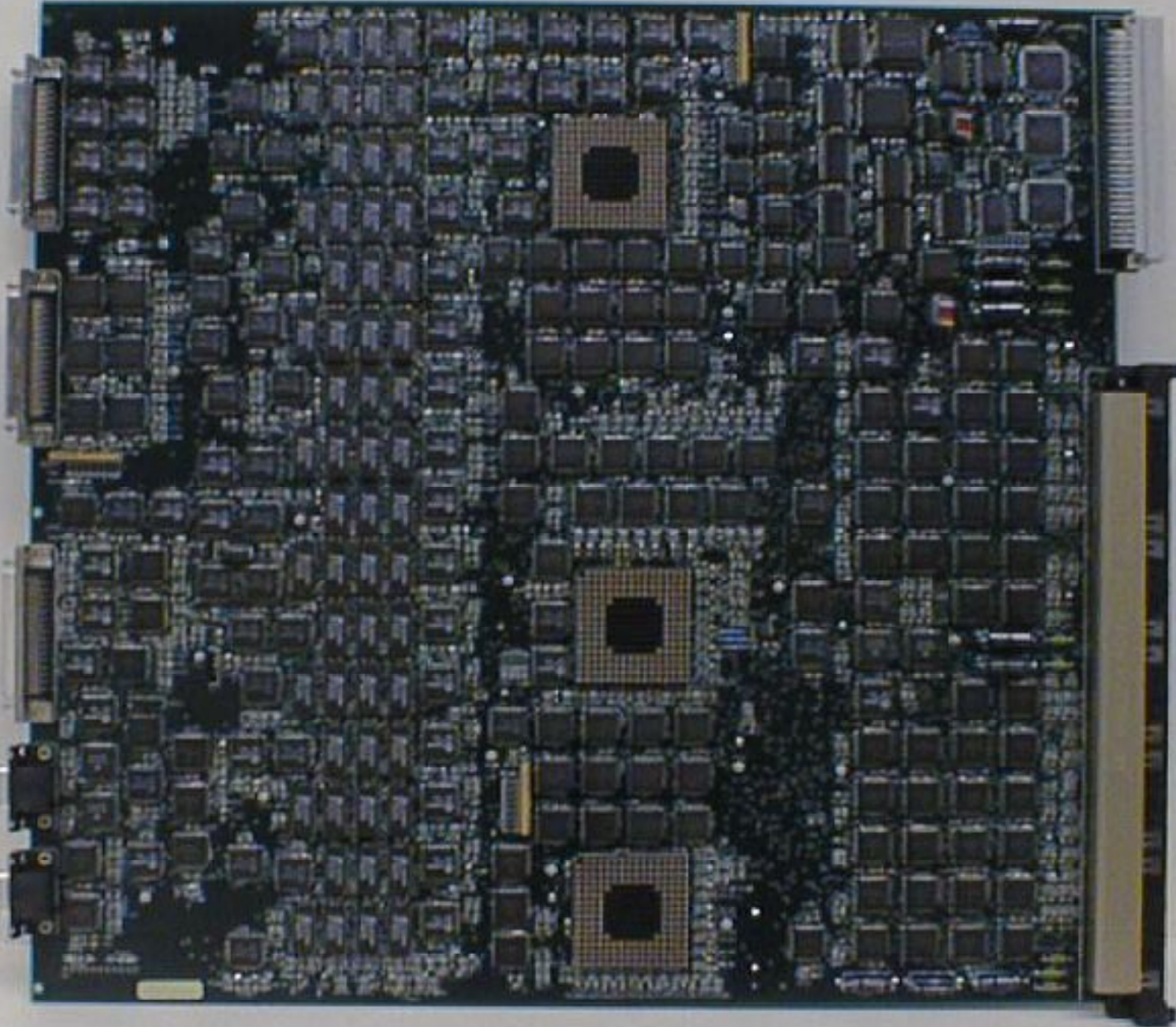
- **Receiver Card Prototype delivered** - milestone
  - Testing starts next week - main activity
- **Electron ID ASIC Package Study Completed**
  - Layout (floor plan) & timing studies
  - 2 different Vitesse packages
- **Electron ID Card Prototype Design & Layout close to completion**
  - Will construct after test of common design circuits used on Receiver Card

## Near-term plans:

- **Full Dataflow tests**
  - Receiver Card Prototype
  - Backplane Prototype
  - Electron Identification Card Prototype
- **Electron Isolation ASIC**
  - Design in Vitesse GaAs
  - Produce Prototype
- **Prototype Phase ASIC**
  - Design started



# Receiver Card Prototype



**Prototype under test**



# Muon Trigger

## Highlights, Milestones, Activities:

- **Summer Beam Test:** successful operation of
  - Trigger Mother Board Prototype
  - Cathode & Anode LCT Prototypes
- **Initial Designs & Documentation: - milestones**
  - Muon Port Card
    - <http://bonner-ntserver.rice.edu/cmsscstrigger>
  - Sector Receiver Card
    - <http://bonner-ntserver.rice.edu/motherboard/Archive/src.htm>
  - Sector Processor Cards
    - <http://www.phys.ufl.edu/~acosta/cms/trigger.html>
- **Design & Status Review at Rice**
  - Sep 27,28
  - Good Progress on all fronts
  - Revision to Muon Port Cards: RPC Input
  - Movement of Electronics to Periphery
  - Revision to Track-Finder

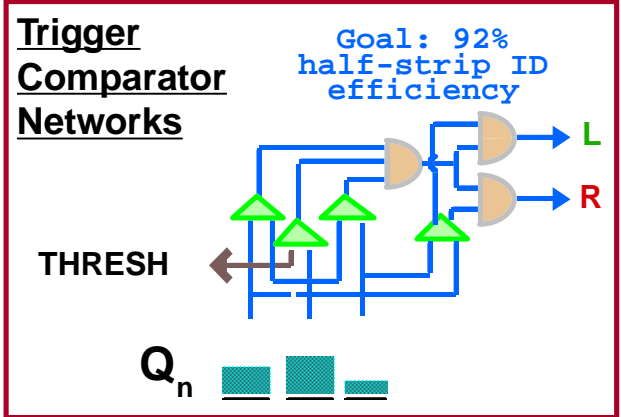
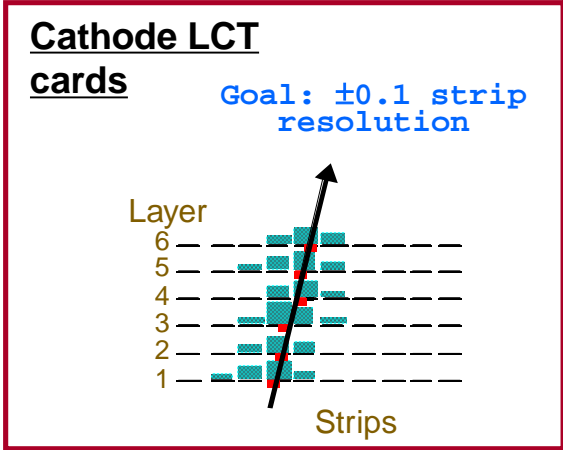
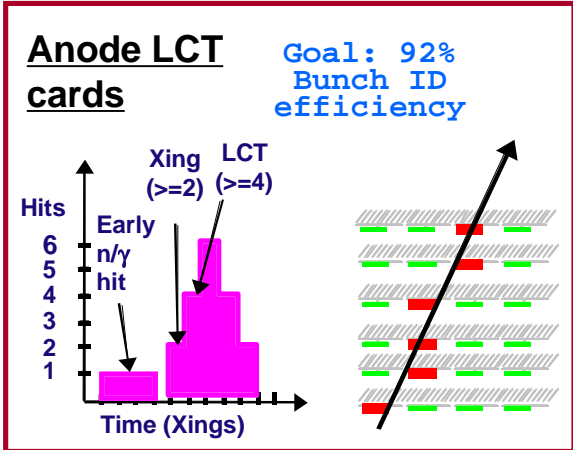
## Near-term planned activities

- Preparations for Summer '99 Test
- Designs of Prototype MPC, RC, SP



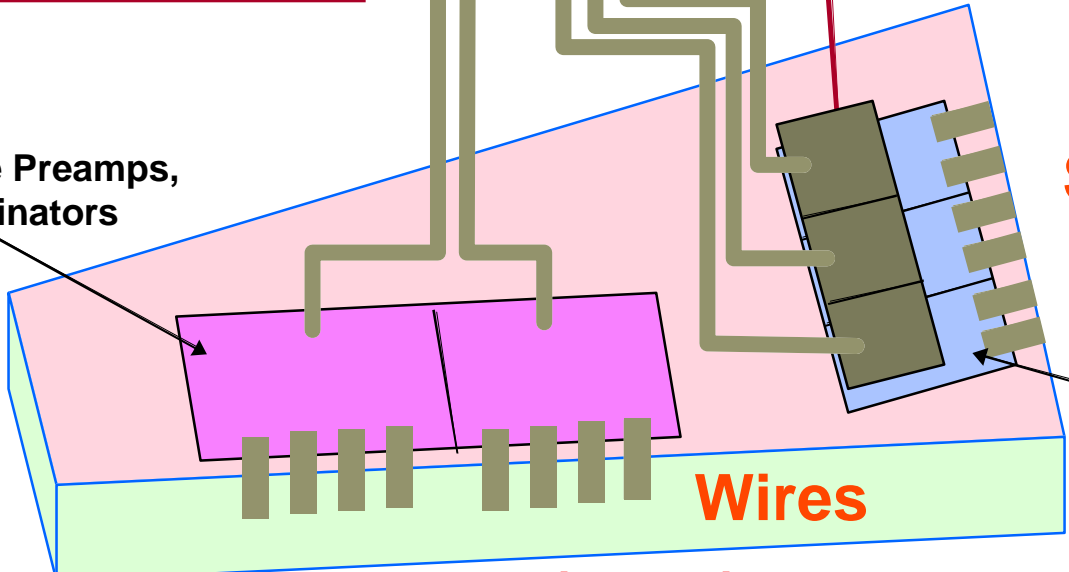
# Summer '98 CERN Beam Tests

LCT cards and Trigger Motherboard are in counting house (CAMAC)



**Trigger Motherboard**  
Goal: 99% efficiency for  $\pm 1$  BX correlation

Anode Wire Preamps, CF Discriminators



**P2 (large) chamber**



# Track-Finding in Overlap Region Vienna/Bologna Proposal

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- Data path: ME1/3 → DT T-F
  - special link from ME1/3 motherboard, or from Sector Receiver card.
- No modification to DT T-F hardware
  - ME1/3 becomes MB4 neighbor in  $\eta$
  - inputs already there
- $P_T$  measurement determined mostly from MB1/MB2 which are barrel chambers
- Simplifies CSC T-F:
  - Reduced Sector Processor logic and I/O
  - Reduced I/O for Sector Receiver cards (no fan-out)
  - Fewer CSC muons to sort
  - No CSC crate interconnections
- Saves CSC latency



# Track-Finding in Overlap Region

## U.S. Proposal

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- Data path: MB1+MB2 → CSC T-F
  - special DT Sector Receiver card
- CSC Trigger Motherboard design unchanged
- Uses  $\eta$  information for  $P_T$  determination
  - B-field changes by  $\pm 5\%$
- Full 3D Track-Finding in  $\eta$  and  $\phi$ 
  - reduces fakes
- Greater redundancy with ME2 in case ME1/3 misses hit

In any case, we can do track-finding in the overlap region with just the CSC chambers. Only lose  $P_T$  resolution without MB1 and MB2.



# CSC Electronics for Summer '99 Test Beam and FAST Sites

Commercial devices

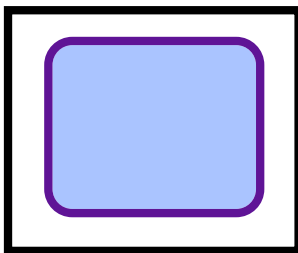
Clock distribution

Slow control

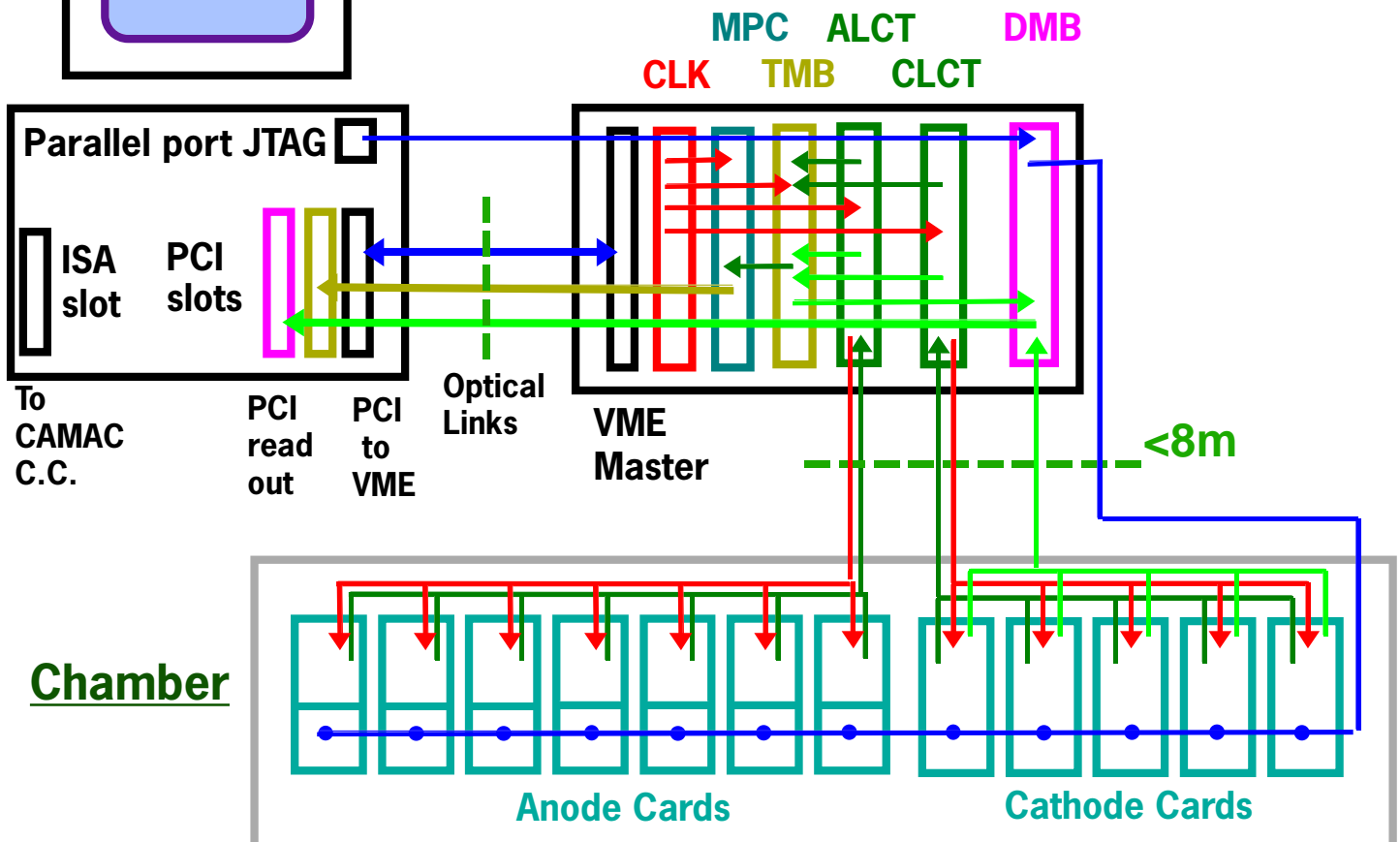
DAQ data

Trigger data

## Linux PC



9U Crate: ALCT, CLCT, TMB have VME slow control interfaces







# Concerns

## Calorimeter Trigger

- **HCAL Primitive Generation**
  - Can FE make tower sums?
- **Geometry**
  - Can we find a good endcap tower geometry?
- **Design Complexity**
  - Long vendor turn-around
  - Much vendor communication required
- **Integration**
  - System clocking
  - Interfaces with ECAL/HCAL/Global CAL

## Muon Trigger

- **Electronics on Periphery**
  - Is there room for the crates?
- **Data flow design: MPC → SR → SP**
  - Need details of processing, particularly in Sector Receiver, to proceed with Card Designs
    - New effort underway for exact bit accounting
- **Interface with Russian Groups on ME1/1**
- **Integration**
  - DAQ, Front End, & Slow Control Interfaces