



Task T -- CMS at the LHC

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Professors

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Senior Engineer

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Assistant Scientists

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PSL Engineers

M. Jaworski*

Physics Dept. Engineer

Calorimeter Trigger* -- W. Smith

- Simulation Results
- Hardware Developments

Common Projects -- R. Loveless

Muon Project -- D. Reeder



Wisconsin Senior Personnel Responsibilities

D. Reeder

- Acting US CMS Spokesman
- CMS Management Board
- US CMS Collaboration Board Chair
- US CMS Steering Committee
- US CMS Project Management Group
- US CMS Executive Committee

W. Smith

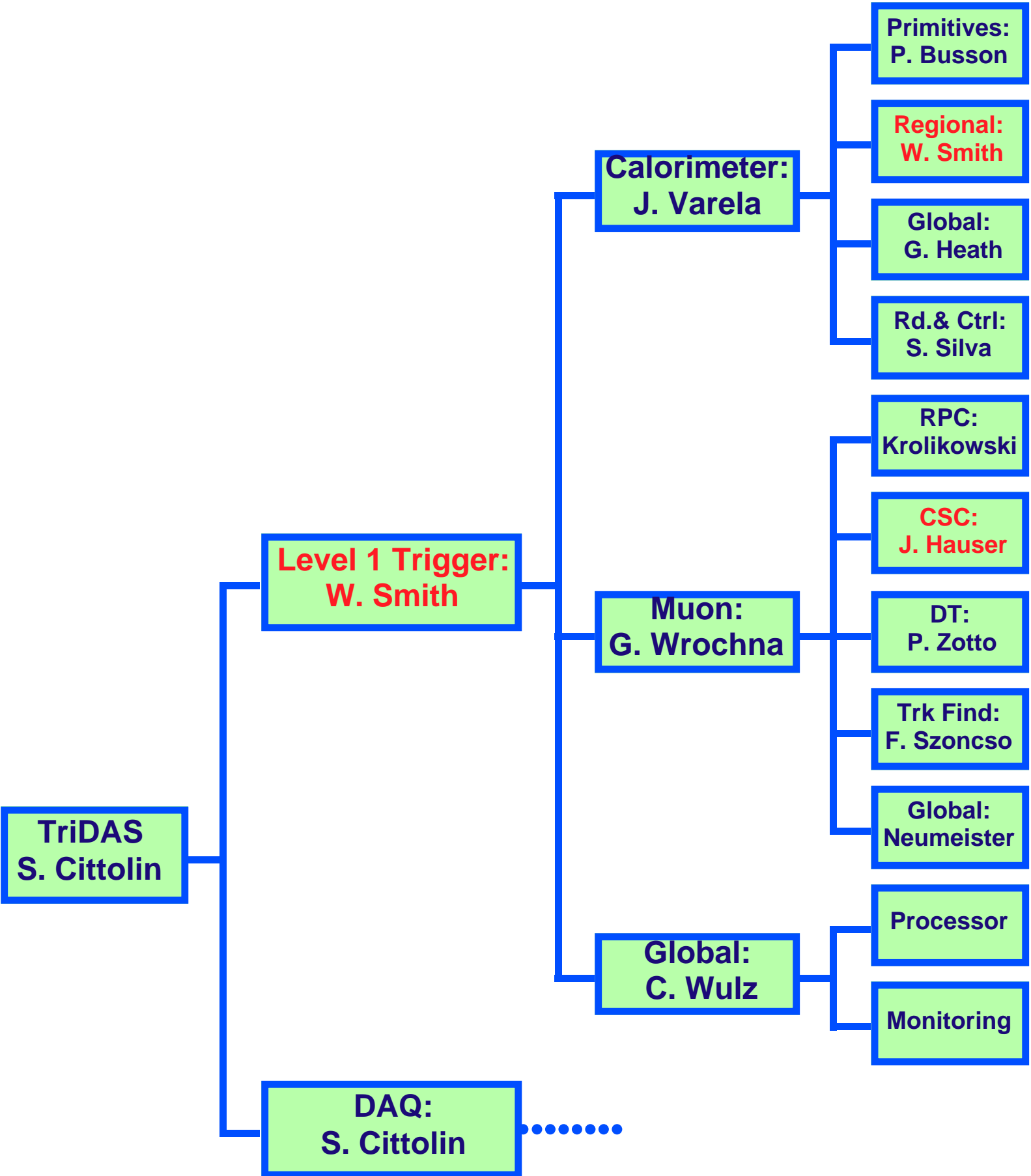
- CMS Trigger Project Manager
- CMS Steering Committee & Management Board
- US CMS Trigger Level 2 Manager
- US CMS Steering Committee
- US CMS Project Management Group
- LHC Electronics Board

R. Loveless

- US CMS Common Projects Level 2 Manager
- Endcap Muon System Technical Coordinator
- CMS Technical Board
- US CMS Steering Committee
- US CMS Project Management Group

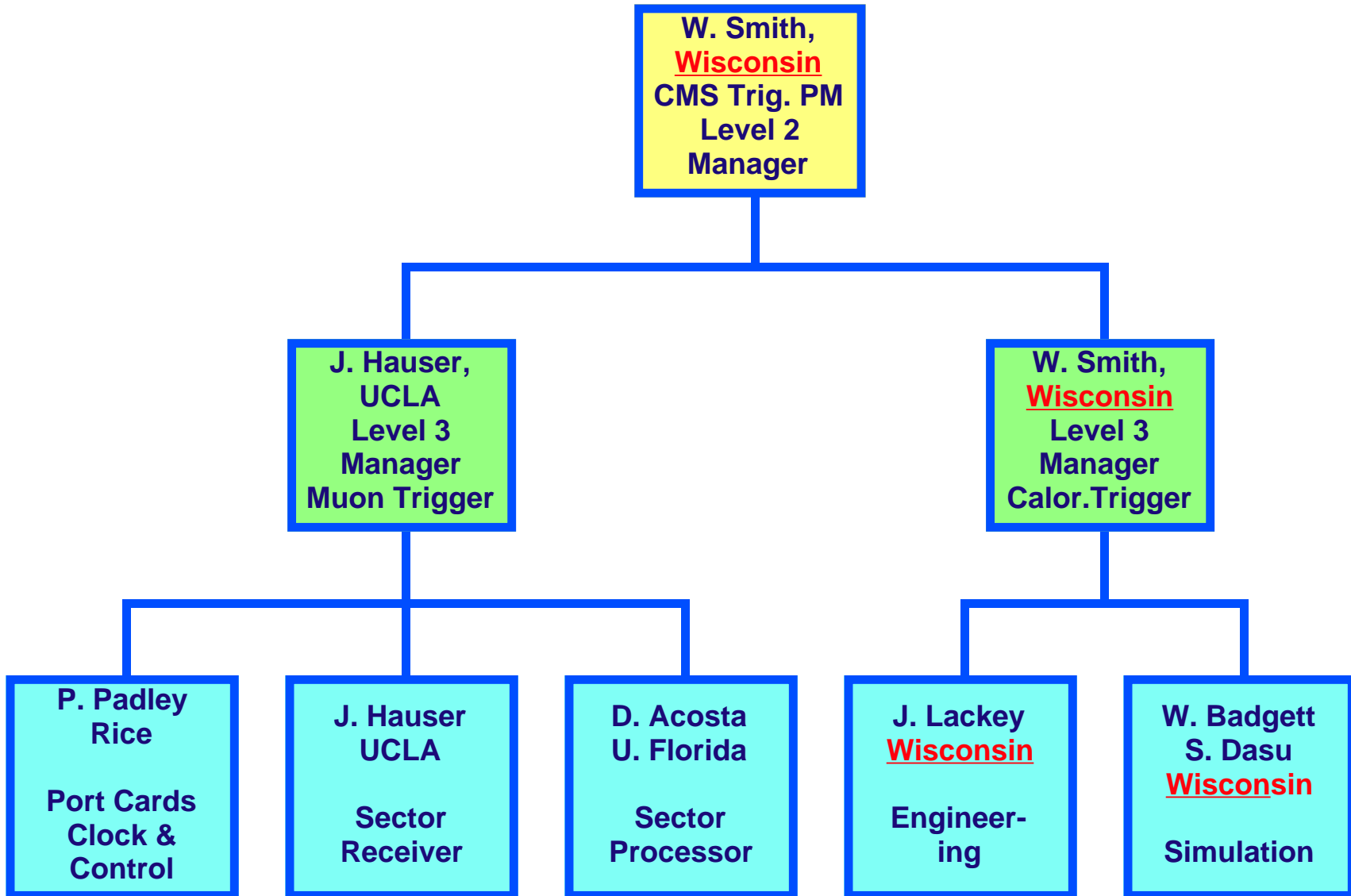


CMS Trigger Organization





U. S. Trigger Organization





Trigger Project Management

CMS Annual Reviews

- **April: TriDAS Status**
 - Progress, draft R&D plans & expenses for next year
- **November: TriDAS Internal Review**
 - R&D Plans/Progress, Cost & Schedule, Milestones
 - Finalize R&D plans & expenses for next year
 - Internal CMS Review w/CMS referees
- **Internal Electronics Reviews by LHC Electronics Board CMS Reps.**
 - G. Hall (Imperial), G. Stefanini (CERN), W. Smith (Wisc.)
 - Reports to CMS Management Board (next trigger review in Fall '98)

US Reviews/Reporting

- **Monthly Video Conferences:**
 - Florida, Rice, UCLA, Wisconsin, Davis (sim)
 - Review Progress, milestones, simulation activities
- **Integration Meetings:**
 - Calorimeter Trigger: FNAL, Maryland, Wisconsin
 - Muon Trigger: Ohio, Florida, Rice, UCLA, Wisconsin, others.
- **Annual Site Visits:** Florida, Rice, UCLA



CMS Task Support

Infrastructure Grant

- HP-RISC Processor Farm
- Scopes
- Pulse Generators
- Test Equipment
- (augmented by SSC equipment)

Mentor Graphics Grant

- Full CAD Software Suite

UW 95-96 Support of Personnel

- J. Lackey
- S. Dasu
- PSL Engineering

UW Equipment Support

- Teleconference Equipment
- Video Room Remodeling
- CAD Printers

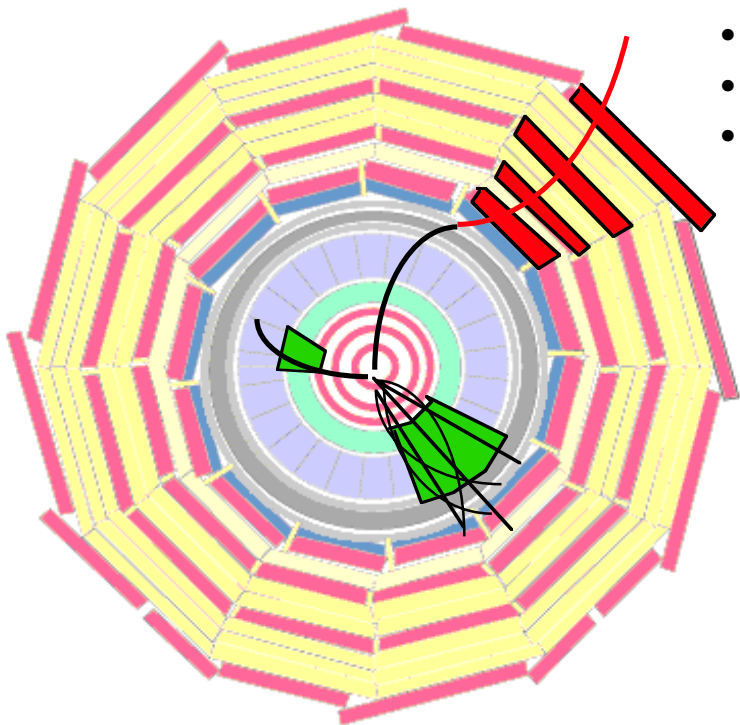
UW CAD support

- Purchase of Visula PCB Suite
- Includes specialized high speed router
- New version of Zeus trigger design suite

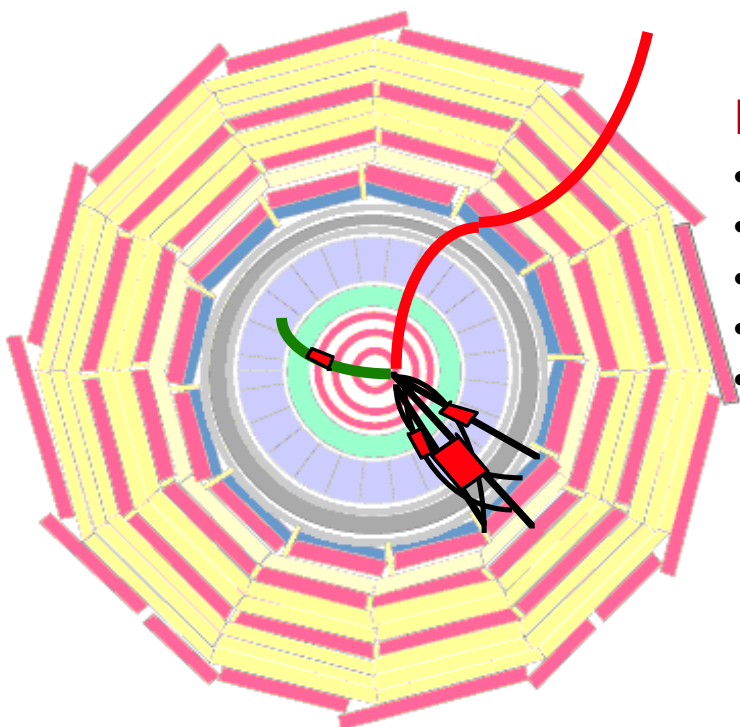


CMS Trigger Levels

40 MHz



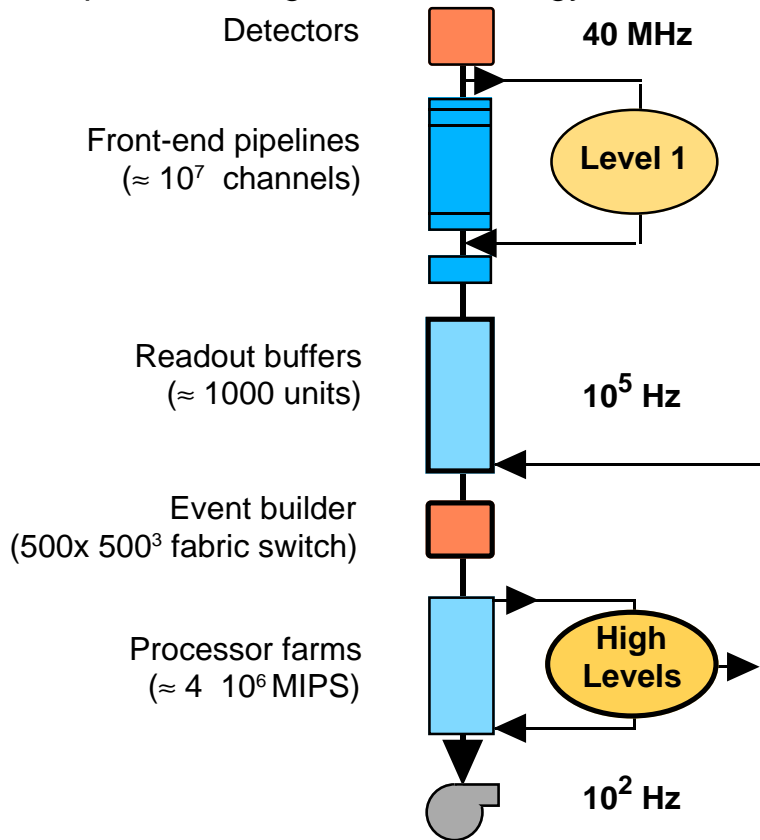
up to 75 kHz



≈ 100 Hz

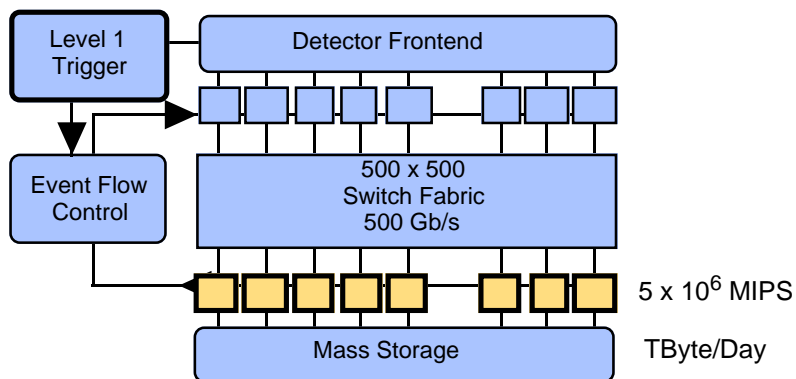
Level-1. Specialized processors

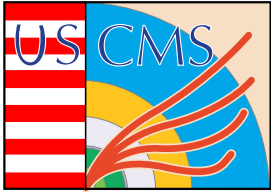
- Particle ID: electron/ γ , muon, jets, missing E_T
- Coarse granularity to reduce data volume
- Local pattern recognition and energy sums



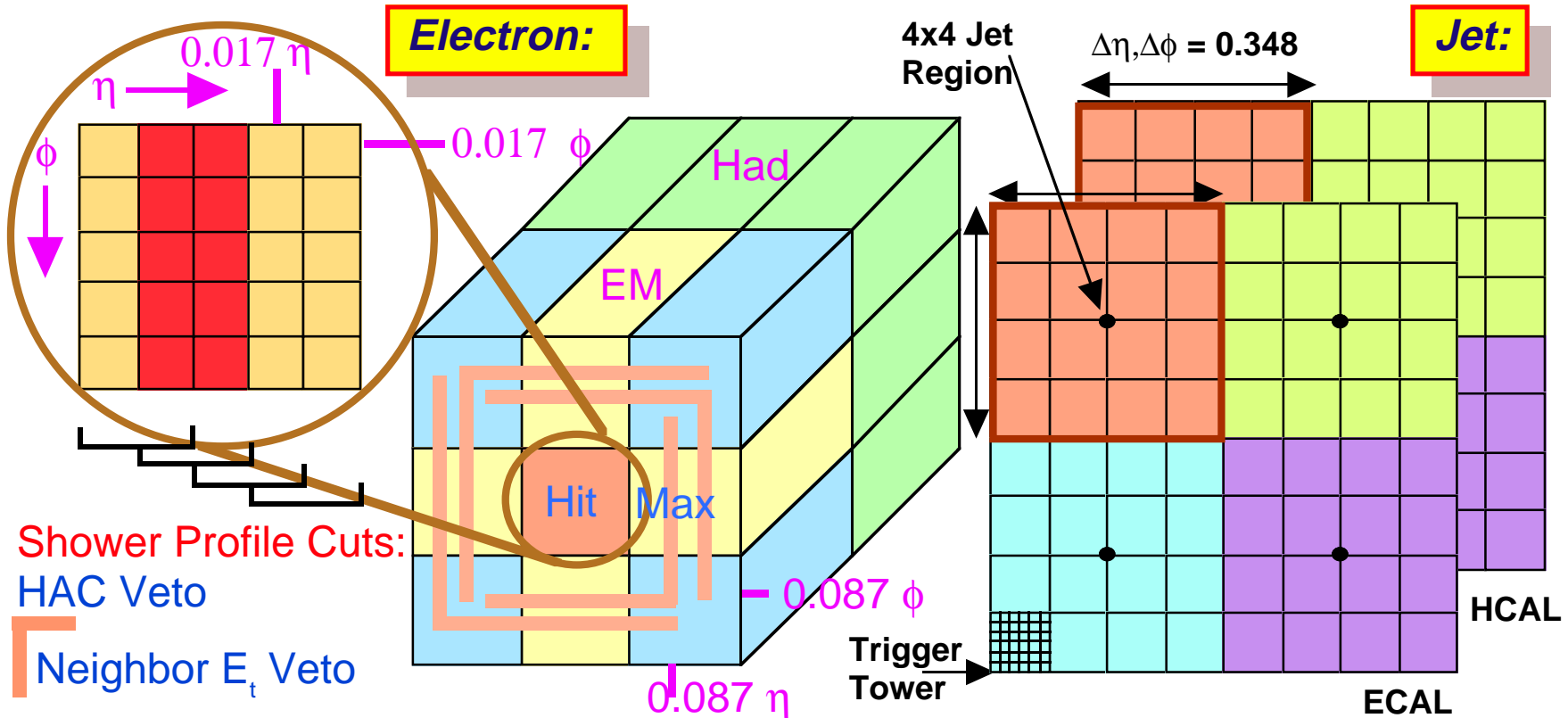
High trigger levels. CPU farms

- Clean particle signature (Z, W, quarks..)
- Finer granularity precise measurement
- Kinematics. Effective mass cuts and topology
- Track reconstruction and detector matching
- Event reconstruction and analysis





Calorimeter Triggers (Wisconsin Design)



Shower Profile Cuts:
HAC Veto
Neighbor E_t Veto

**3 x 3 sliding window
centered on ECAL/HCAL
trigger tower pairs
Tower count =
 $72\phi \times 54\eta \times 2 = 7776$**

**Jet E_t from sum of ECAL & HCAL
trigger tower E_t in non-overlapping 4x4
regions (also used for $E_{x'}$, $E_{y'}$, $E_{t'}$, E_t^{Miss})
Use multijet triggers
Jet candidates are sorted to find
highest energy jets**



Simulation programs

FASTSIM - Fast simulation of event response

- Simplified CMS geometry, uniform tracking medium, meson decays & parameterized calorimeter showers

CMSIM - Version 111

- CMS standard GEANT based detector simulation
- Detailed calorimeter geometry, average tracker

PYTHIA - common for FASTSIM/CMSIM

- QCD background events are used for rate studies.
- High P_t signal events, e.g., top, Higgs and SUSY particle decays, are used for efficiency studies.
- Noise hits are superposed with high P_t events.
- Minimum bias included - FASTSIM minbias is added for both CMSIM and FASTSIM.

Trigger simulation - common for FASTSIM/CMSIM

- Various digital scales with limited resolution and dynamic range involved in the trigger system are fully implemented.
- Algorithms are performed in integer arithmetic using memory lookup tables when needed.

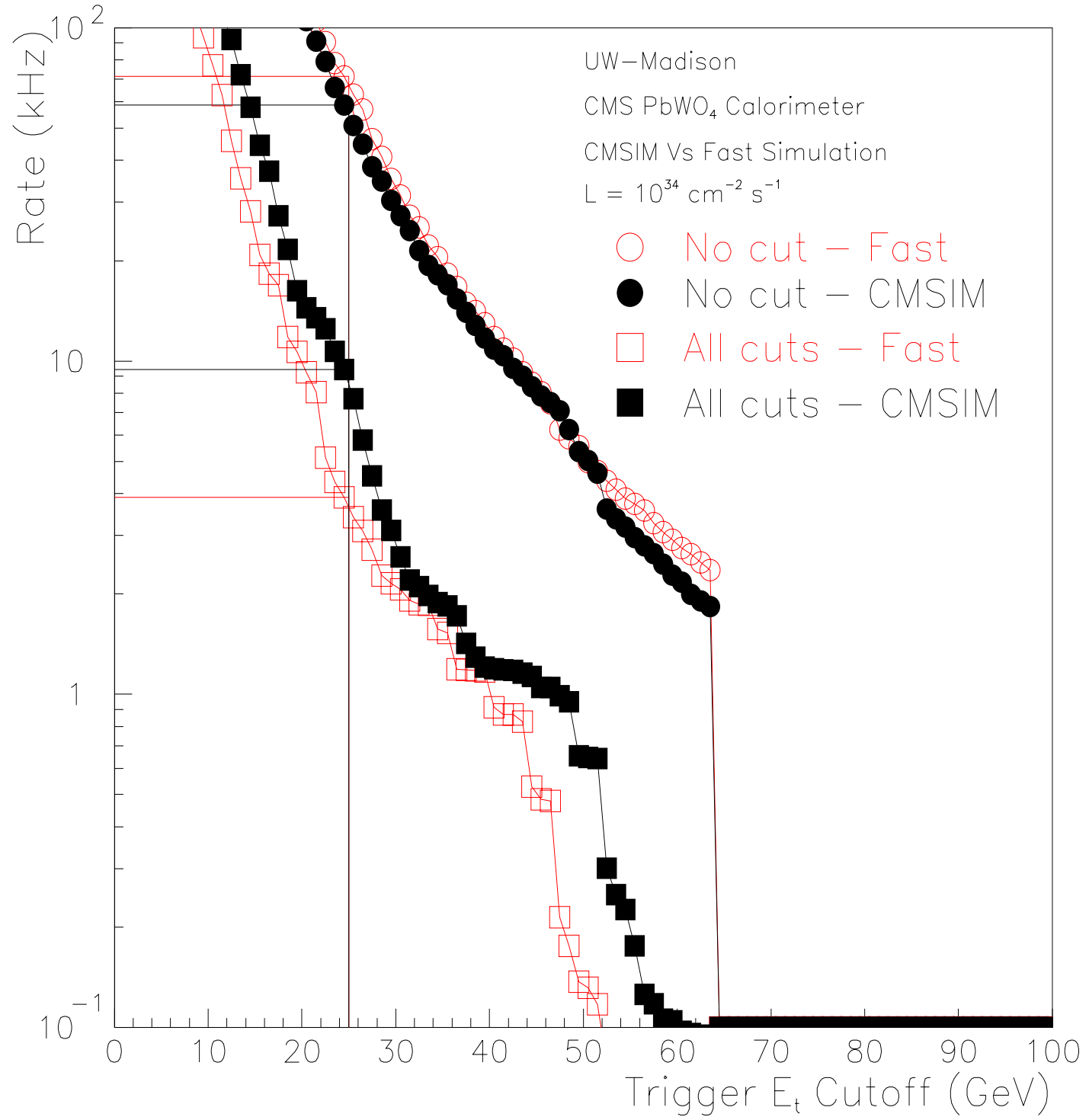
Wisconsin Role:

- FASTSIM & CMSIM Trigger Code Author: **S. Dasu**
- Upgrade of FASTSIM & New CMSIM: **W. Badgett**



Electron/Photon Rates

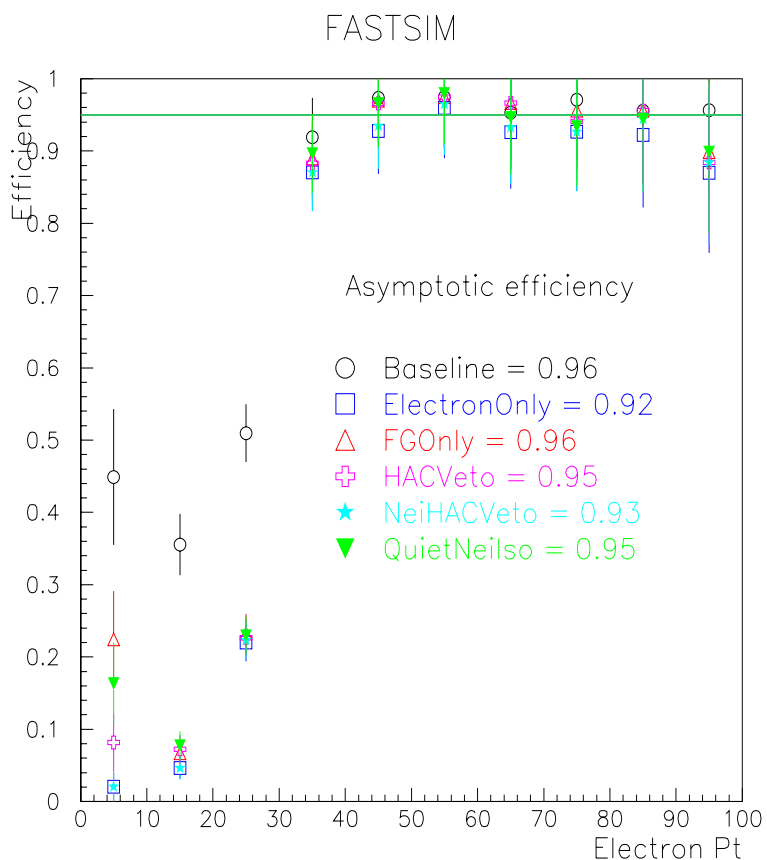
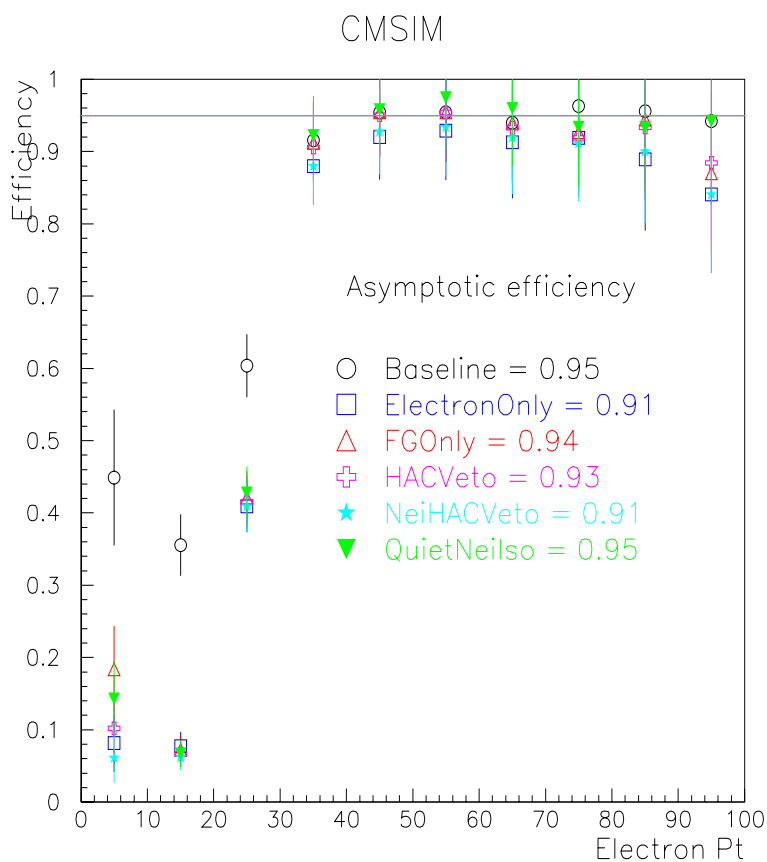
Electron/photon trigger rates



Integrated rate above E_t cut is plotted versus E_t cut.
All four, i.e., finegrain, HAC veto, neighbor HAC veto and quiet neighborhood, cuts are included.
For 25 GeV E_t cut, CMSIM rate is 9 kHz versus to 4 kHz in FASTSIM



Electron/photon Efficiency



Efficiency for triggering top to electron decay events is plotted versus the P_t of the electron for various cuts.

Identical values for the four cut parameters yield similar efficiencies - custom tuning was not necessary.

All efficiencies are over 90%.

Note: drop at high E_t is artificial. Actual trigger removes conditions at high E_t



Physics at high luminosity

Wisconsin Simulation for Luminosity = $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$

Trigger Type	Trigger Et Cutoff (GeV)	Rate (kHz)				Process	Efficiency (%)		
		CMSIM		FASTSIM			CMS-TN-95/183	FASTSIM	CMSIM
		Individual	Incremental	Individual	Incremental				
Sum Et	400	0.3	0.3	0.4	0.4	H (80 GeV) $\rightarrow \gamma\gamma$	97	92	94
Missing Et	80	1.2	0.9	1.7	1.3	H (120 GeV) $\rightarrow Z Z \rightarrow e e \mu \mu$	76*	76*	74*
Electron	25	11.4	9.3	4.5	3.9	H (200 GeV) $\rightarrow Z Z \rightarrow e e j j$	99	96	95
DiElectron	12	2.1	1.8	1.0	1.0				
Single jet	100	1.5	1.0	2.0	1.3	$p p \rightarrow t t \rightarrow e X$	88	82	82
Dijet	60	1.2	0.7	1.9	1.1	$p p \rightarrow t t \rightarrow H X \rightarrow t X$	82	76	76
Trijet	30	2.3	1.3	3.1	1.8	SUSY CMS TP Scenario A ($M_{LSP} = 45, M_{\text{spart}} \sim 300 \text{ GeV}$)	83#	-	-
Quadjet	20	2.6	1.1	3.3	1.4				
Jet+Elctrn	50 & 12	1.3	0.3	0.7	0.2				
Cumulative Rate		16.7		12.4					

QCD Background

The sum & missing E_t cutoffs chosen to yield 2 kHz rate.

Electron/photon triggers are emphasized, ~8 kHz rate out of total available 15 kHz.

Remaining 5 kHz available for jet triggers.

Signal Efficiency (no offline cuts)

High efficiency for all channels with electrons and photons.

The difficult-to-trigger top decay events have high efficiency, enabling studies of associated Higgs production.

*Inclusion of muon trigger gives full efficiency



Calorimeter Trigger Overview

Wisconsin Responsibility Circled

4K 1 Gb/s serial links with:
 2 x (8 bits EM or HAC Energy)
 + 5 bits error detection code
 (+ fine grain isolation (or H1) bit)
 72 ϕ x 54 η Towers (.087x.087ea)
 every 25 ns.

US CMS HCAL:
 FNAL/
 Maryland

Calorimeter
 Electronics
 Interface

CMS ECAL:
 Lisbon/
 Palaiseau

Copper40 MHz Parallel
 4 Highest E_t e/γ
 4 Highest jets
 E_x, E_y from each crate

US CMS Trigger:
 U. Wisconsin

Calorimeter
 Regional
 Trigger
 (WBS 3.1.2)
 Receiver
 Electron Isolation
 Jet/Summary

E_t sums

US CMS HCAL:
 U. Nebraska

Lumi-
 nosity
 Monitor

US CMS HCAL:
 U. Nebraska

Lumi-
 nosity
 Monitor

E_t sums

Cal. Global Trigger
 Sorting, E_t^{Miss} , ΣE_t

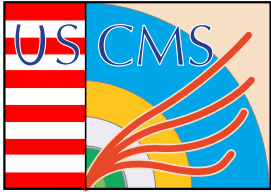
UK CMS:
 Bristol

Global
 Trigger
 Processor

CMS:
 Vienna

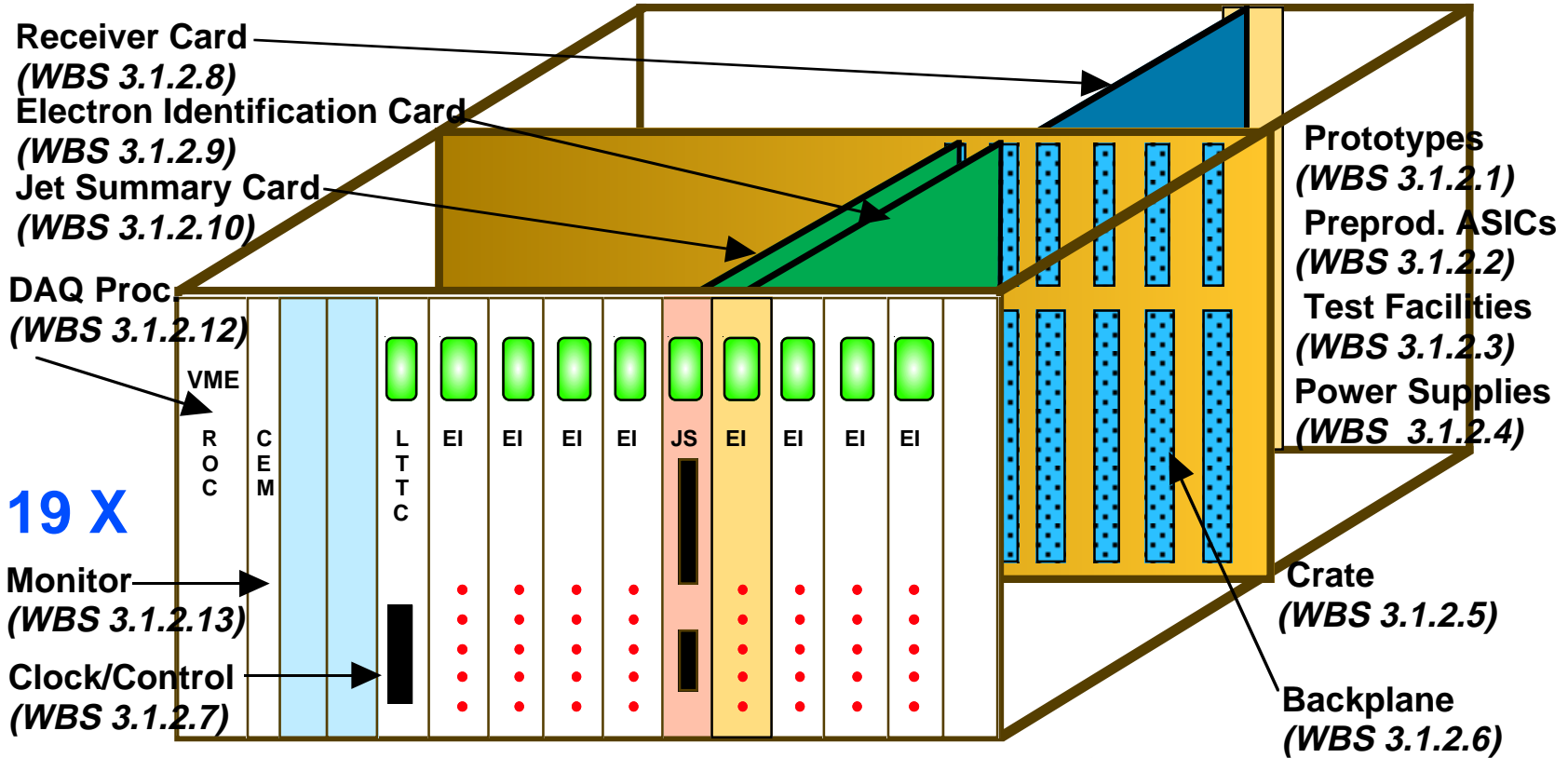
Muon Global Trigger
 Iso Mu Minlon Tag

Minlon Tag for
 each $4\phi \times 4\eta$ region



Regional Calorimeter Crate

(WBS 3.1.2: Full Wisconsin Responsibility)



Data from calorimeter FE on Cu links @ 1.2 Gbaud

- Into 152 rear-mounted Receiver Cards (proto. being built)

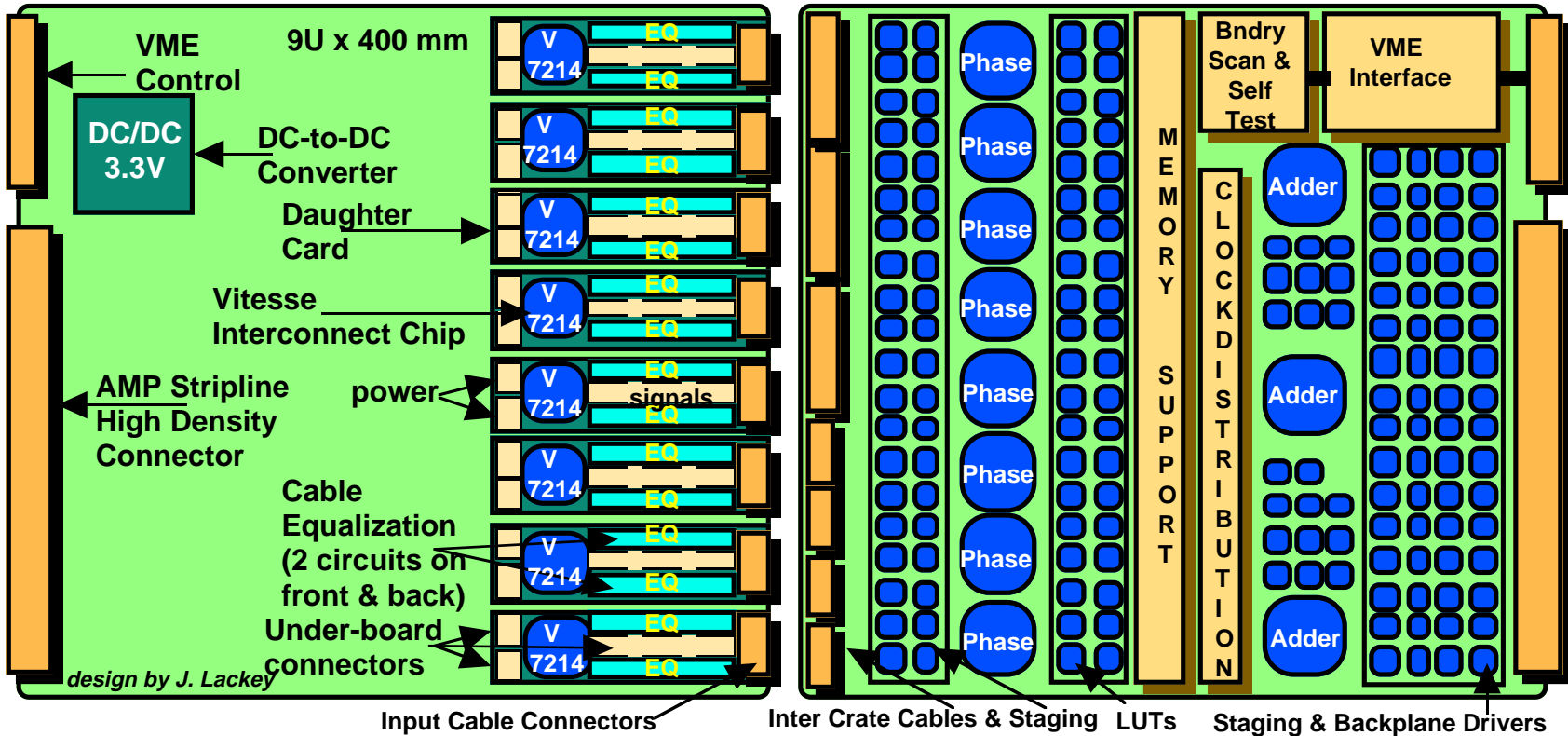
160 MHz point to point backplane (proto. built)

- 19 Clock&Control (proto. built), 152 Electron Identification, 19 Jet/Summary Cards & Receivers operate @ 160 MHz



3.1.2.8: Receiver Card

(prototype being built by U. Wisconsin)



Rear:
 32 Channels =
 4 Ch. x 8 mezzanine cards
 1.2 GBaud copper rcvrs
 18 bit (2x9) data + 5 bit error
Vitesse Chip:
 Converts Serial to Parallel

Front: Data from Rear @ 120 MHz TTL
Phase ASIC: Deskew, Mux @ 160MHz
 Error bit for each 4x4, Test Vectors
Memory LUT @ 160 MHz
Adder ASIC:
 8 inputs @ 160 MHz in 25 ns. (built!)
 Differential Output @ 160 MHz

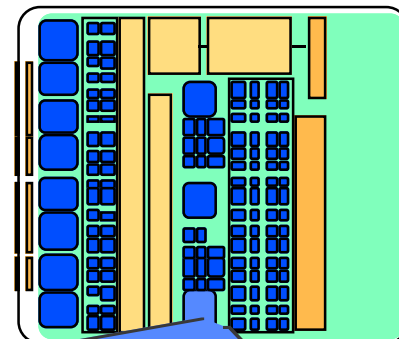


8 x 13-bit 160 MHz Adder ASIC

Vitesse 0.6µ H-GaAs Process: ECL I/O

- 13 bits per operand x 8 operands
- Single thirteen bit output
- Latency: 25 ns @ 160 MHz
- Full Boundary Scan support

Receiver Card:

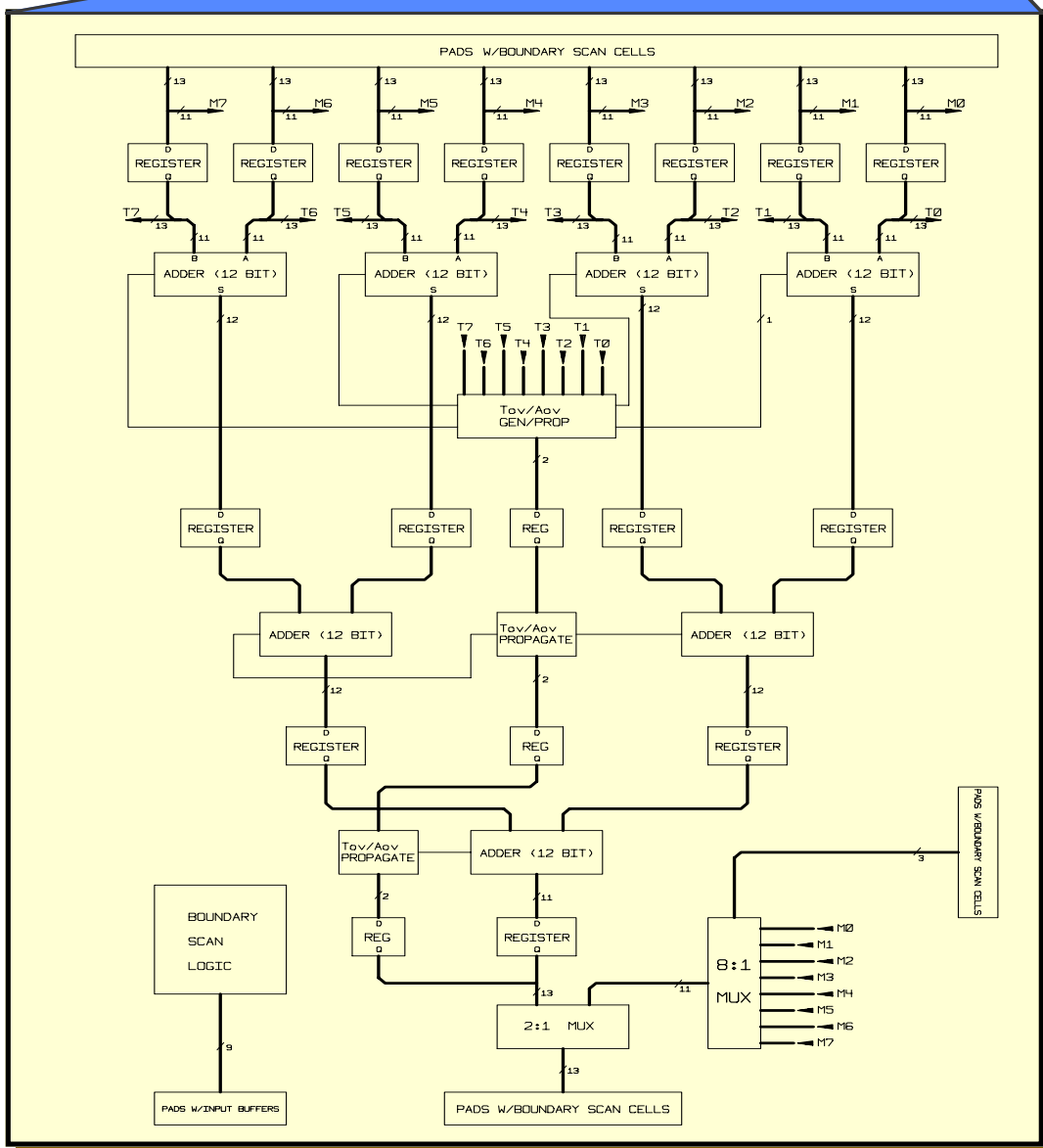


Technical analysis by Vitesse

- ~11,000 cells
- 4 Watts
- 308 MHz

Status:

- 5 tested devices delivered
- select nets exceed simulation speed by 10%

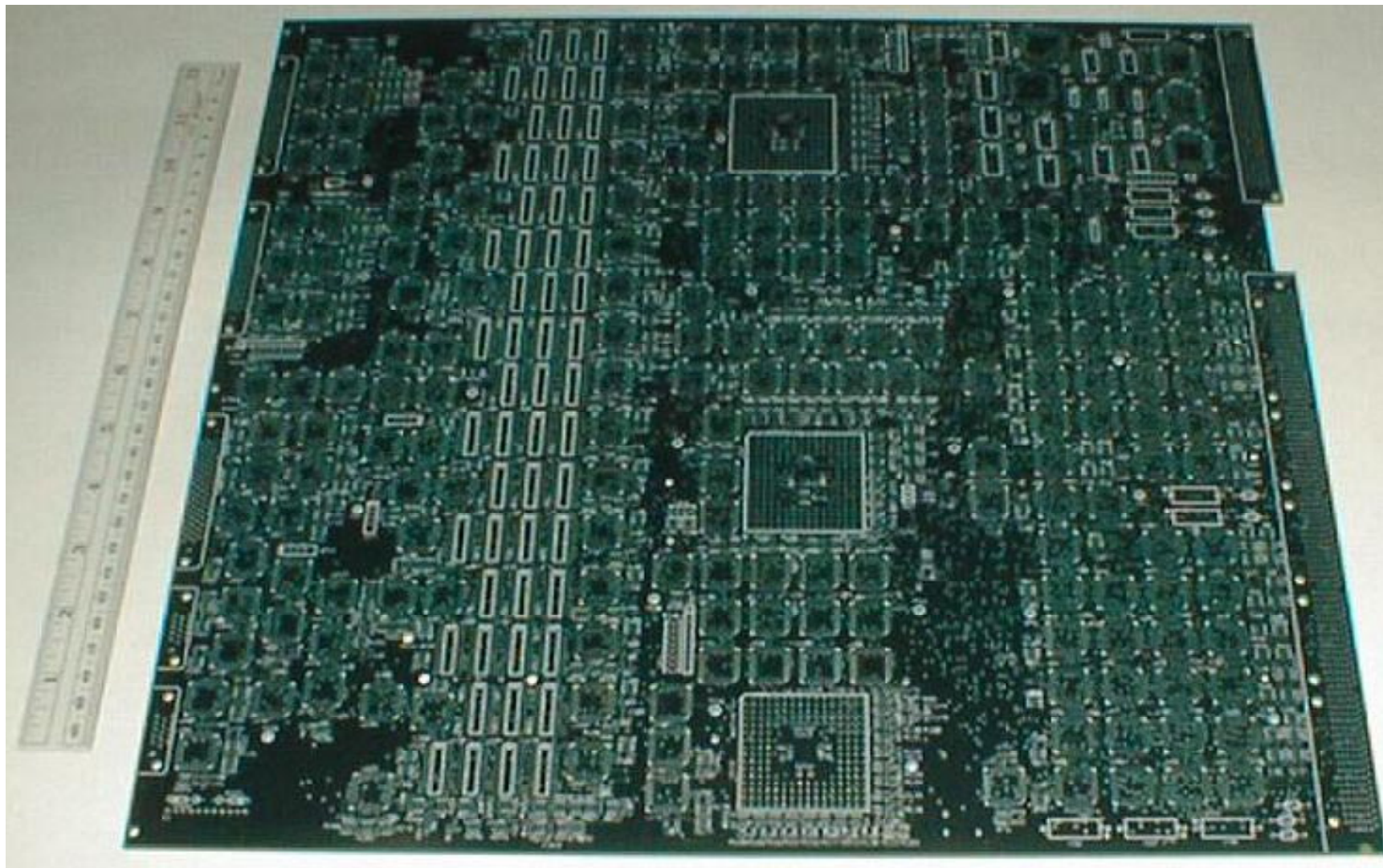


- J. Lackey



Receiver Card Prototype

Card built, assembly next

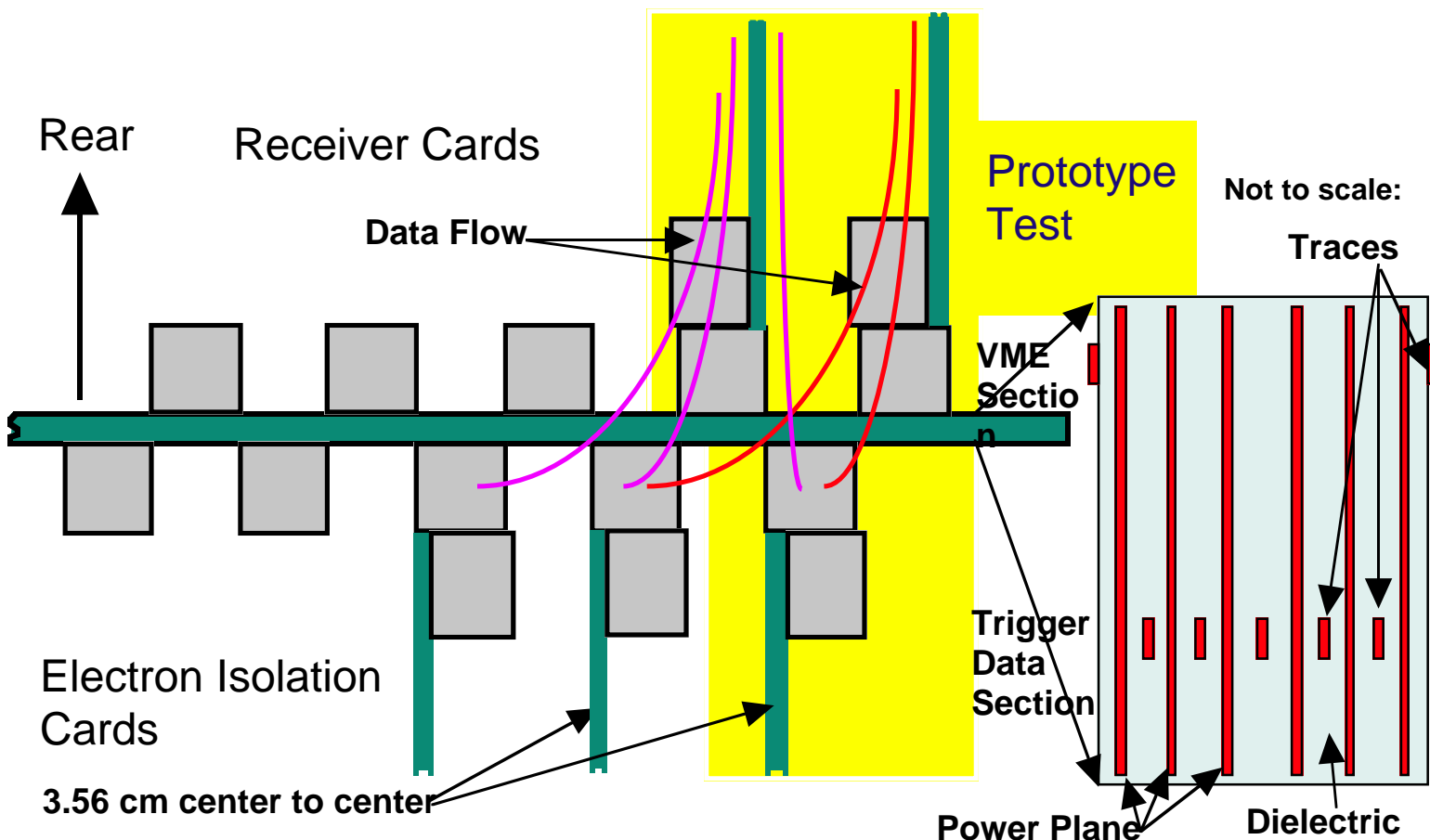




160 MHz Backplane

Monolithic 9U High Backplane

- Incorporates std. 32 bit VME in top connector position
 - Single 128 pin DIN in Trigger Processor Card area
 - Two 96 pin DIN connectors in left most slot positions
- Data sharing on backplane
 - Reduces the number of receivers, serial to parallel convertors, and synchronizing circuits
- Stripline construction w/ five ground and power planes
 - 50 Ω impedance to match connectors and boards
 - 1 oz. copper with multiple power points
- Five signal layers
 - Handles routing density thru connector pins
 - Differential pairs are held to the same layer
 - Point to point on high speed data paths @ 160 MHz





Prototype Clock Board

- J. Lackey & M. Jaworski
U. Wisconsin

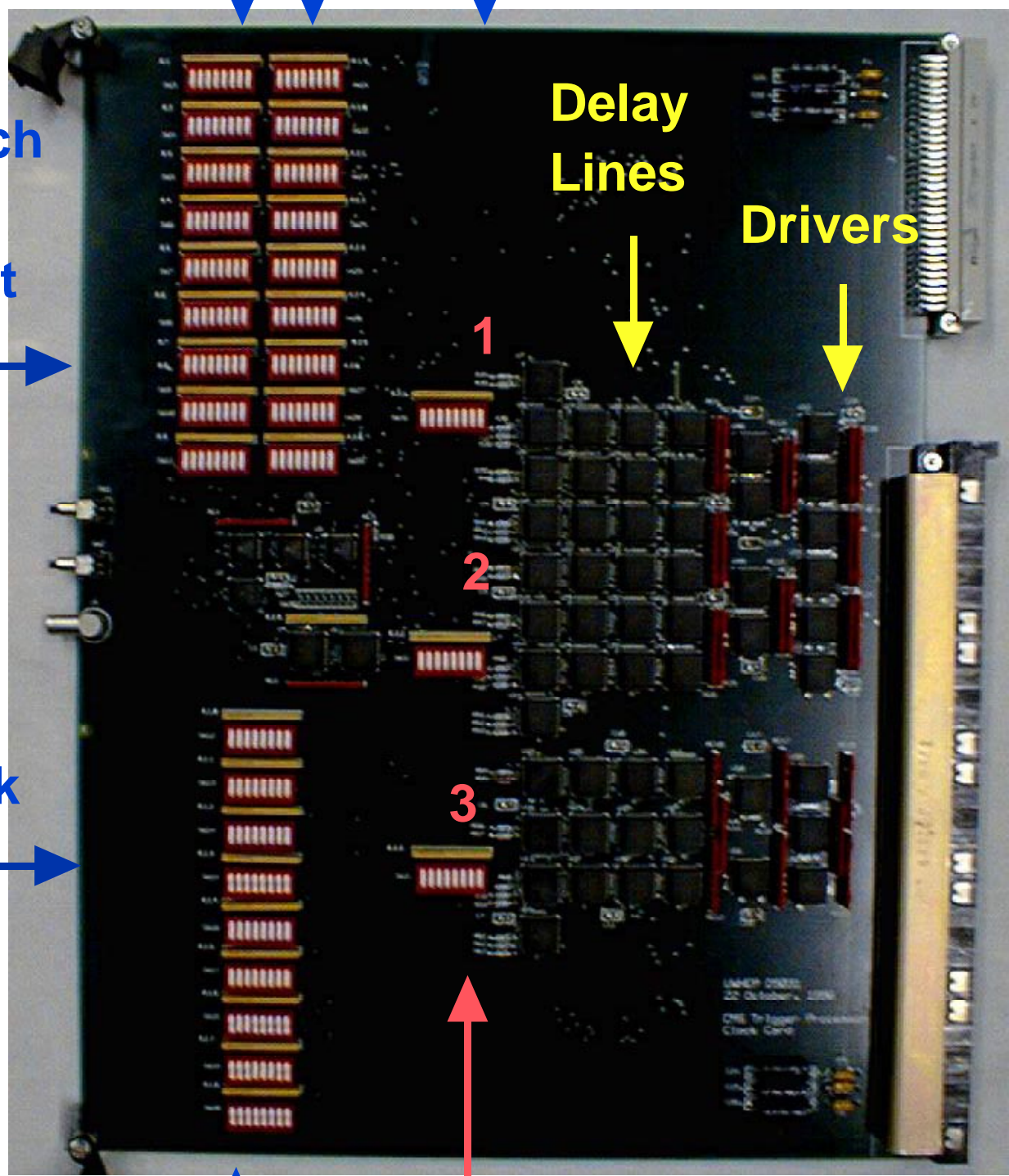
switches to set delay lines

synch
&
reset

clock

Delay
Lines

Drivers



1:Rcvr-E.I. 2:clk-sync 3:clk-reset

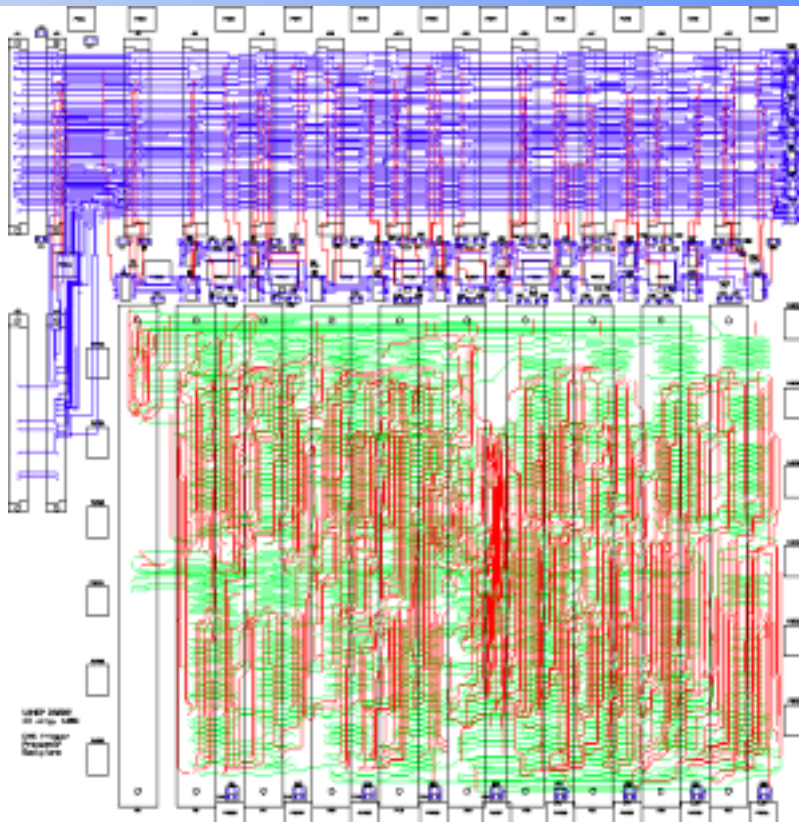
4 Recvr Cards, 4 Electron Iso, 1 Jet/Sum



160 MHz Backplane Prototype

**Display 3 of 5
signal layers:**

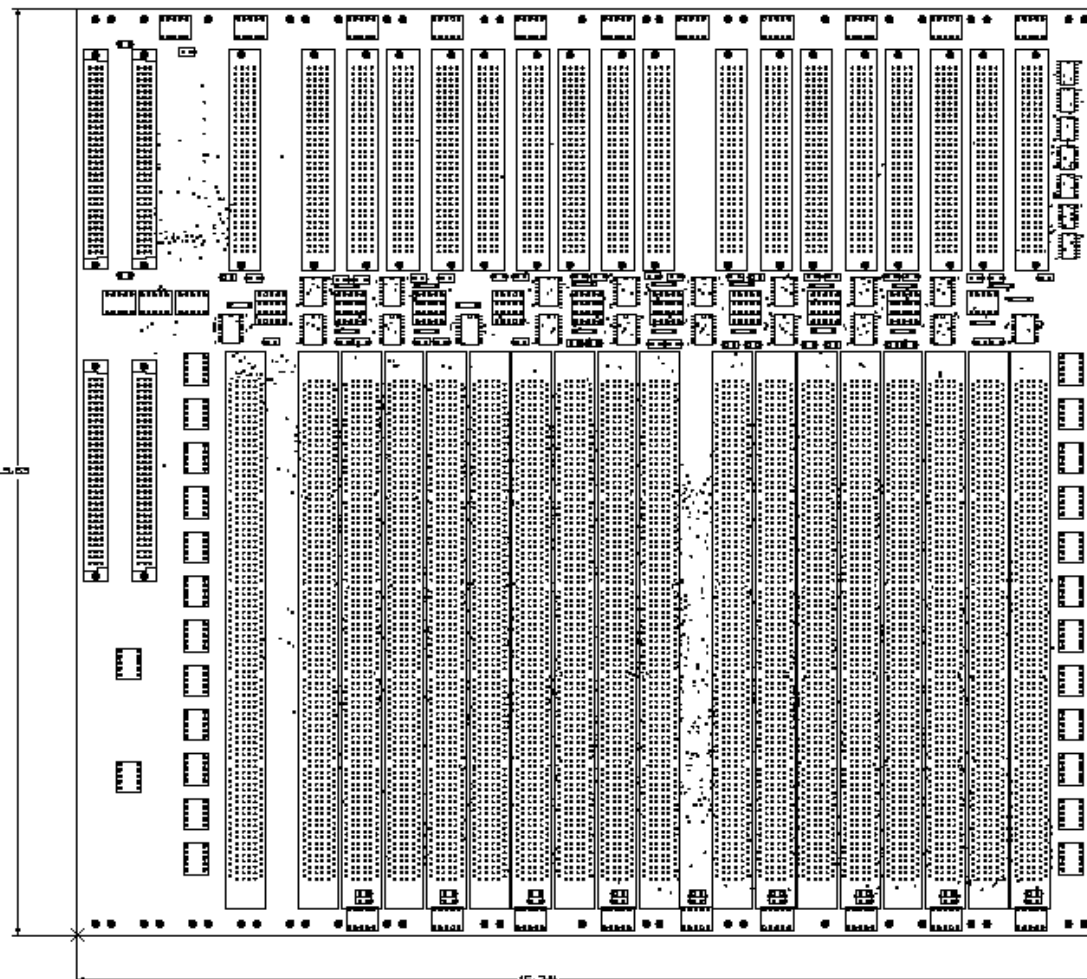
(most signals
are hidden by
top layer)



Board layout:

(Alternate
connectors on
opposite sides)

std.
2
conn.
VME
area



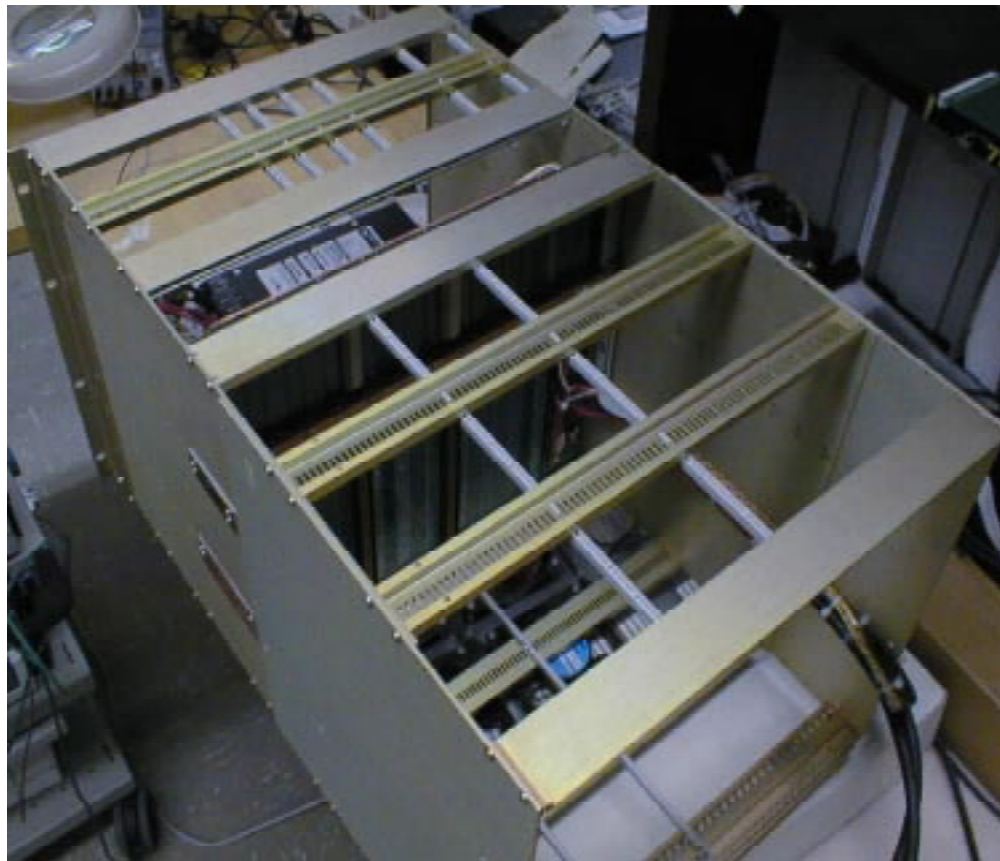
single
VME
connector

trigger
processing
area

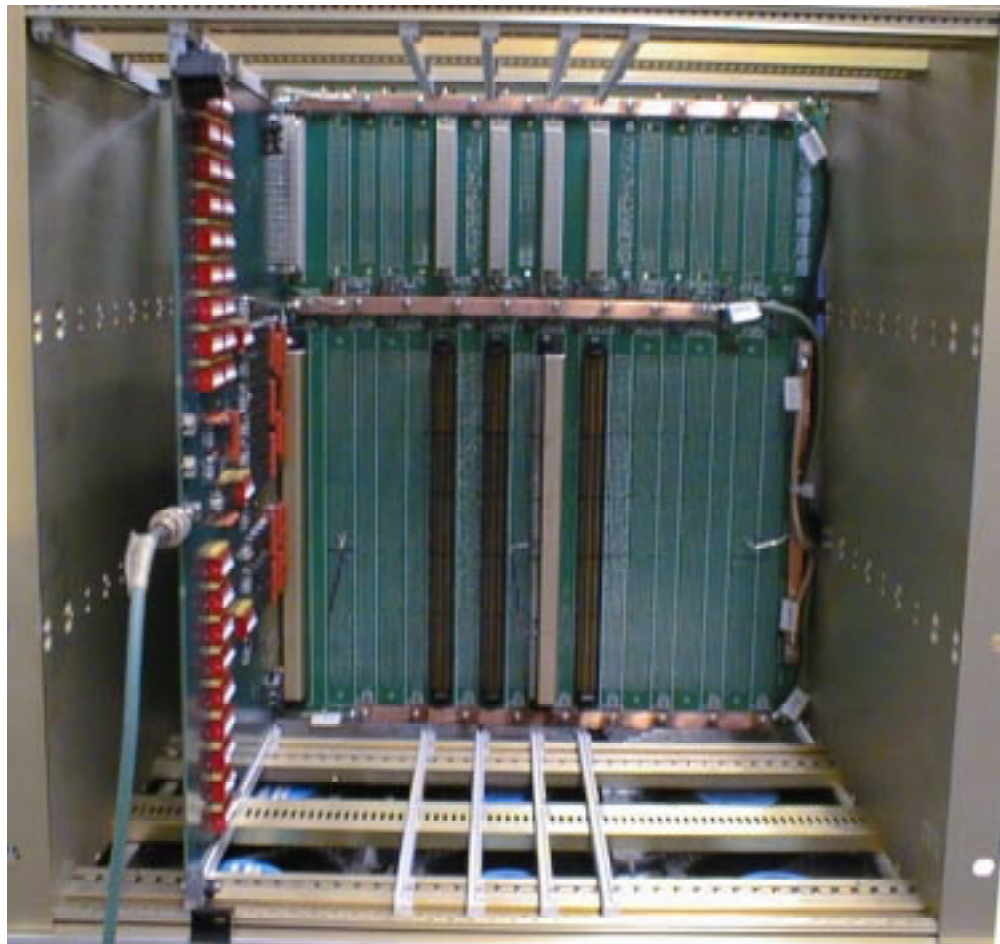
- J. Lackey



Backplane Test Setup



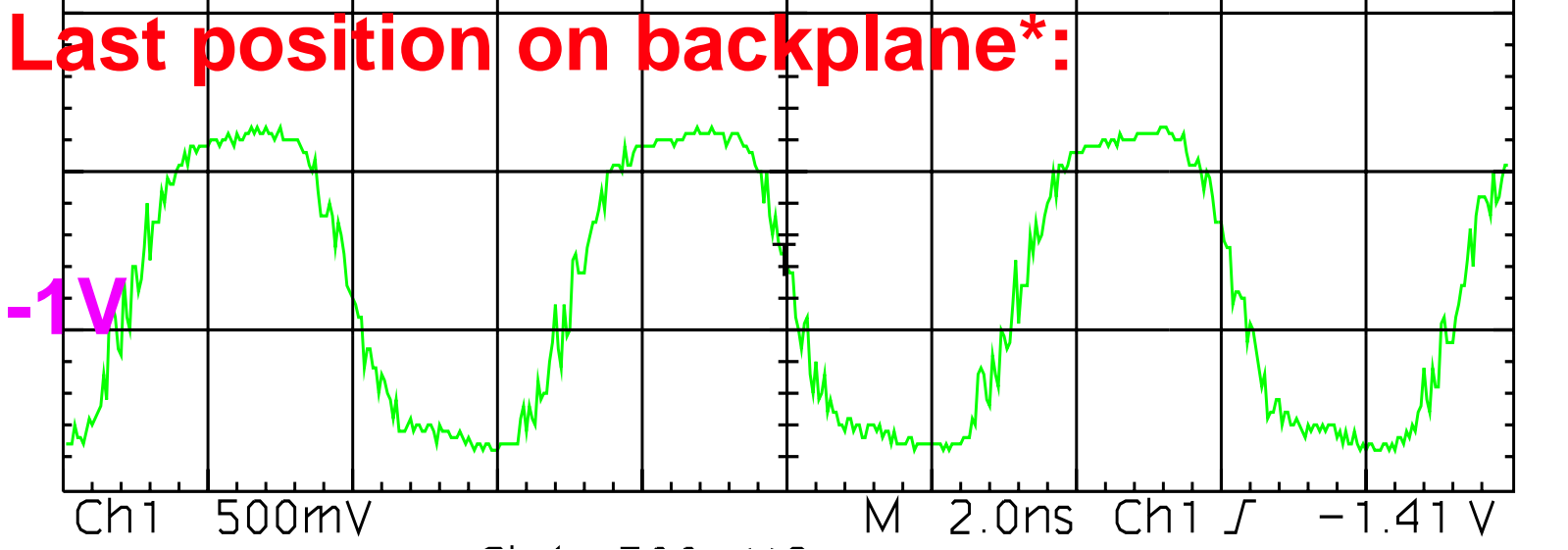
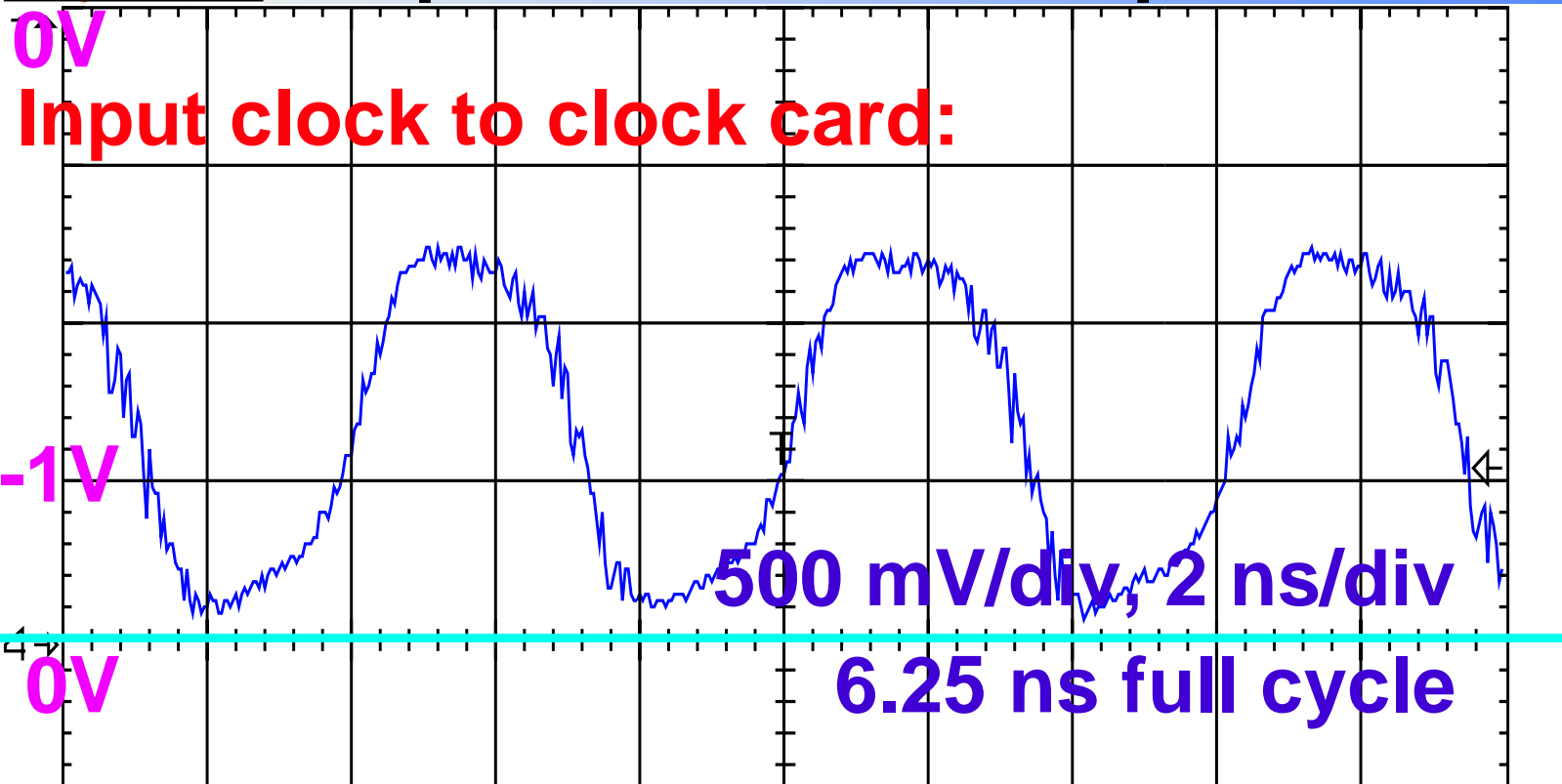
Top rear view of crate & backplane with power supplies



Front view of crate & backplane with clock board installed



Backplane Test Results



***one side of differential pair**

Conclusions:

- Output of backplane rise 820 ps
- Output of backplane fall 840 ps
- Measured 20% to 80%



CMS Cal. Trigger '98/'99

Full dataflow tests

- Receiver Card Prototype
- Backplane Prototype
- Electron Identification Card Prototype

Electron Isolation ASIC

- Design in Vitesse GaAs
- Produce Prototype

Prototype Jet Summary Board

- Trigger data summary generation
- Data transmission to global cal. trig.

Intercrate data transfer

- Second crate & backplane
- Test transmit/align techniques

System Design

- Interfaces to HCAL & ECAL (Geometry)

Detailed Simulation

- Update/improve full GEANT - CMSIM
- Verify against fast simulation results
- Study processing of level 1 by higher levels
- study b-physics triggers
- use of quiet regions by muon triggers



Conclusions from May '98 Lehman Review

TRIDAS:

"The U.S. CMS Trigger and Data Acquisition groups have made excellent progress since the previous Lehman Review. The effort has strong leadership in place and is capable of meeting their obligations to CMS."

Trigger:

"The Trigger group is well advanced in design and has a clearly defined path to completion"

Simulation:

"The trigger simulation studies...provided estimates of the overall Level 1 trigger rate which are important for justifying the reduction in the Level 1 trigger rate and associated DAQ bandwidth from 100 kHz to 75 kHz."

Technical, Cost & Schedule:

"The Trigger project is well advanced and have developed detailed planning and reference documentation...the Trigger and DAQ groups are well managed and have clear mechanisms in place for decision-making and for reporting and monitoring expenses."



Conclusions

CMS Regional Calorimeter Trigger

- **Inputs on 1.2 Gbaud Cu serial links**
 - 8-bits energy & 1 bit fine grain/trigger tower
 - Careful mapping of calorimeter towers into trigger logic
- **Receiver Card scales, sums, preprocesses**
 - Prototype being manufactured
 - Designed to receive data from serial links
 - Designed to operate @ 160 MHz
 - 13 x 8 bit Adder ASIC tested > 160 MHz
- **Backplane for VME & trigger data**
 - Prototype constructed/tested
 - Prototype Clock Card constructed/tested
 - Signal performance excellent @ 160 MHz
 - Confirmation of design feasibility
- **Electron Isolation & Jet Summary Cards**
 - Receive data from Backplane
 - Algorithms matched to data & physics
 - Next on development plan
- **Simulation & Hardware Plans for '98/'99**
 - Comprehensive program