CMS TriDAS Report

Wesley H. Smith
CMS Trigger Project Manager

March 7, 2002

Trigger:

Calorimeter Trigger Status

Muon Trigger Status

Global Trigger Status

DAQ (on behalf of S. Cittolin):

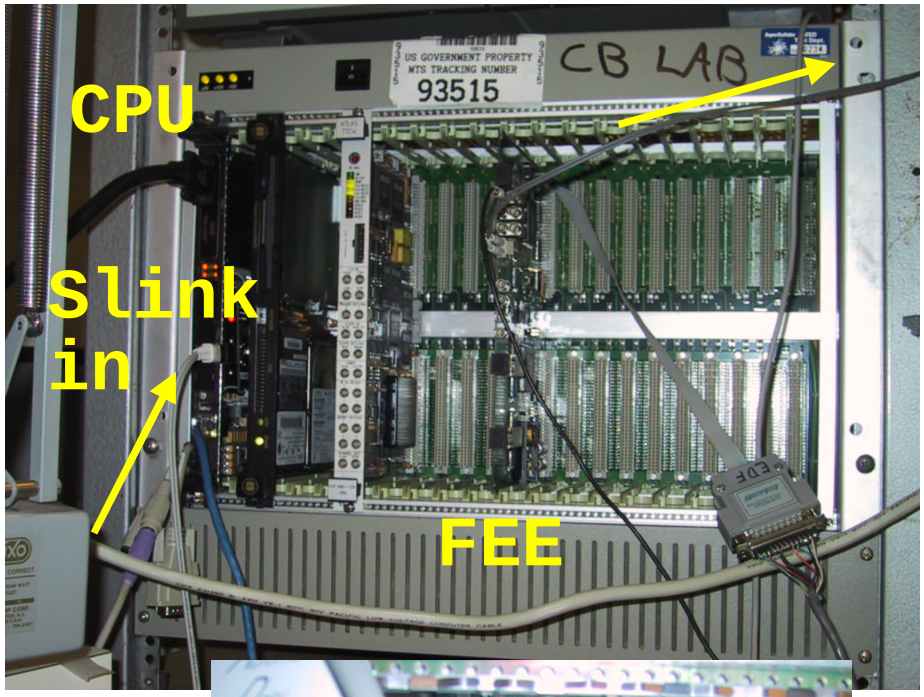
DAQ TDR & Baseline

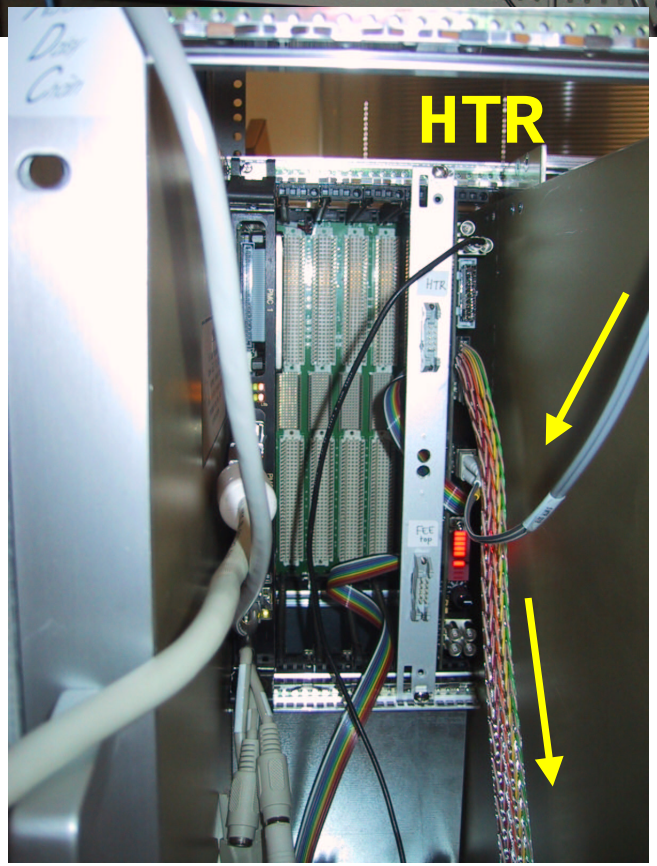
FED Builder & Multiuse kits

XDAQ

The pdf file of this talk is available at:
http://cmsdoc.cern.ch/~wsmith/TriDAS__report_0302.pdf
See also CMS Level 1 Trigger Home page at
http://cmsdoc.cern.ch/ftp/afscms/TRIDAS/html/level1.html

HCAL Demonstrator Setup at BU

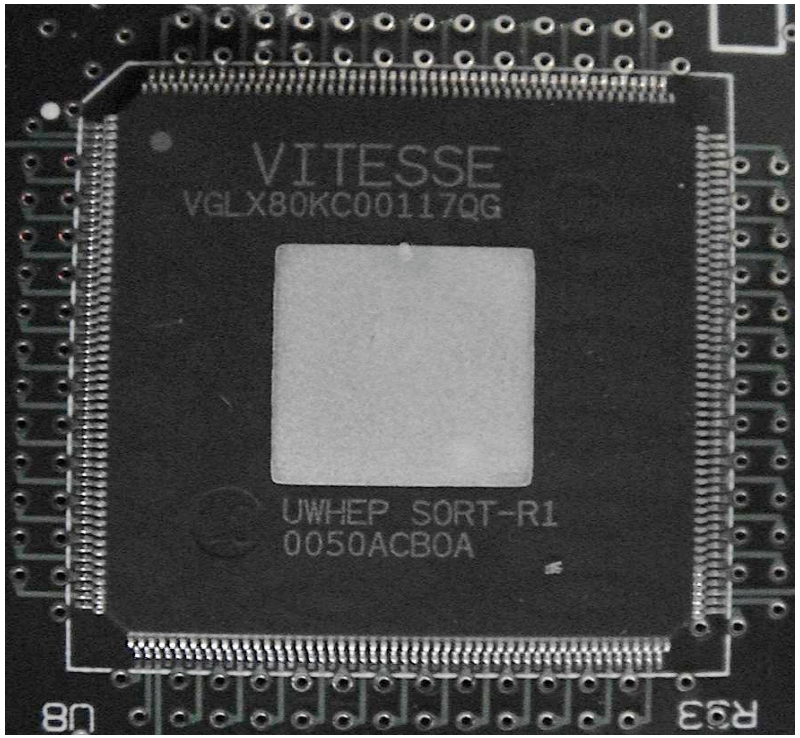


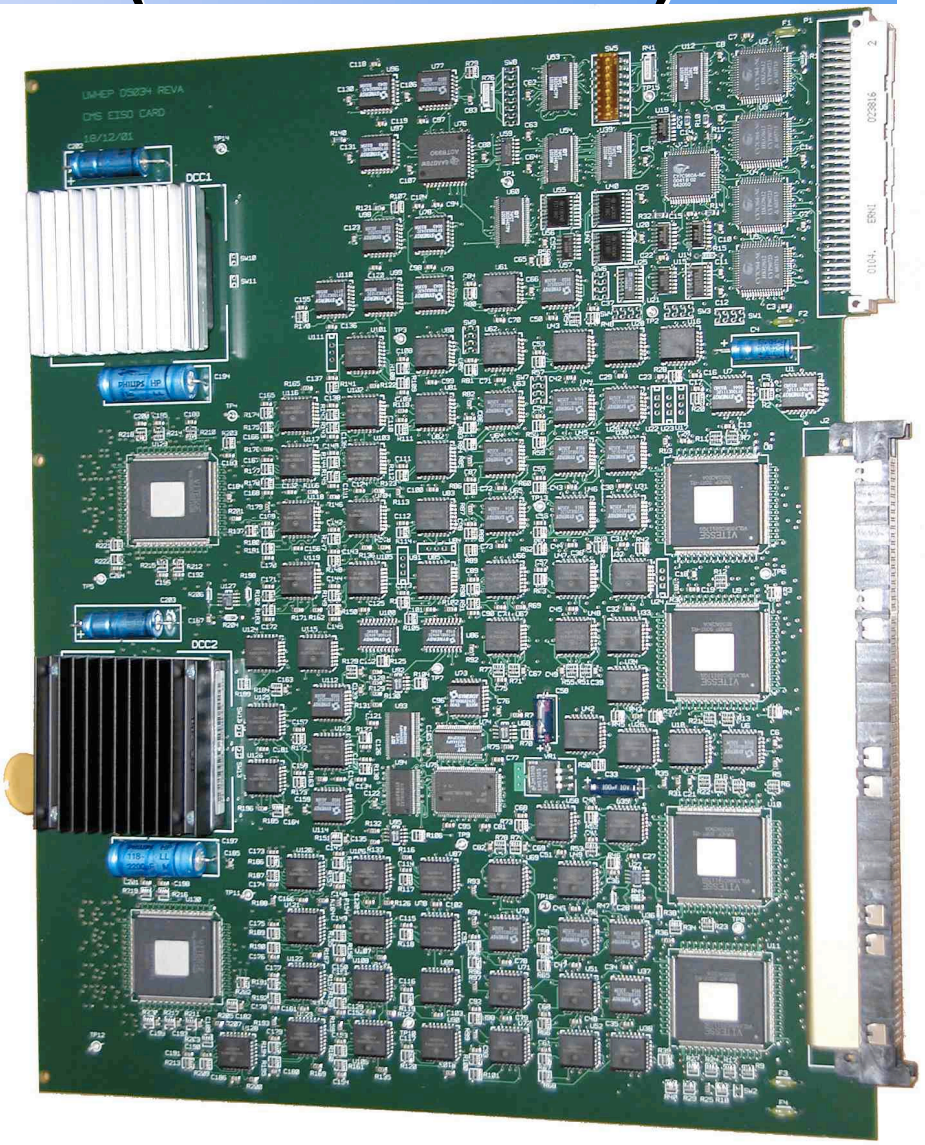


New Calorimeter Trigger Electron Isolation Card (U. Wisconsin)

Full featured final prototype board is finished & ready for testing.

Will test Electron ID ASICs & Sort ASICs :

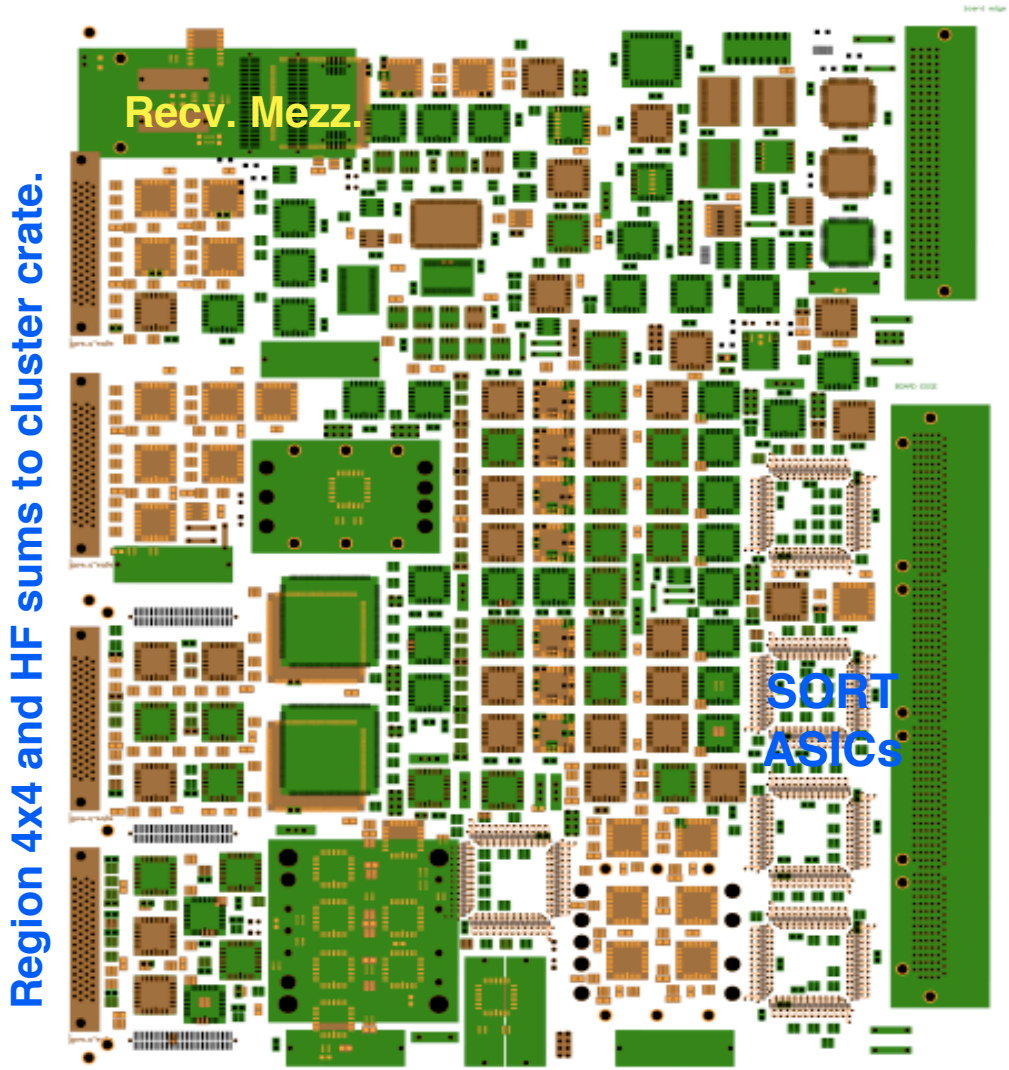




Jet-Summary Card

Jet Summary Card layout done

- **Electron/photon/muon info.**
  - SORT ASICs to find top four electron/photons
  - Threshold for muon bits
  - To GCT
- **Region energies**
  - To cluster crate
- **Absorbs HF functionality**
  - Reuses Receiver Mezzanine Card
  - To cluster crate

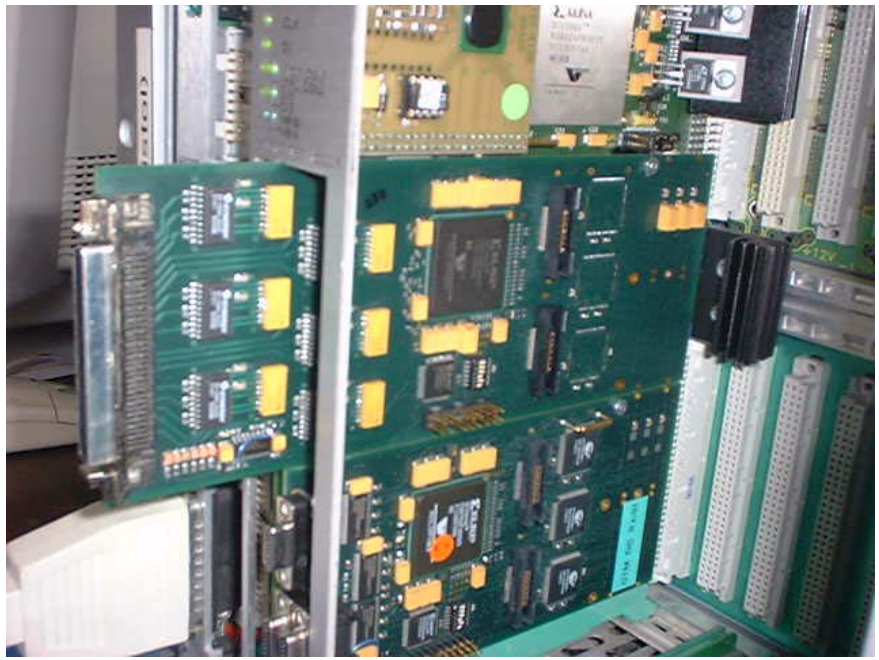


Global Cal. Trigger Slice

- " Cable backplane" will use:
  - Teradyne VHDM-HSD connectors.
  - Gore "eye-opener" cables or equivalent Molex product.

ECL daughter card

- Slice of an IM
  - SCSI II connector
  - Input synchronisation FPGA
    - Virtex E 400
- Now thoroughly tested



New Trigger "H_T"

Use all 12 jets: 4 each of central, τ, and forward

- all jets are mutually exclusive

After correcting the jet energies, sum up E_T's of all jets with energy greater than a certain threshold:

- $H_T = \Sigma E_{Tjet}$ E_{Tjet} > threshold energy

Advantages

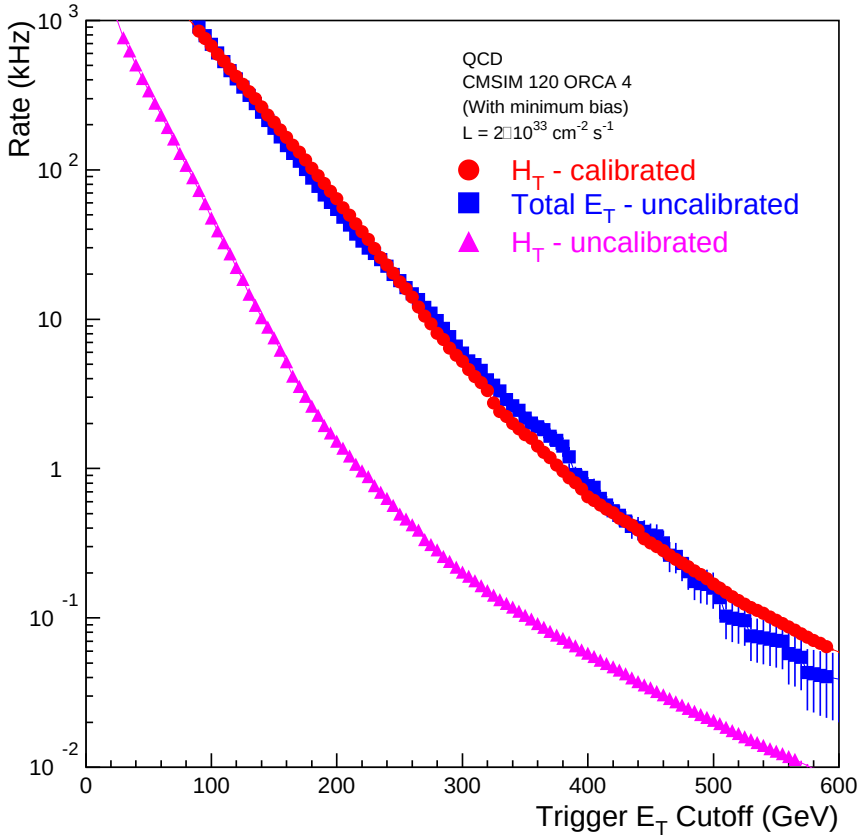
- Calibrated (jet energies are calibrated)
- Simple trigger for decays of heavy objects to multiple jets

New H_T Rate

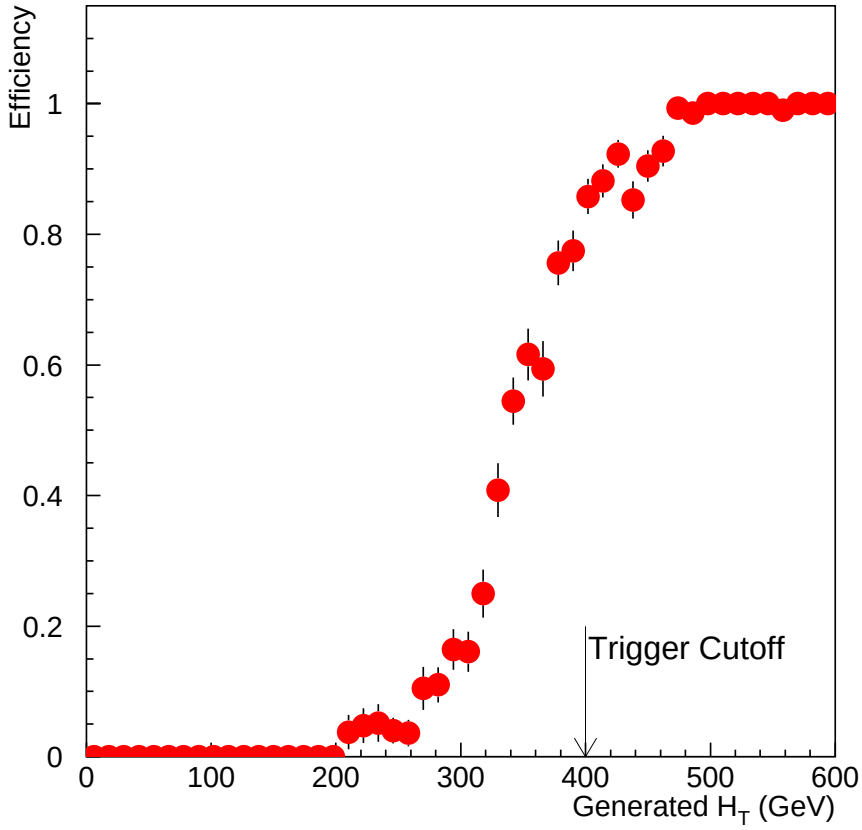
H_T=sum of all jet E_T's with E_T > some programmable threshold

- **E_T > 10 GeV for this result**

H_T trigger rate



jm_gg_h500_2tau_jj H_T Efficiency

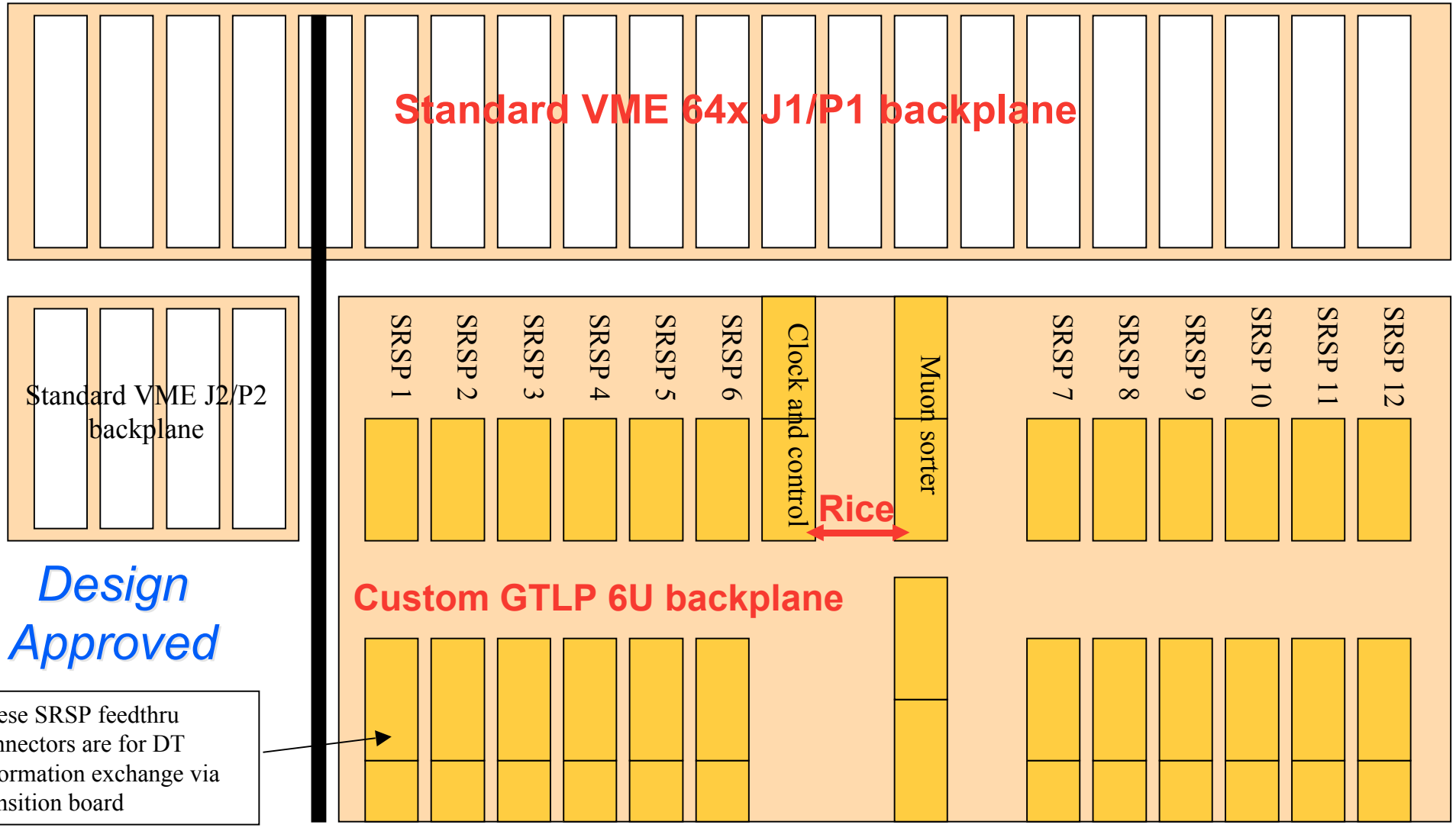


For a 400 GeV cutoff: Rate = 0.7 kHz and 95% eff = 470 GeV

Nice sharp turn on.

Uses data from FNAL for $\mathcal{L}=2\times10^{33}$

CSC Track Finder Backplane
(U. Florida)

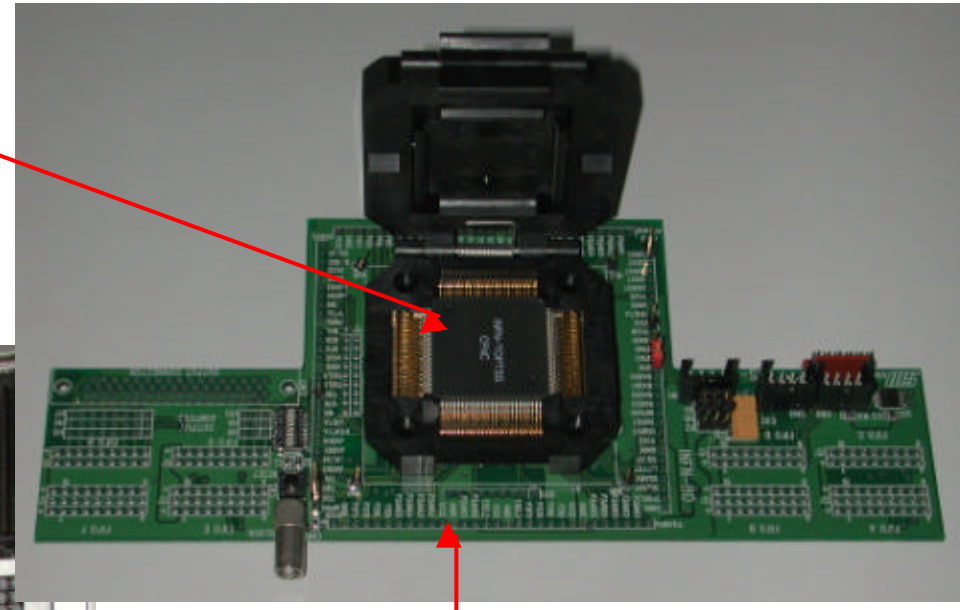


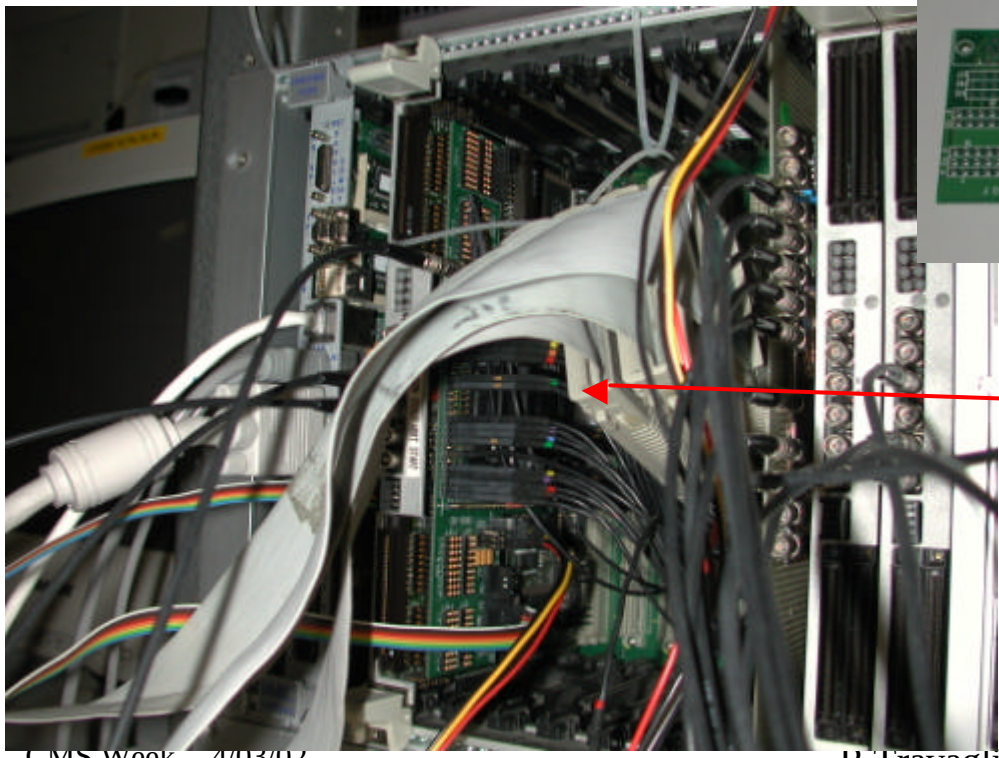
Design Approved

These SRSP feedthru connectors are for DT information exchange via transition board

TSS test system

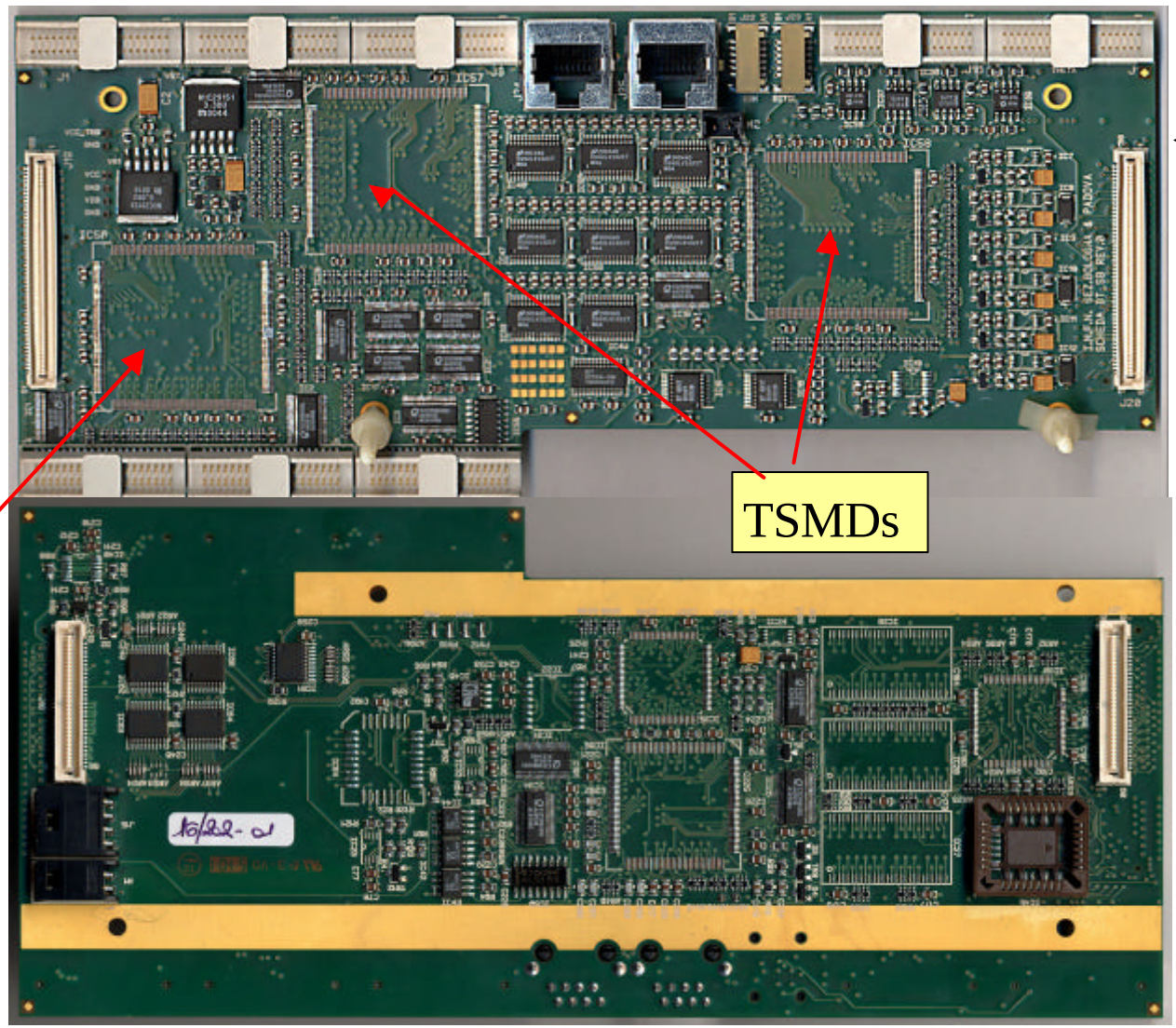
TSS Asic prototype
Alcatel 0.5 μm CMOS
Produced through Europractice





Piggy board mounted on a
Pattern unit emulating Traco input
And checking output

TSM and Server Board – New Prototype



PCB
16 layers !

TSM
side

Reminder:
TSM has
implemented
With 3 pASIC
Actel A54SX32
0.35 µm CMOS

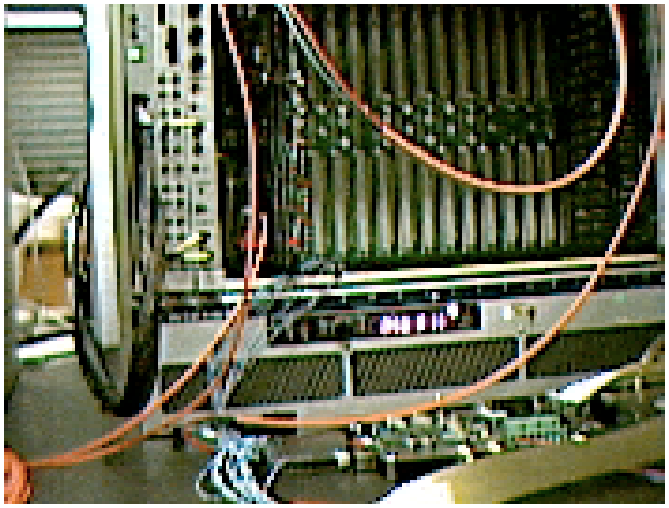
Chamber
Controller
side

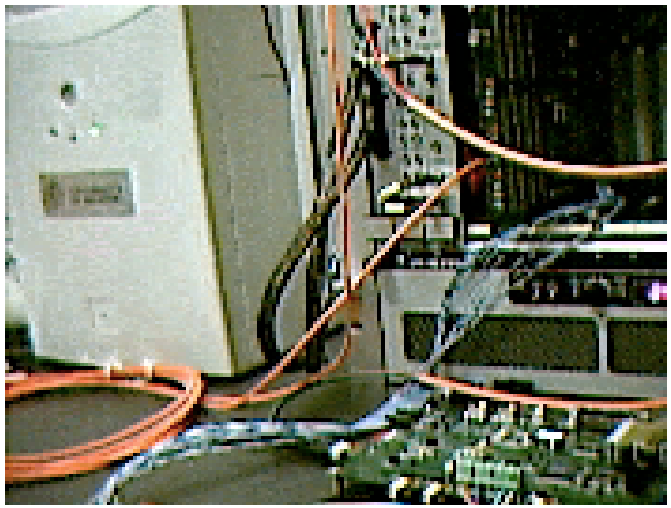
Drift Tube Muon Track Finder (Vienna)

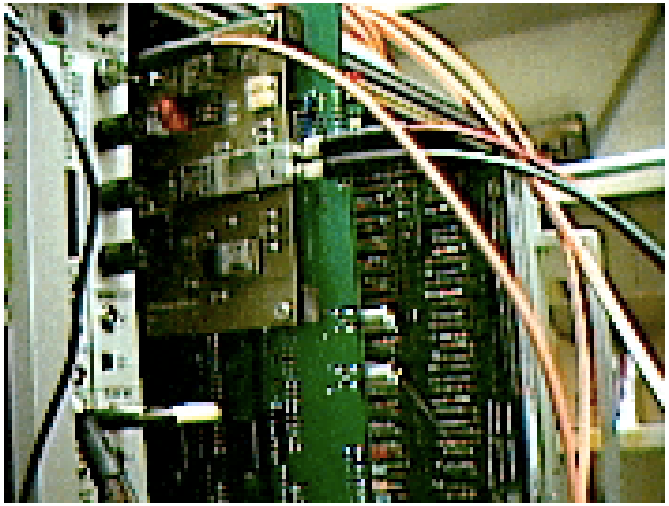
Status:

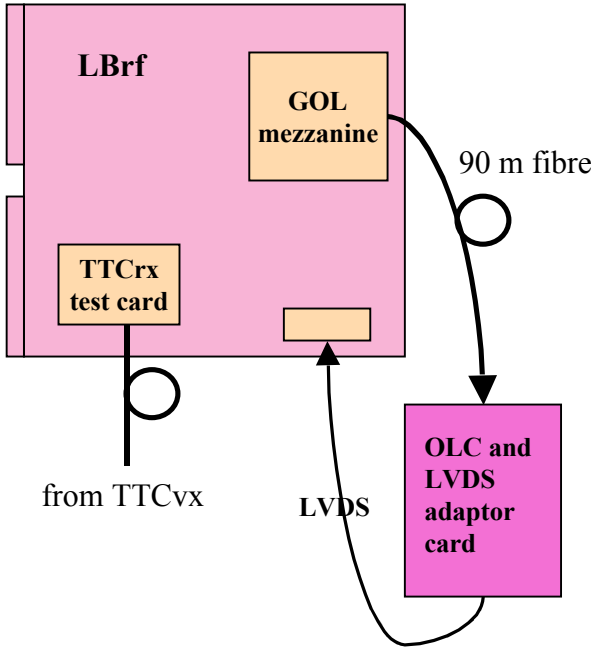
- **Drift Tube Track Finder Board**
  - VHDL Behavioral & Synthesis Models simulated, tested
  - Board schematic design finished, board layout design in progress
- **Backplane**
  - Layout ready, checked, prepared for board production
- **Input Receiver**
  - bit allocation for ETTF revision during this CMS week
- **Test Input Board**
  - board ready, soldering in progress
- **Eta Track Finder**
  - VHDL model extended, testbench defined
  - LUTs generated in H/W format (used also by VHDL)

RPC Optical Link Test Setup
(Helsinki & Warsaw)



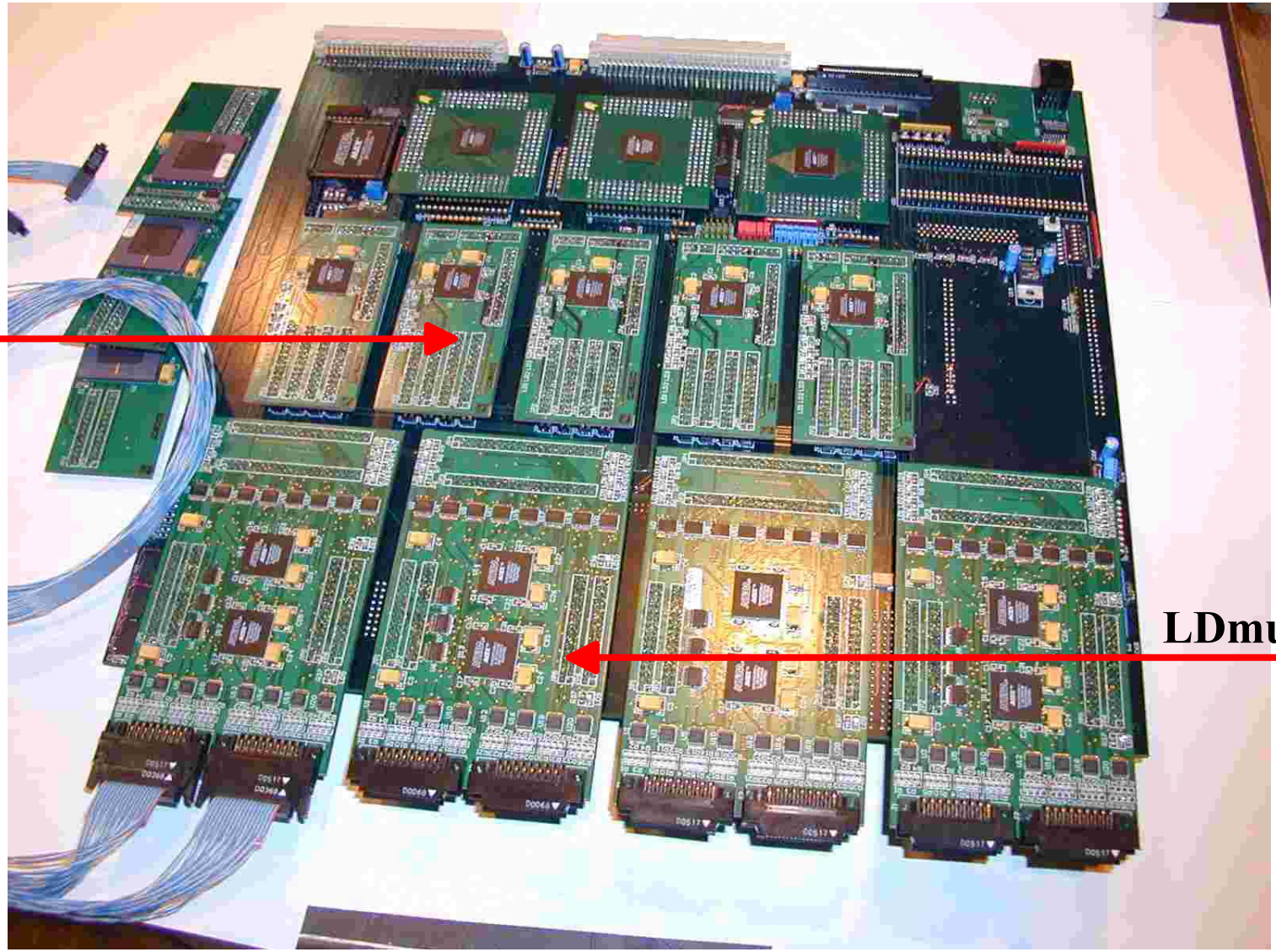






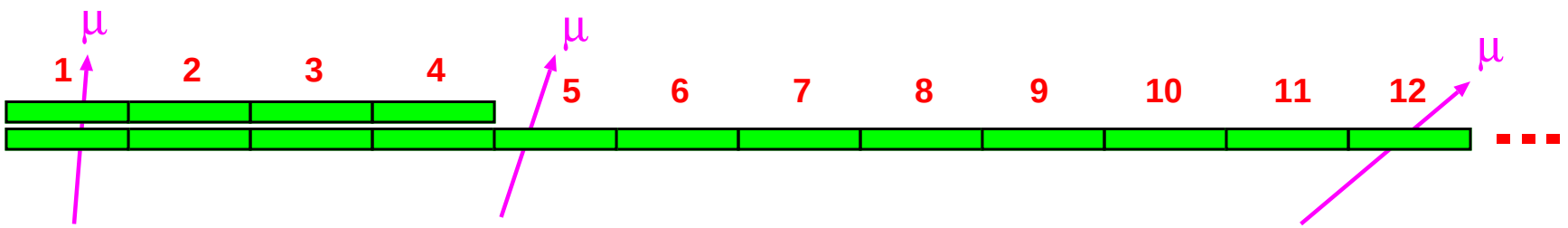
PC-controlled VME crate with SBS VME-PCI interface, TTCvi, TTCvx and LBrf. Data are looped back to the LBrf via OLC, which is acting as the receiver for the fibre optic link. On LBrf and OLC we can choose between an on-board oscillator, clk from TTCrx or other external clk

All hardware is ready, as is most of the software for the PC and VHDL for Alteras. Initial tests have showed no problems, more detailed tests will be done in Warsaw on 17th-27th March.


PAC's
LDmux Boards

MUONS IN HO : CALCULATIONAL DETAILS

CMSIM 121 + ORCA_5_3_1



Updated HCAL readout simulation

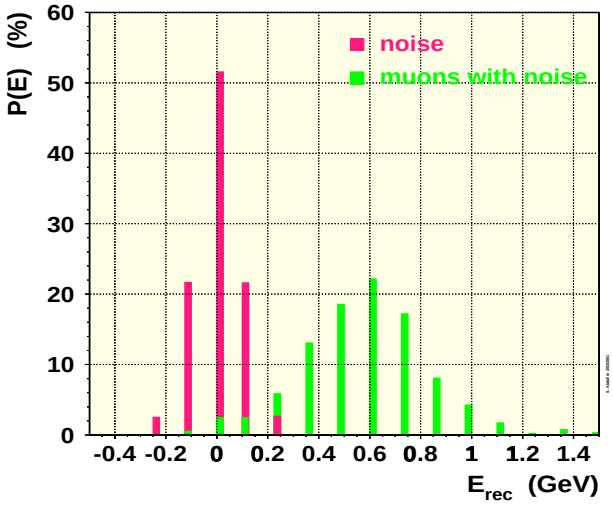
- Noise sigma per time bucket : 1.5 pe
- Singal collection in 2 time buckets (~ 90 %)
- ADC count : 3 pe, baseline position - 2d AC bin
- Muon signal : ~ 8 pe / scintillator -> 0.25 MeV / pe

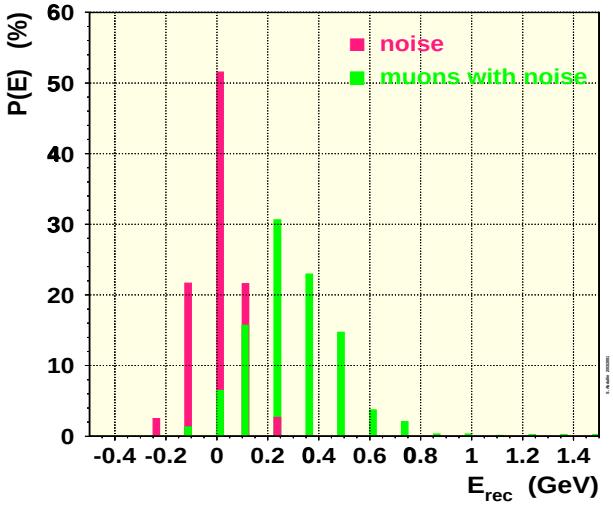
20 GEV MUONS VS NOISE

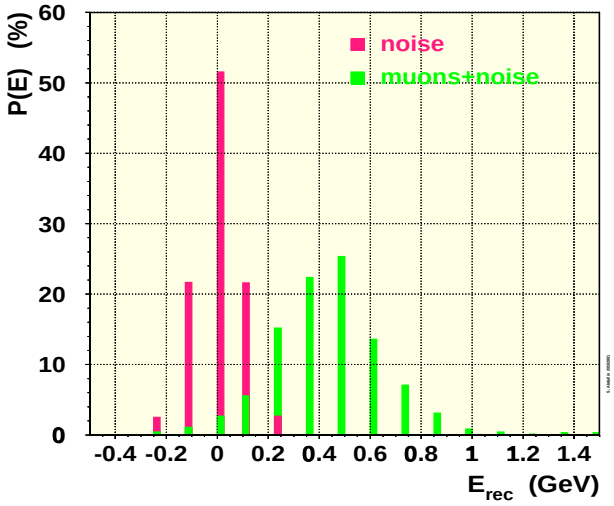
HO central ring (tower 1) : two scintillator layers

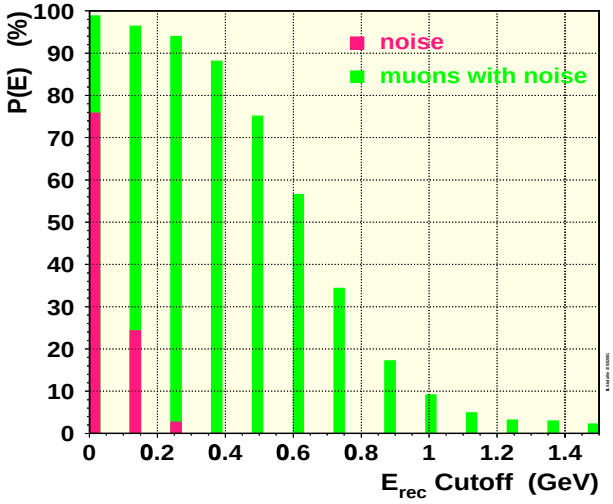
HO first ring (tower 5) : one scintillator layer

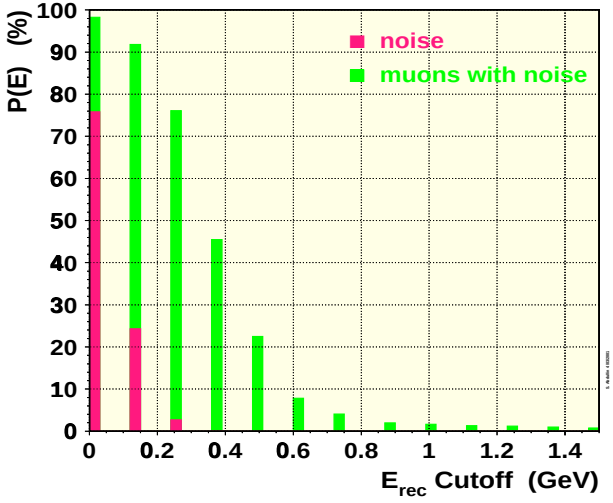
HO second ring (tower 12) : one scintillator layer

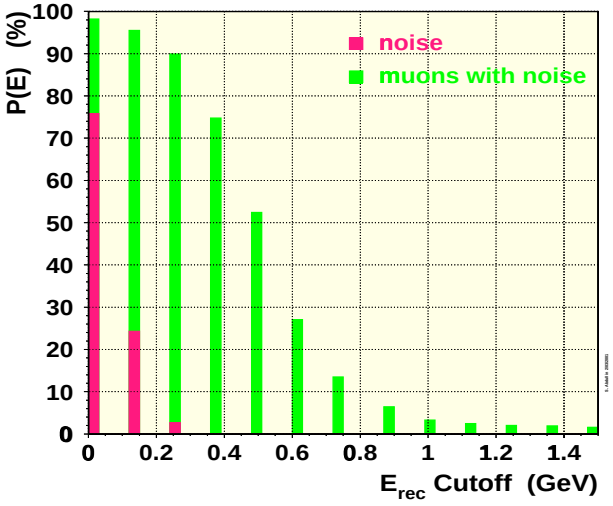












HO in the Muon Trigger

Additional Plane in RPC Trigger - J.F. Troconiz/Madrid

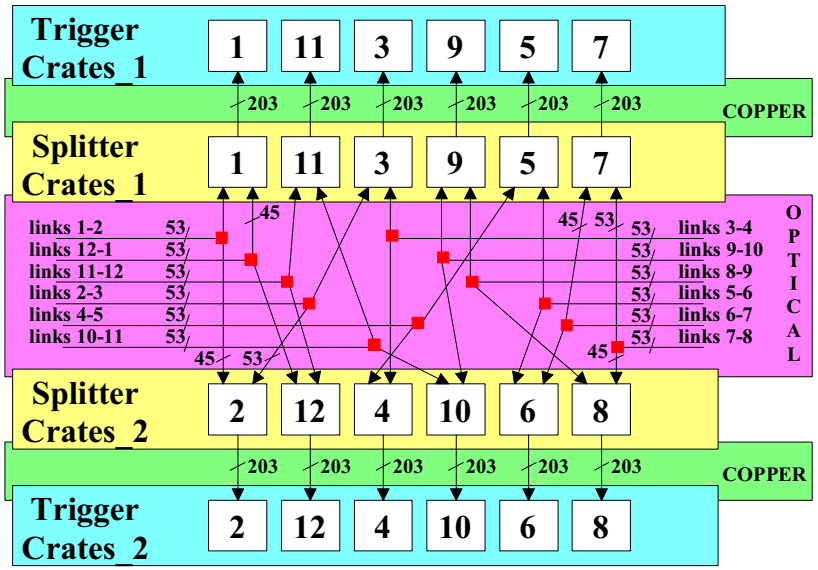
- Preliminary results
- Geometrical acceptance 93% correlated w/RPC
- HCAL group working on improvement of HO performance

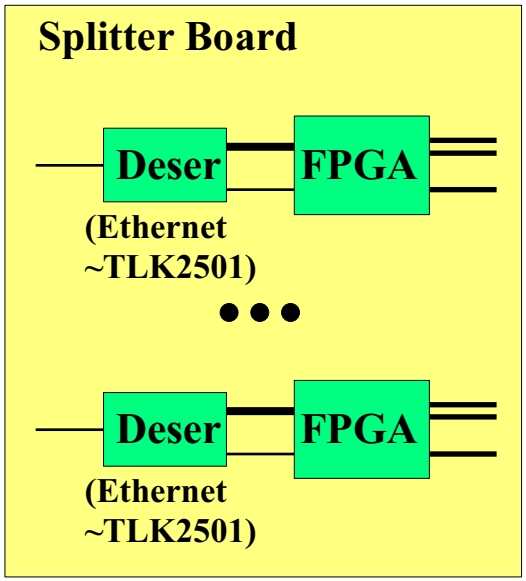
	Area (cm^2)	kHz	Hz/cm^2	Eff (%)
RPC oiled	250	1.2	5	95-98
RPC non-oiled	250	12	50	95-98
HO (7pe) >380 MeV	2000	56	28	64
HO (10pe)>200 MeV	2000	240	120	93
HO (10pe)>265 MeV	2000	56	28	88
HO (10pe)>300 MeV	2000	0.92	0.46	80

RPC trigger towers are different and the data need to be regrouped before they enter Trigger Boards. They are only 15 towers in the barrel, so if the data are regrouped before the links one needs only 3 x 12 = 36 links for the whole detector, assuming 1 link for 5 towers x 6 tiles (30 degree).

Detailed remaping table can be prepared (eta_min, eta_max for each HO tower (or Z_min, Z_max and R for each tile) are needed.

Splitter Crate can be used to make optics/electrics conversiom and data regroupping



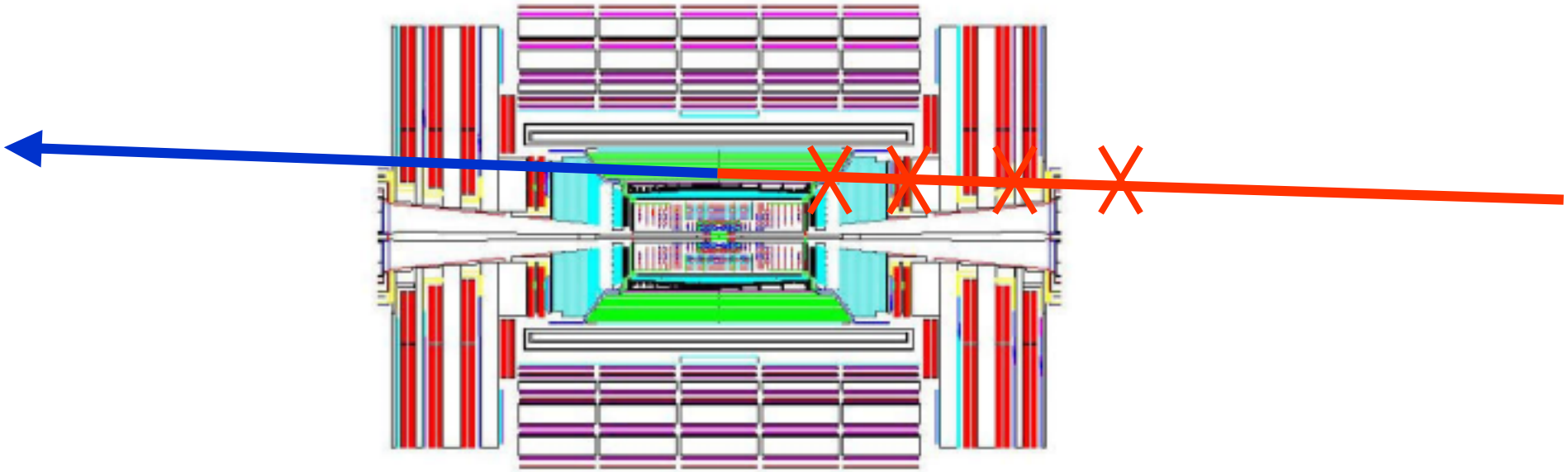


one additional Splitter Board needed

Beam Halo Muon Trigger

➢ The situation

- ⇨ halo muons are seen by CSC, only (flag indicates halo muon)
- ⇨ 4 bunch crossings delay between the two endcaps
- ⇨ read-out will only work correctly in one half of the detector, where halo muon is moving away from interaction point
- ⇨ do we need matching between the endcaps for alignment?

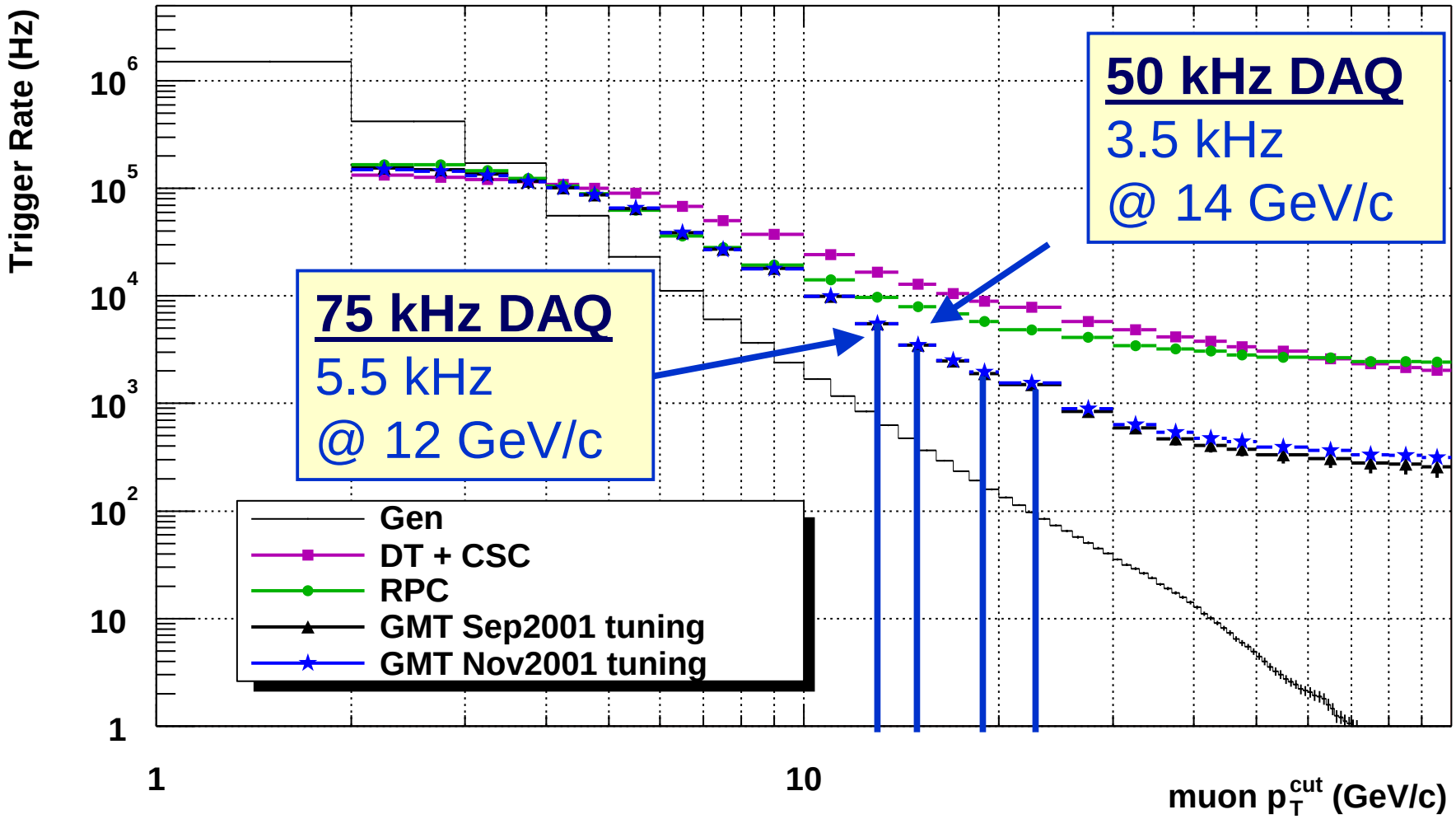


L1 single muon trigger rates

samples: pt1, pt4, pt10, W, Z

whole detector: 0 < |η|< 2.5

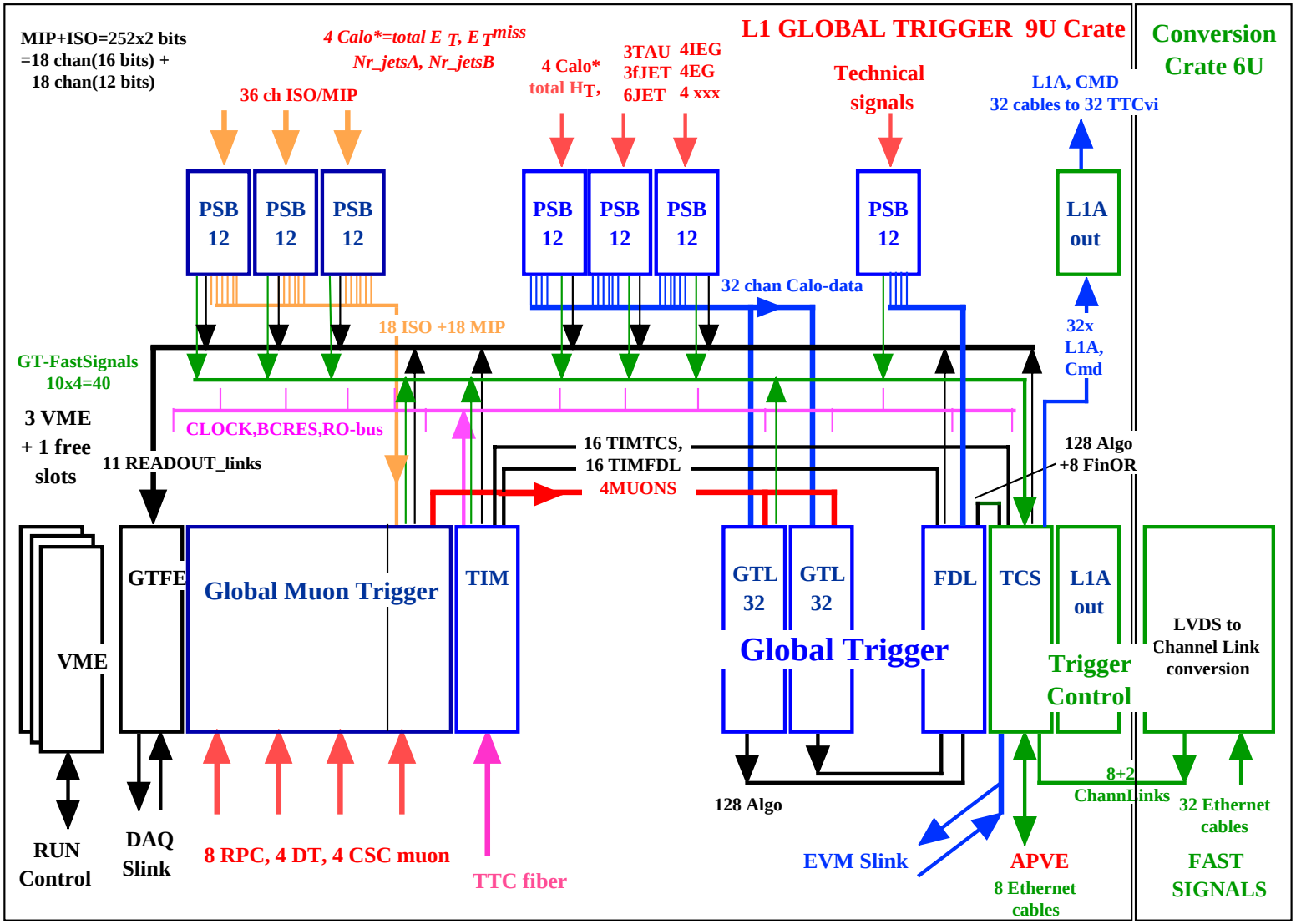
L=2x10^{33} cm^{-2} s^{-1}



Alternative Global Trigger Crate

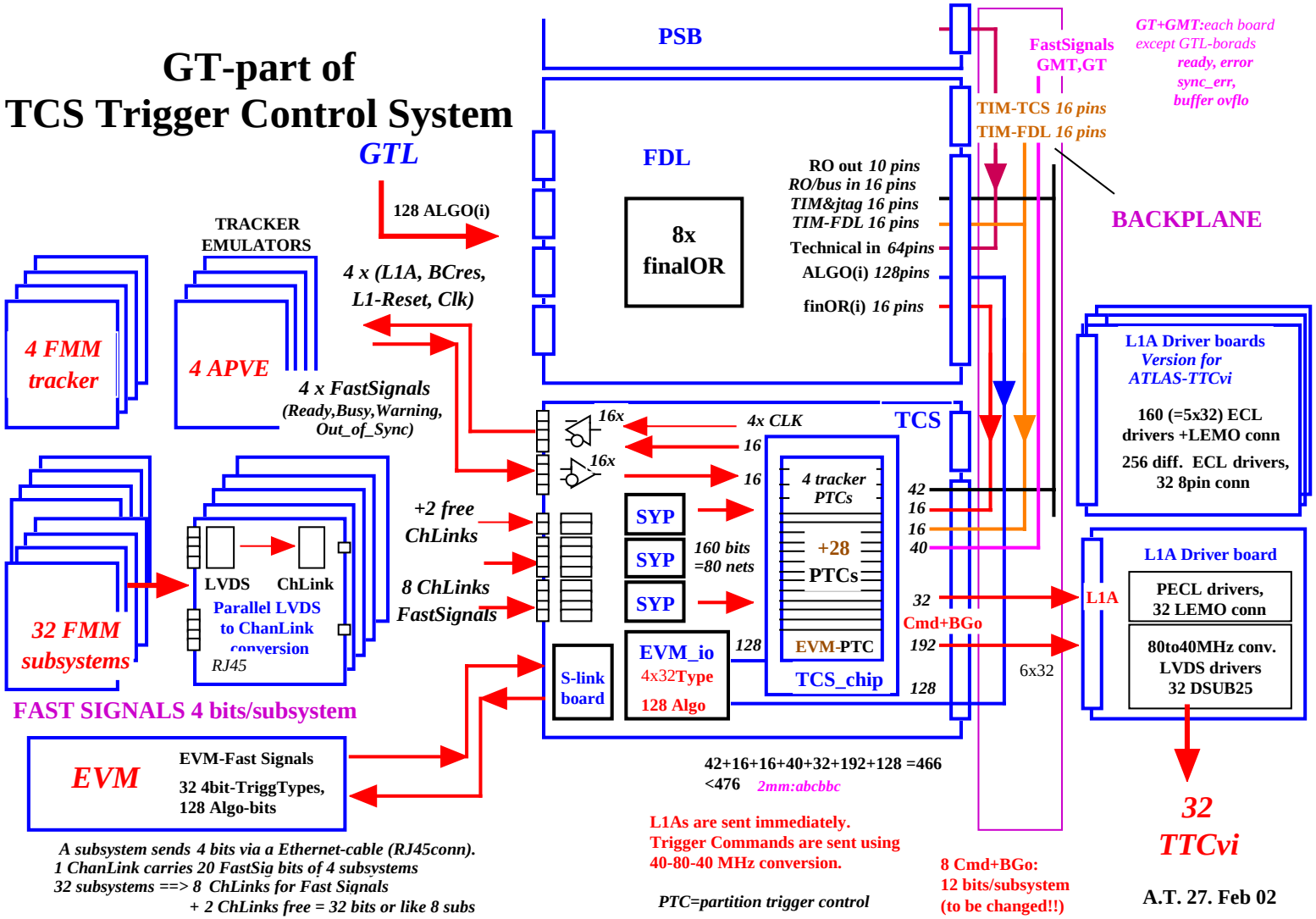
6U prototype exists

9U backplane: MS 10/02



A.T. 27.Feb 02

Global Trigger FDL and TCS board with connections



Trigger Software Working Group

Distributed Model of Software Development

- **XDAQ**
  - configuration, communication and database access
- **PVSS II**
  - commercial toolkit used by Detector Controls System
- **PCI-VME**
  - Studying various hardware & software options
- **Libraries**
  - Adaptive Communications Environment library
  - Hardware Access Library
- **Reviewing test beam & lab experiences**

LHC-Machine Interface

Questions to CMS

- **Beam information CMS can provide to machine**
  - Position: Tracking vertex, HF energy balance
  - Radiation levels in sensitive components
- **How often would CMS adjust timing**

  Adjustment to center crossing clock at begin run
- **Readout of LHC Beam Pickups for CMS**
  - RF pickups 70 m from the IP
  - Readout in 4 quadrants for measuring beam position
  - What signals does CMS want (summed?)
- **Replies due at the next meeting of the Ad-Hoc Working Group on LHC Machine Parameter and Signal Exchange on March 26. (Comments to W. Smith)**

March 2002. DAQ Summary

DAQ TDR

- Draft in preparation for the April CPT week
- Myrinet-GEthernet baseline design

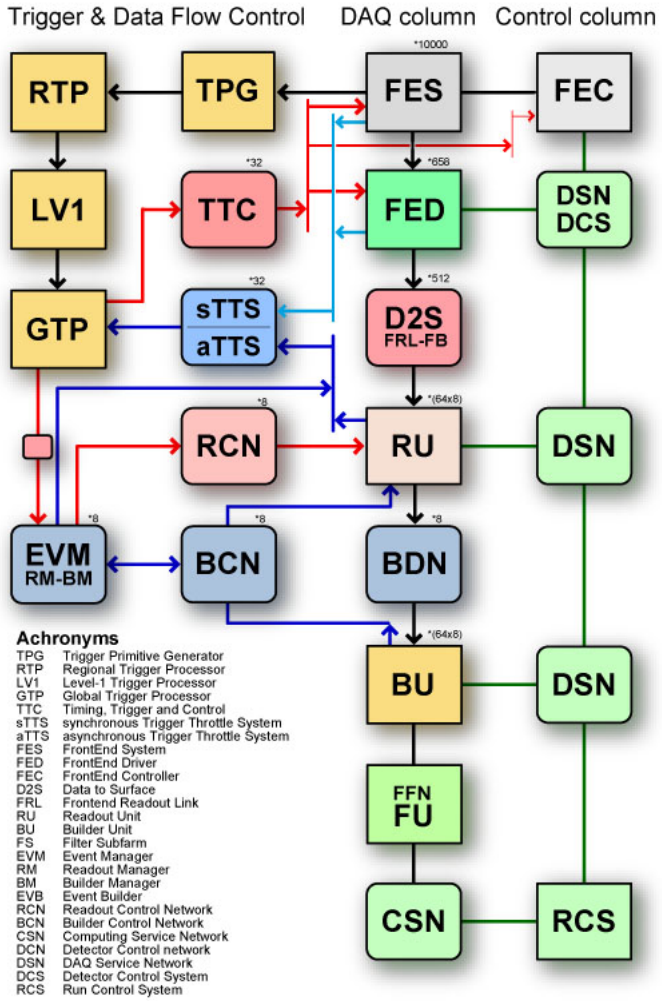
Readout prototypes and applications

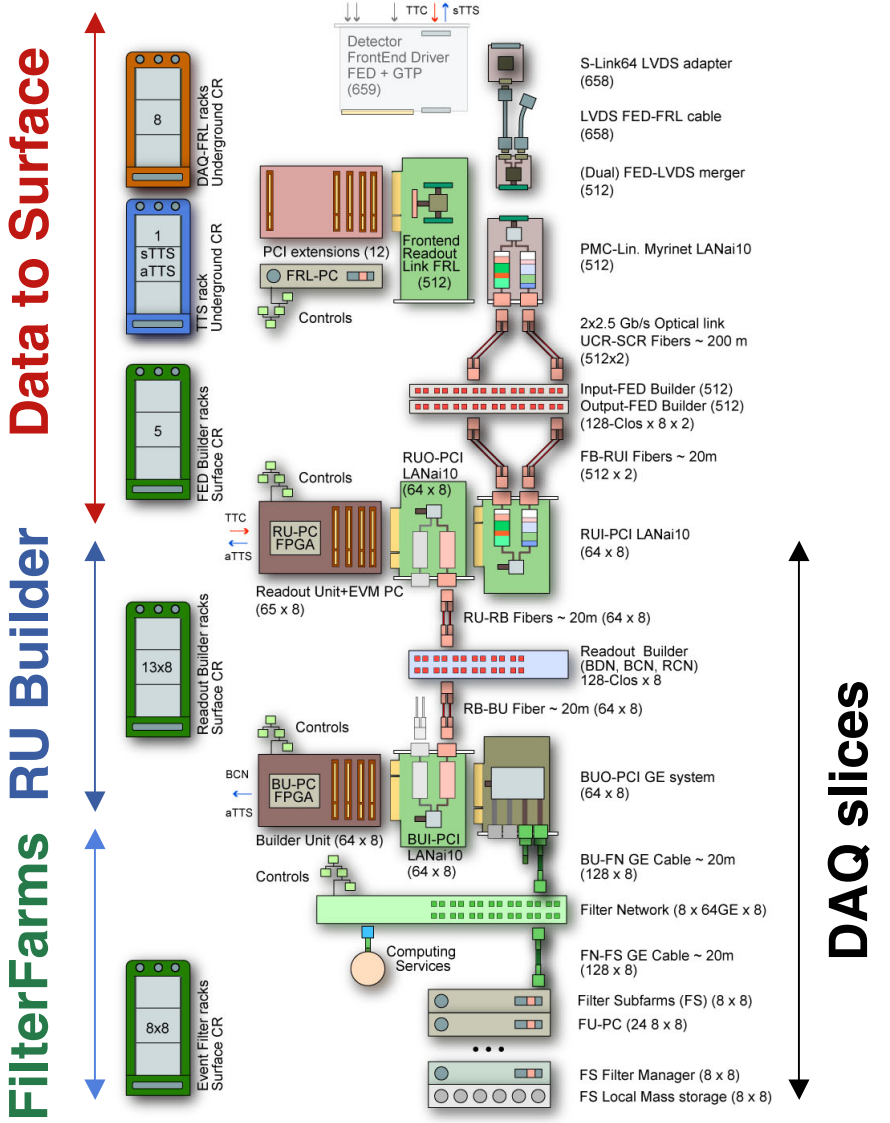
- First FED Builder test bench results
- FED readout hardware/software kit ready
- On-line software framework XDAQ last release
- DAQ column progress
- Run control prototype

New design

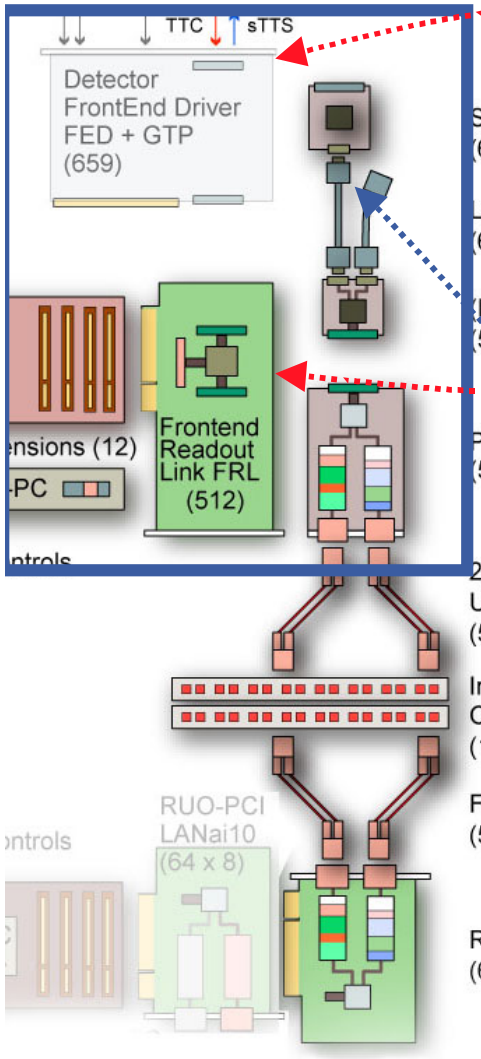
- Costs evaluation and expenditures profile

TDR baseline layout (MY-GE)





GIII FED-Slink-RUI multi use kit



S-Link64 LVDS adapter (658)

LVDS FED-FRL cable (658)

(Dual) FED-LVDS merger (512)

PMC-Lin. Myrinet LANai10 (512)

2x2.5 Gb/s Optical link UCR-SCR Fibers ~ 200 m (512x2)

Input-FED Builder (512)
Output-FED Builder (512)
(128-Clos x 8 x 2)

FB-RUI Fibers ~ 20m (512 x 2)

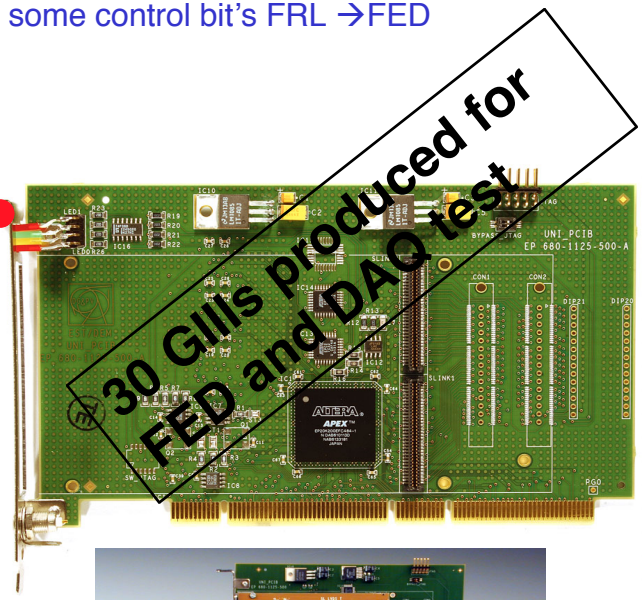
RUI-PCI LANai10 (64 x 8)

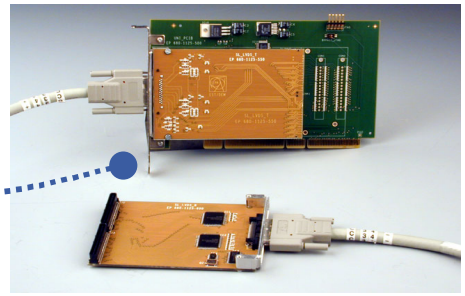
LVDS link is a unidirectional data link
transmission (64-bit@60MHz) FED →FRL (+some control bit's)
back pressure + some control bit's FRL →FED

Generic III as FED emulator

Generic III as FRL prototype

S-Link64 FED merger





Results:

- 10^{15} bit transfer without error (on 2 meters length cable) 64b-100MHz
-Transfer on 7.5m cable length 64b-100MHz
-Transfer on 17 m (3 cables coupling) cable length 64b-60MHz
- Pending 20 m cable length 64b-60MHz

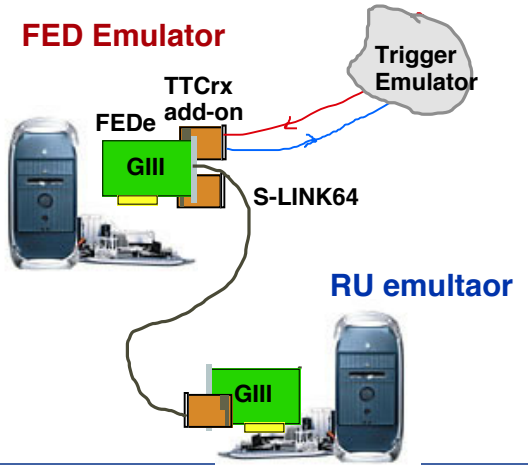
GIII FED kit basic software

FEDKIT Performance

- Performance tested on Supermicro 370DLE, PC133 SDRAM, PIII 733MHz,
- Bandwidth over the bus measured at 500MB/s
- Overhead per event : 579ns
- Additional overhead per block (4k blocks) :182ns
- Average poll time (software) at 2kB : 200ns
- Tested up to 512kB event fragment
- Global throughput at 2kB fragment : 448 MB/s
- Global throughput for 512kB fragment : 480 MB/s

DAQ-Tracker meeting
29th january 2002

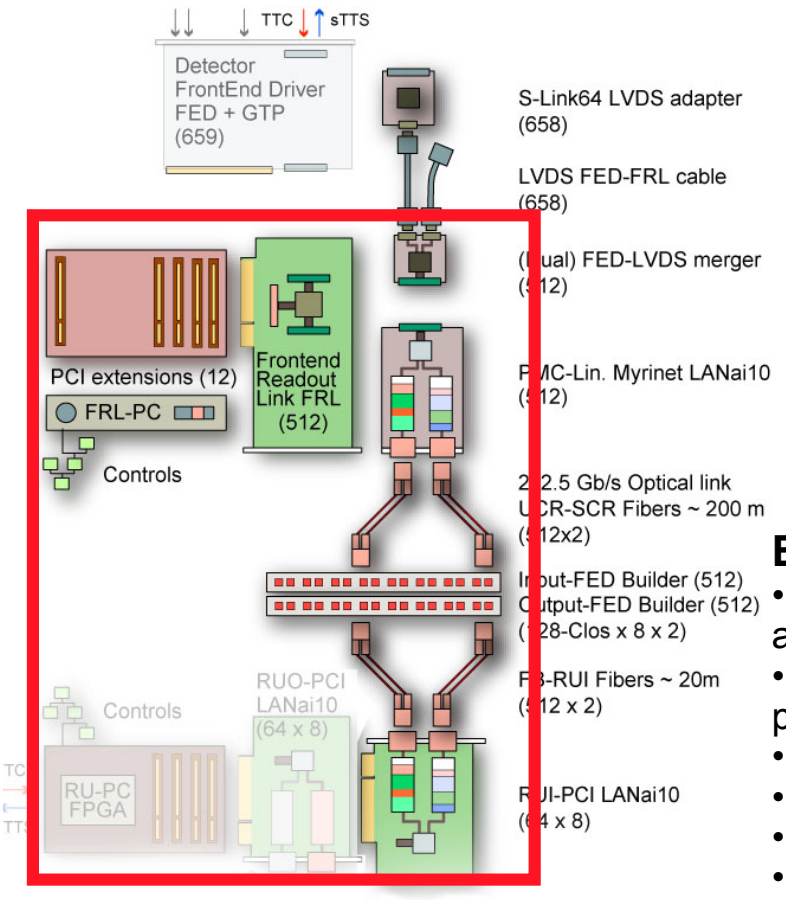
Eric CANO, CERN/EP-CMD

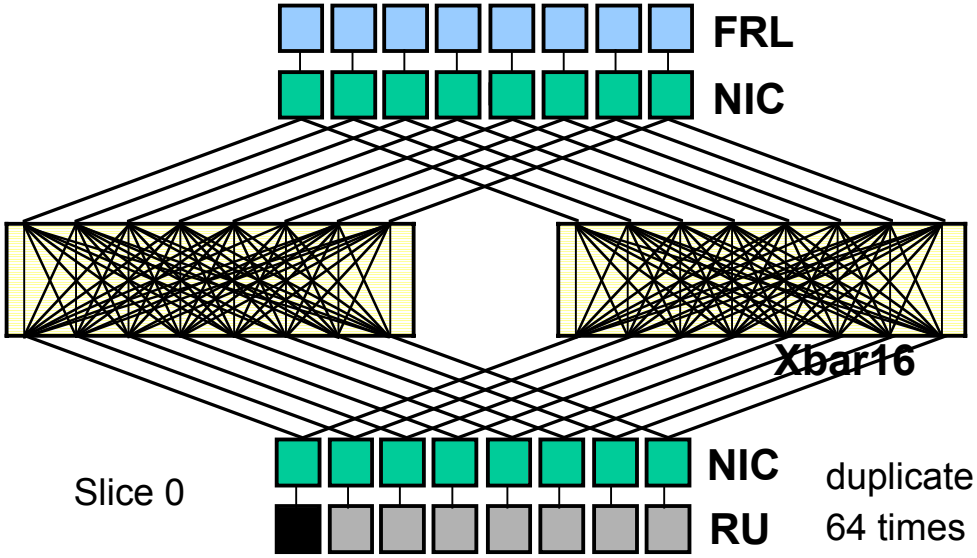


FEDKIT Software status

- Software tested with generator mode
- Software integrated in Xdaq, runs for days with no problem
- Features additions in progress (additional robustness)
- API designed to be minimal, and simple to use
- Documentation for both software and hardware at http://cern.ch/cano/fedkit

FED builder based on Myrinet

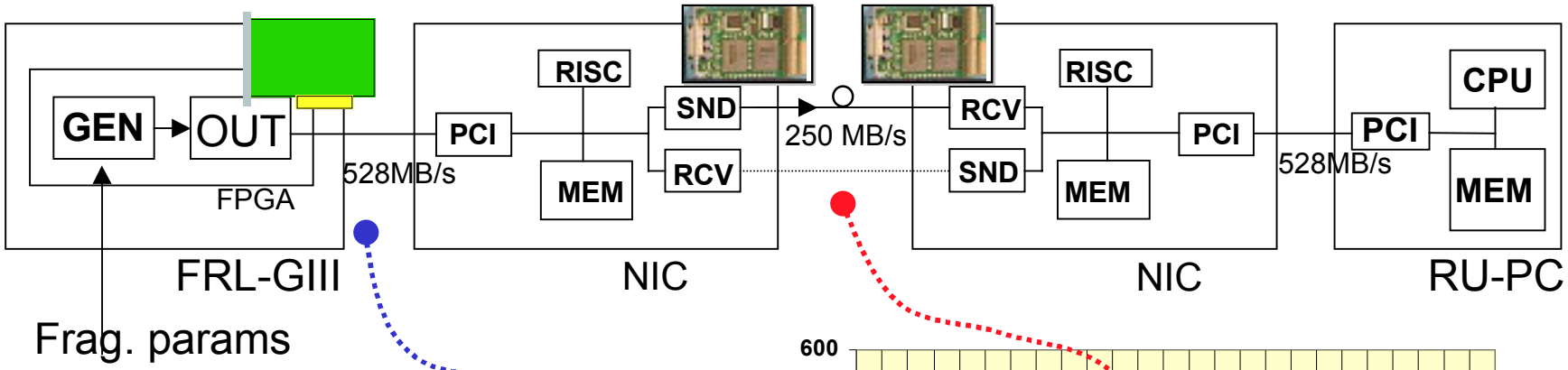




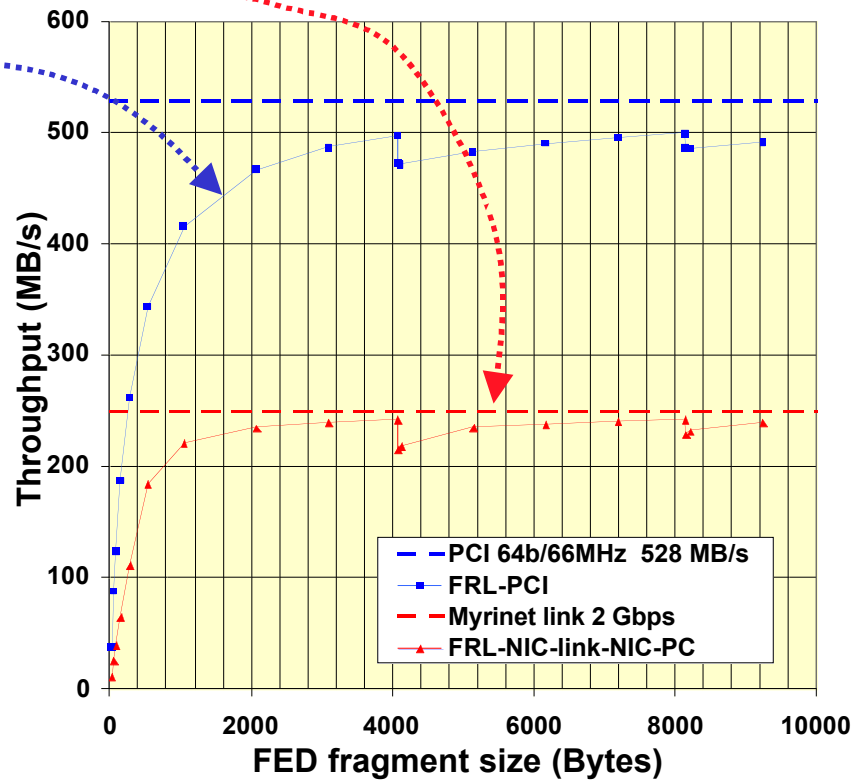
Basic idea:

- destination = trigno%8 ; (via Xbar 0 or Xbar 1 according to availability)
- NICs on FRL (FED Readout Link) and RU input have 2 Myrinet ports
- each port goes to separate Xbar16 (8x8) [“two-rail network”]
- no traffic shaping
- data throughput 2x2Gbps maximum per FRL
- typical **throughput 50% due to HOL blocking, so 250 MB/s sustained per FRL**
- useful to **balance inputs if FRL data rates not uniform**
- NIC at FRL side buffer of 1.5 MByte (derandomiser and buffer before switch)
- NIC at RU side performs event building

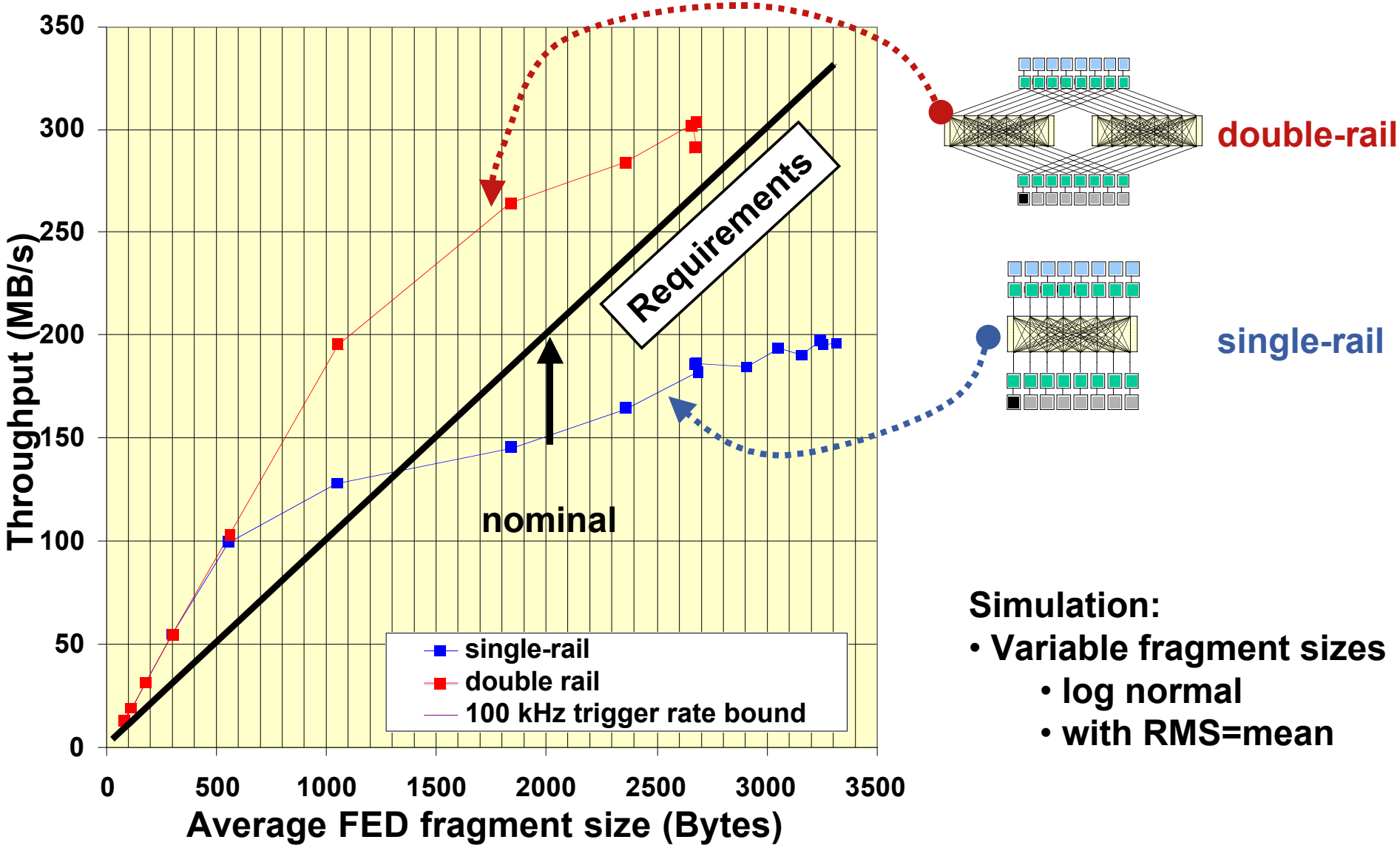
FED builder prototype setup



- sawtooth due to page size
- PCI close to wire speed
- Myrinet close to wire speed
- for 2 kByte:
  - througput 230 MB/s
  - or 115 kHz trigger rate



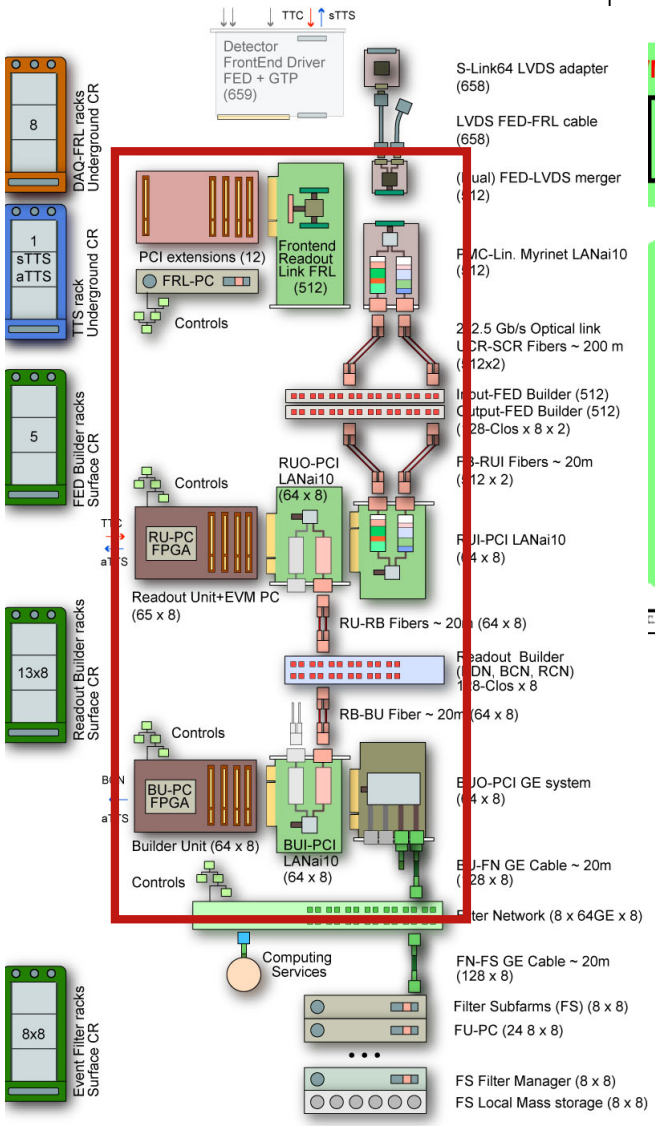
FED builder EVB performance - Simulation

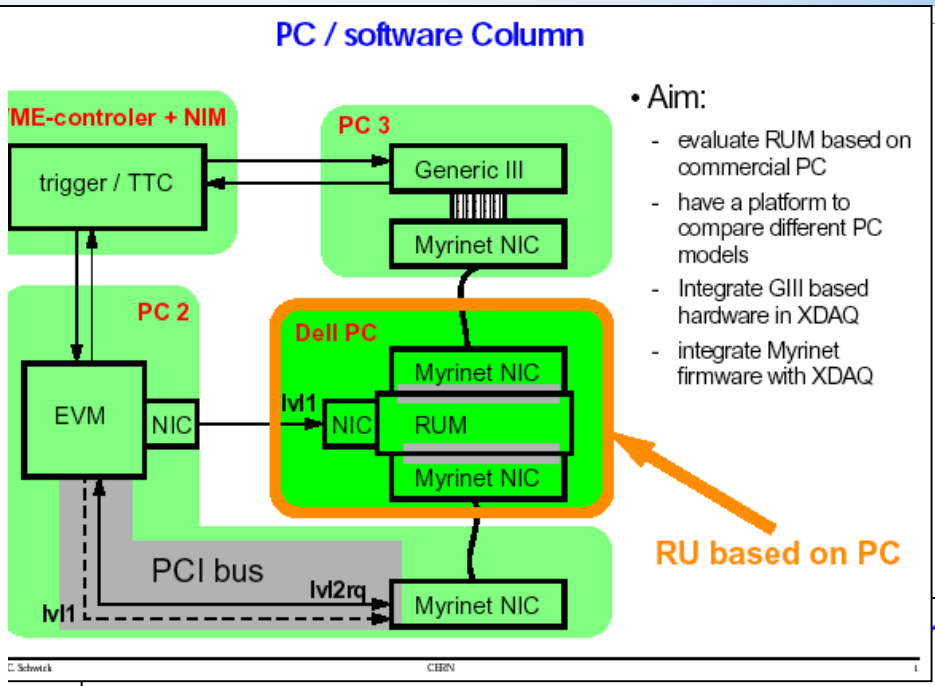


Simulation:

- Variable fragment sizes
  - log normal
  - with RMS=mean

DAQ column





- Hardware
  - Everything which is needed exists :
    - 3 PCs
    - TTC system with TTCvi, TTCrx, TTCex, and NIM logic for trigger generation (might be substituted with GIII)
  - Myrinet links
- Software
  - Myrinet firmware at RU - Input exists
  - XDAQ applications, Myrinet firmware RU-output, control software and monitor (measurer software have to be written.
- AIM: have measurements available for TDR (august / september)

XDAQ Release

- V1.0 baseline release
  - Source and binaries for **Linux, VxWorks**
  - Graphically assisted installation
  - All modules, applications and framework extensions are now dynamically loadable
    - smaller and more stable XDAQ core
    - XDAQ framework can now be better tailored to various application domains
  - Graphical control client for Java
  - **Hardware access library**
    - for NI and SBS VME/PCI interfaces
    - Local VME and PCI access
  - **G-III SLINK-64 readout library**
- **Download** from http://cern.ch/xdaq
- **Documentation**
  - Chapter: Getting started (install, compile, HelloWorld example)
  - I2O messaging
  - SOAP messaging
- XDAQ enters production state
  - Future versions will contain extensions, core API shall remain stable

TriDAS organization

Trigger and Data Acquisition Project