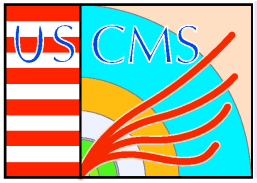


US CMS TriDAS Report

US CMS Collaboration Meeting

Wesley H. Smith, *U. Wisconsin*
CMS Trigger Project Manager

April 25, 2003

Outline:

Calorimeter Trigger

Endcap Muon Trigger

DAQ

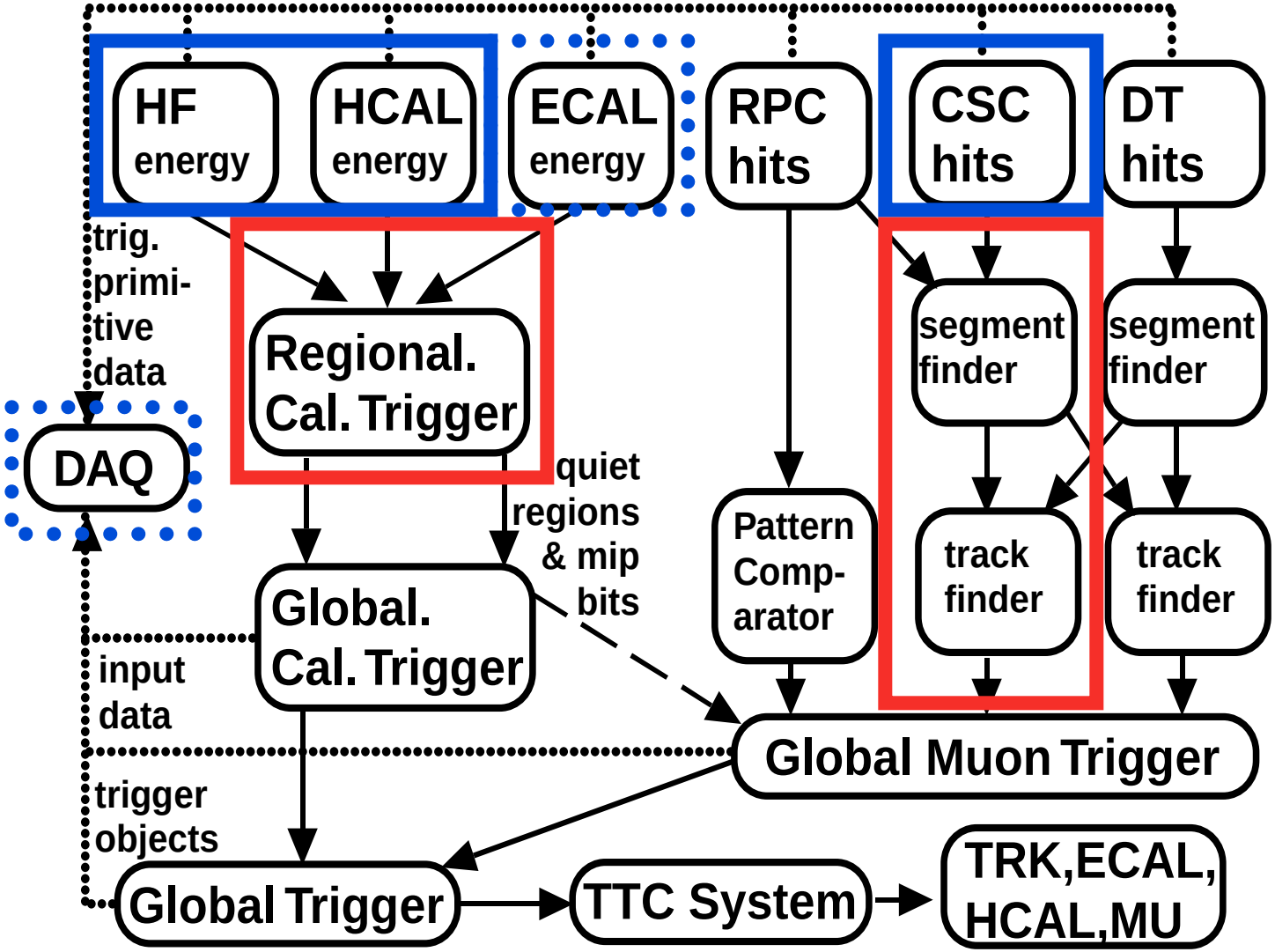
This talk is available on:

http://hep.wisc.edu/wsmith/cms/USCMSTriDAS_0403.pdf

L1 Trigger Hardware Overview

US CMS Trigger (this talk)

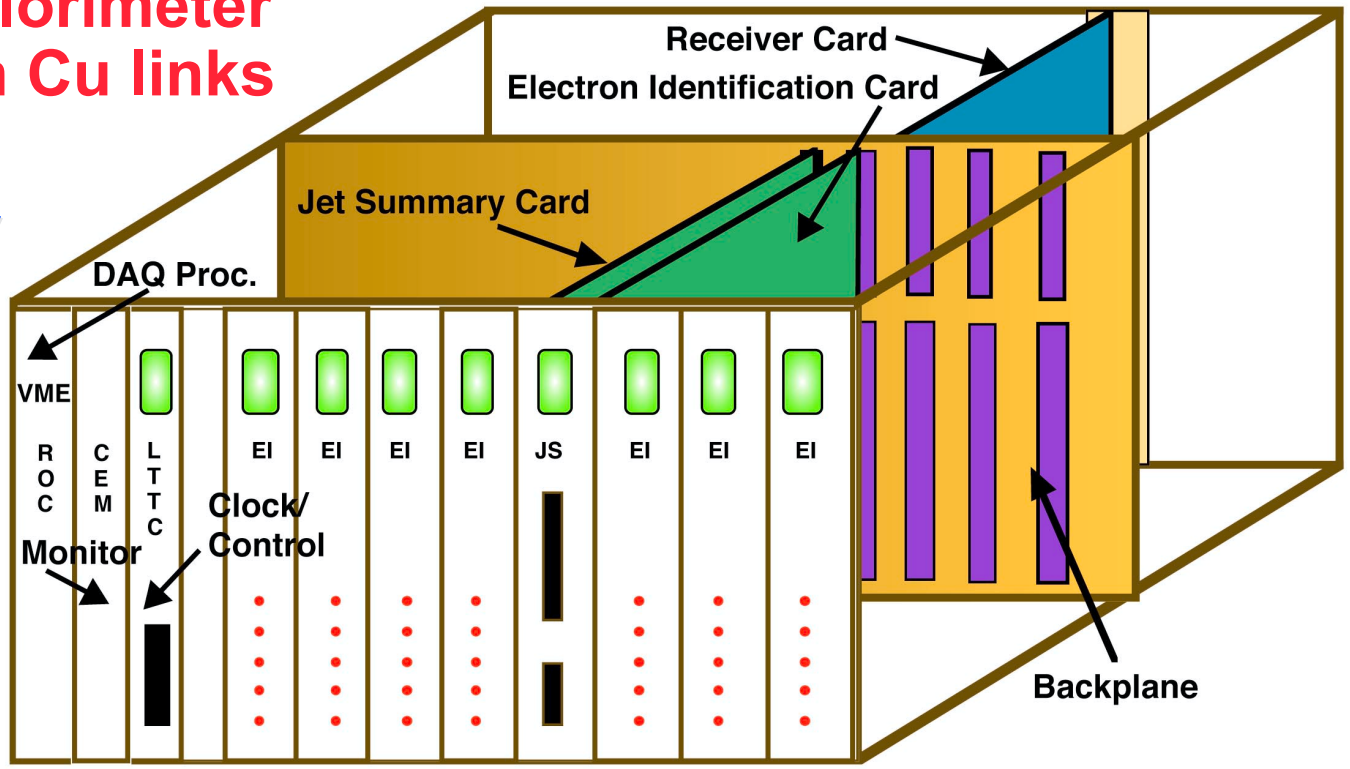
US CMS



Calorimeter Trigger Crate

Data from calorimeter Front End on Cu links @ 1.2 Gbaud

- ***Into 126* rear Receiver Cards***

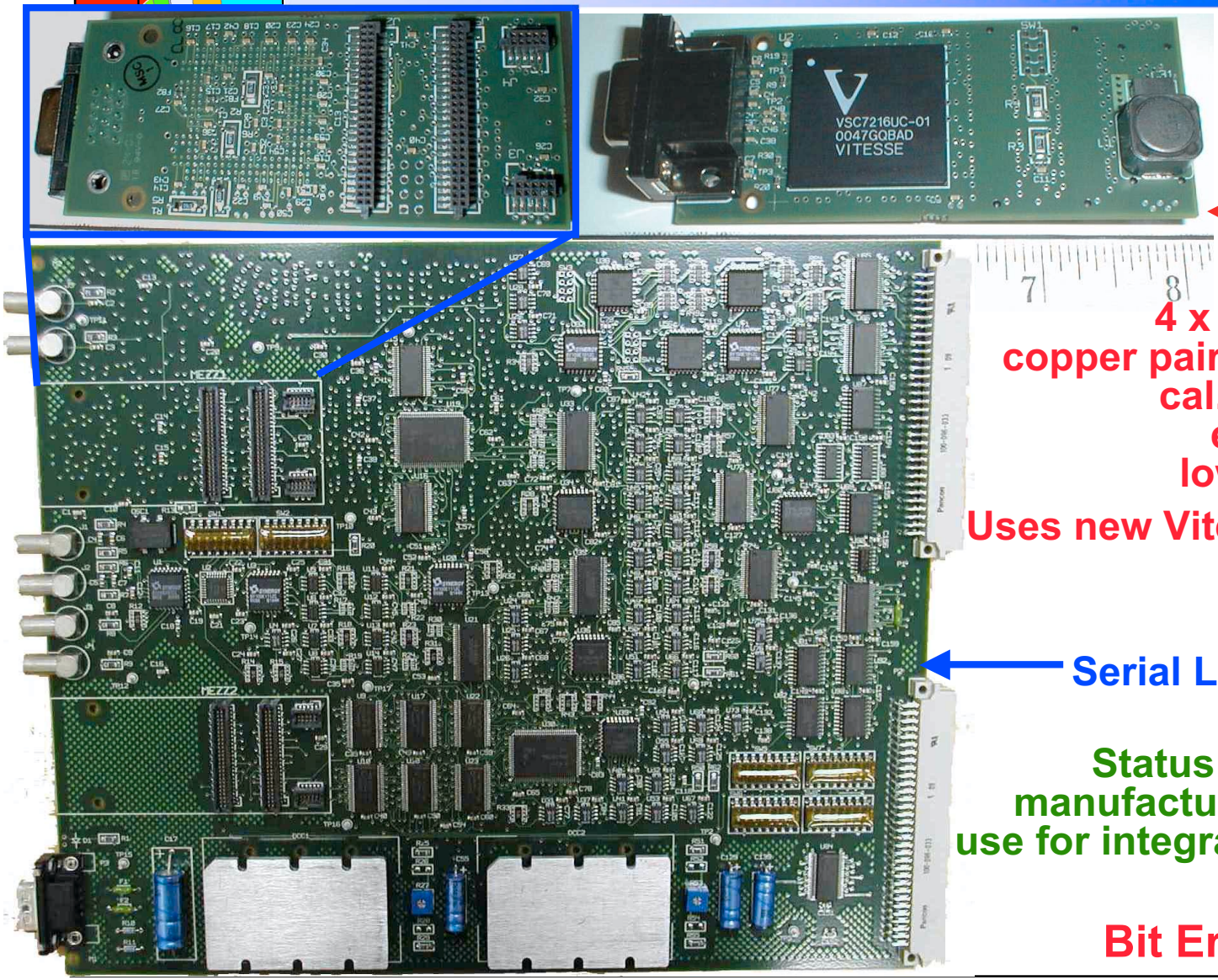


160 MHz point to point backplane

- **18* Clock&Control, 126* Electron ID, 18* Jet/Summary Cards**
  - all cards operate @ 160 MHz
- **Use 5 Custom Gate-Array 160 MHz GaAs Vitesse Digital ASICs**
  - Phase, Adder, Boundary Scan, Electron Isolation, Sort (manufactured)

**Spares not included*

New Cal. Trig. 4 Gbaud Copper Link Cards & Serial Test Card



8 Compact Mezzanine Cards for each Receiver Card accept 4 x 20 m 1.2-Gbaud copper pairs transmitting 2 cal. tower energies every 25 ns with low cost & power.

Uses new Vitesse Link Chips (7216-01).

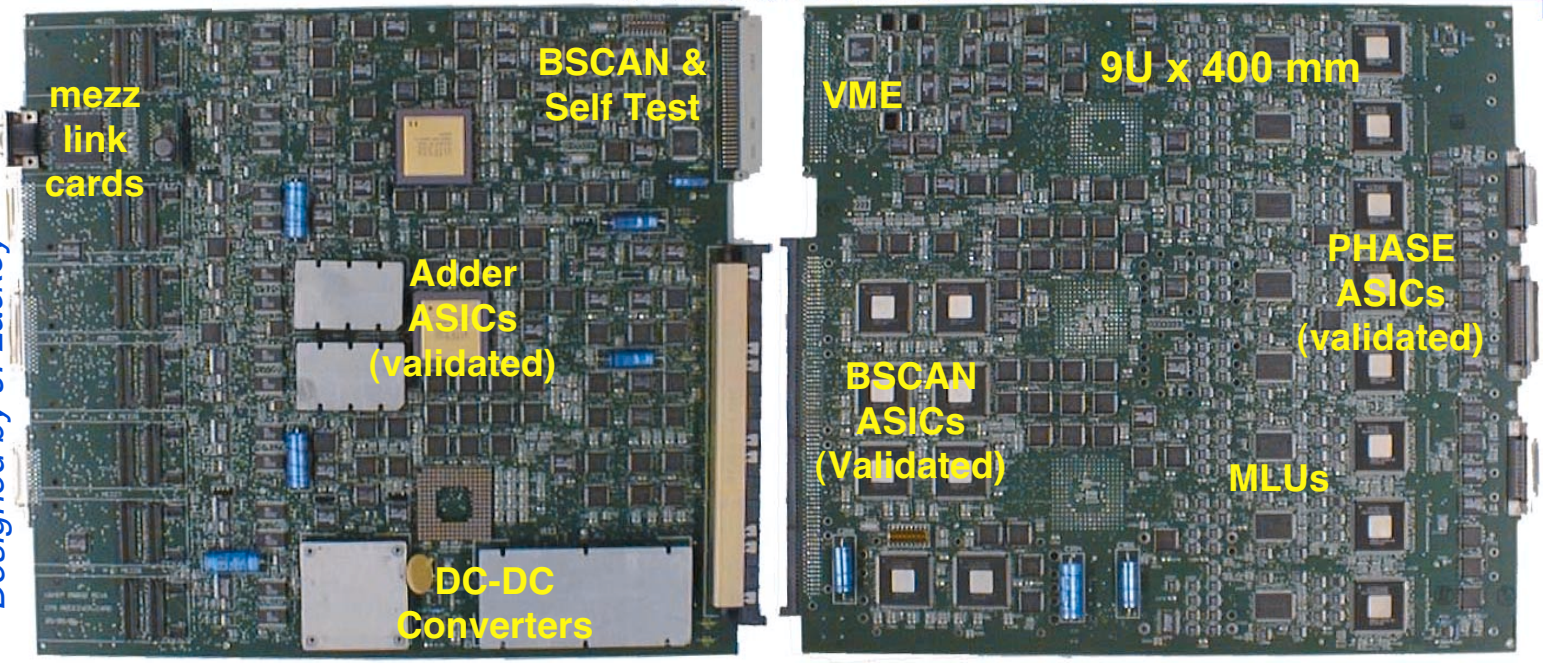
Serial Link Test Card to check links

Status: full production manufactured, currently in use for integration with ECAL

Test Results:
Bit Error rate < 10^{-15}

Calorimeter Trigger Receiver Card

Calo In:
4 Chan.
24 bits:
2x9 data
+ 5 error



Designed by J. Lackey

Top side with 1 of 8 mezzanine cards & 2 of 3 Adder ASICs

Bottom side with all Phase & Boundary Scan ASICs

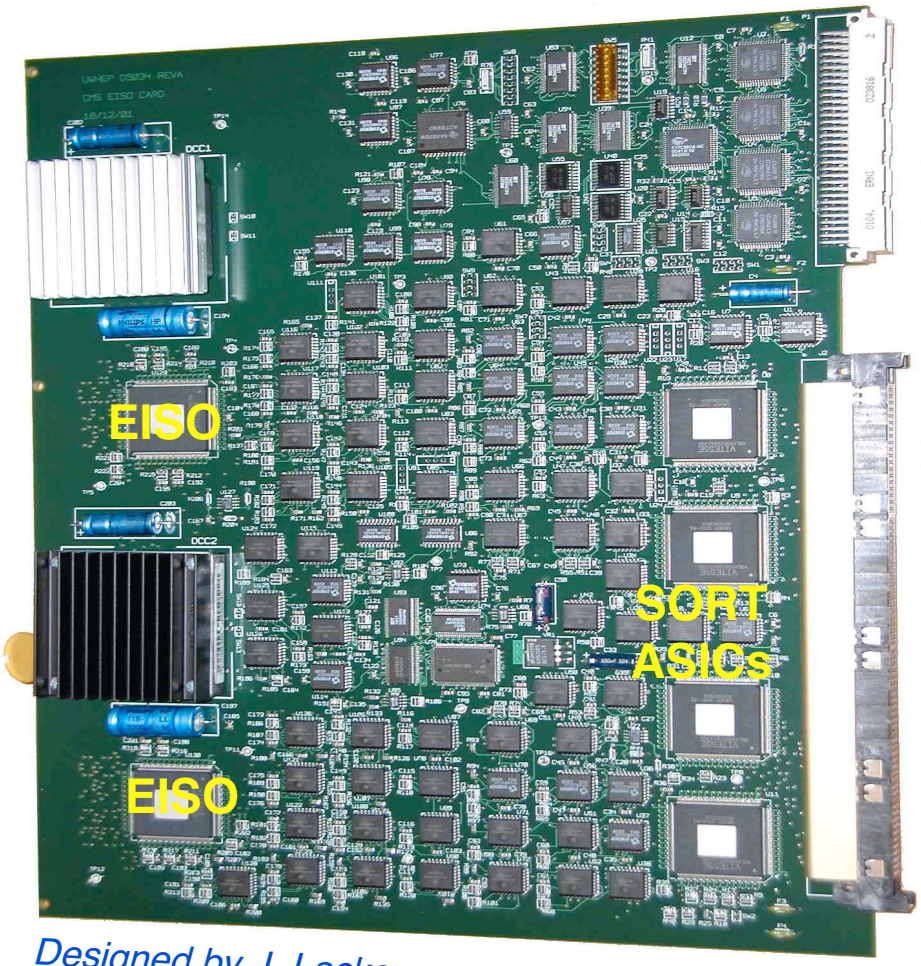
32 Channels = 4 Ch. x 8 mezzanine cards with Vitesse 7216-1 1.2 GBaud copper receivers

V7216-1 deserializes data and sends 120 MHz TTL to front Phase ASIC

Phase ASIC: Deskew,Mux @ 160MHz
Error bit for each 4x4, Test Vectors
Memory LUT @ 160 MHz
Adder ASIC: 8 inputs @ 160 MHz in 25 ns.
BSCAN ASIC: Provides Board BSCAN & Diff. Output@160 MHz to backplane

Full featured final prototype board is validated - production underway, boards manufactured for full crate test, 1422 mezzanine cards being manufactured.

Electron Isolation Card



Designed by J. Lackey

Full featured final prototype board is validated and in production.

Processes 4x8 region @ 160 MHz

Uses Sort and EISO ASICs

- **Both tested by Vitesse before delivery**
- **Sort ASIC used for Backplane Receive**
  - Validated
- **Electron Isolation ASIC**
  - Mostly validated
  - neighbor data for e/γ isolation algorithm needs add'l RCs

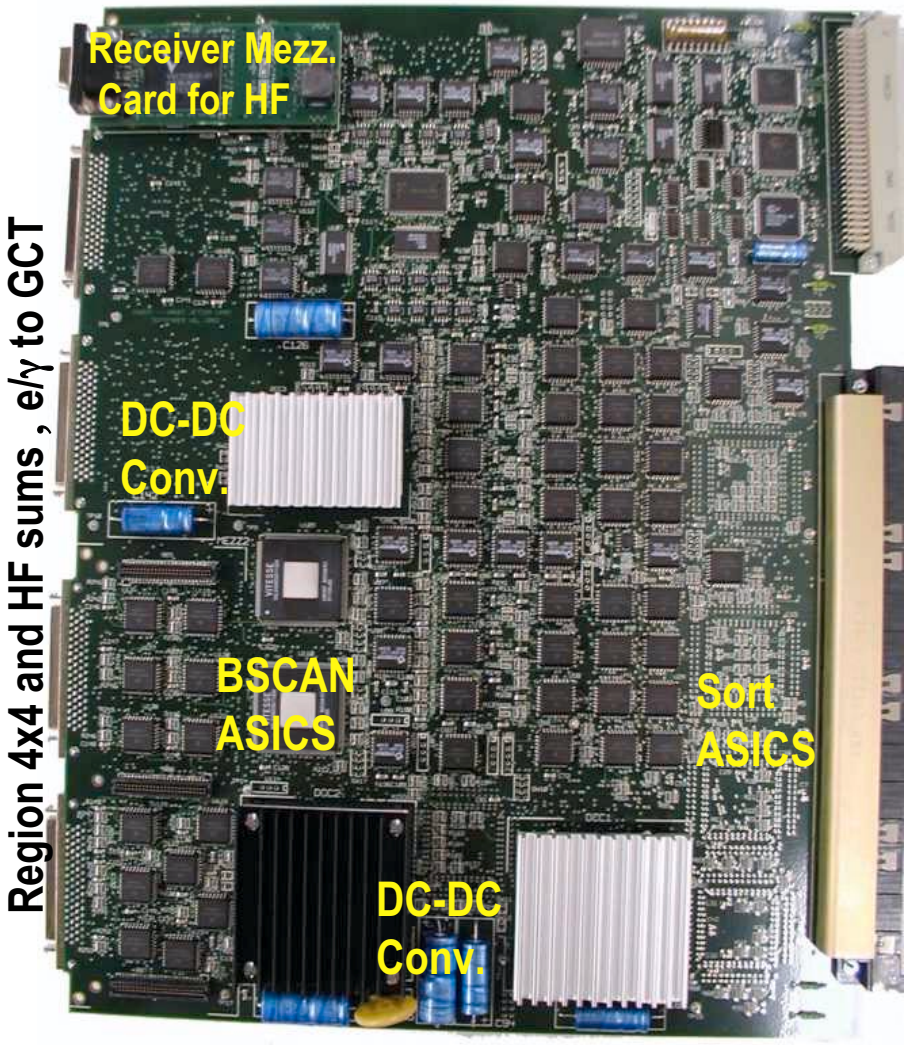
Lookup tables for ranking

Highest energy isolated and non-isolated e/γ per 4x4 region sent to Jet/Summary card for sorting, forwarding to Global Cal. Trig.

Jet/Summary Card

Summarizes full crate:

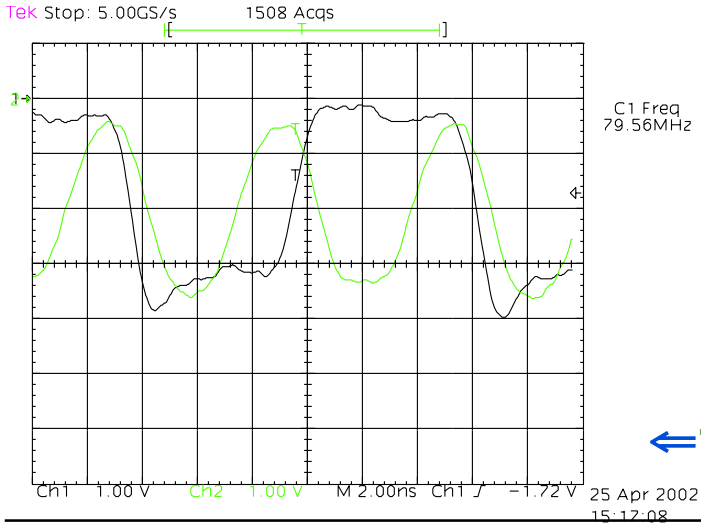
- **Electron/photon/muon**
  - SORT ASICs receive data on backplane and find top four e/γ (of 14 each isolated and non-isolated)
  - Threshold for muon Minimum Ionizing & Quiet bits (one per 4x4 region)
  - Data to Clustering/GCT
- **Forward Calorimeter (HF) functionality**
  - Reuses Mezzanine Card to read in data directly for inclusion in output
  - LUTs for HF regions
- **Region energies**
  - HF and 4x4 tower sums (regions) to cluster crate for central, τ, and forward jet; calculation of global quantities total and missing E_T
- **Under Test**
  - HF path checked
  - Data seen over backplane at Sort ASICs
  - 4x4 tower sum path checked to output



Testing Receiver, Clock, EISO, & Jet/Summary Cards, Crate, & Backplane

Crate Rear: Loopback Cables to test inter-crate data sharing

Front: Clock, EISO, and Jet/Sum Cards with original STC and cable to test HF data transfer to Jet/Summary card at full speed

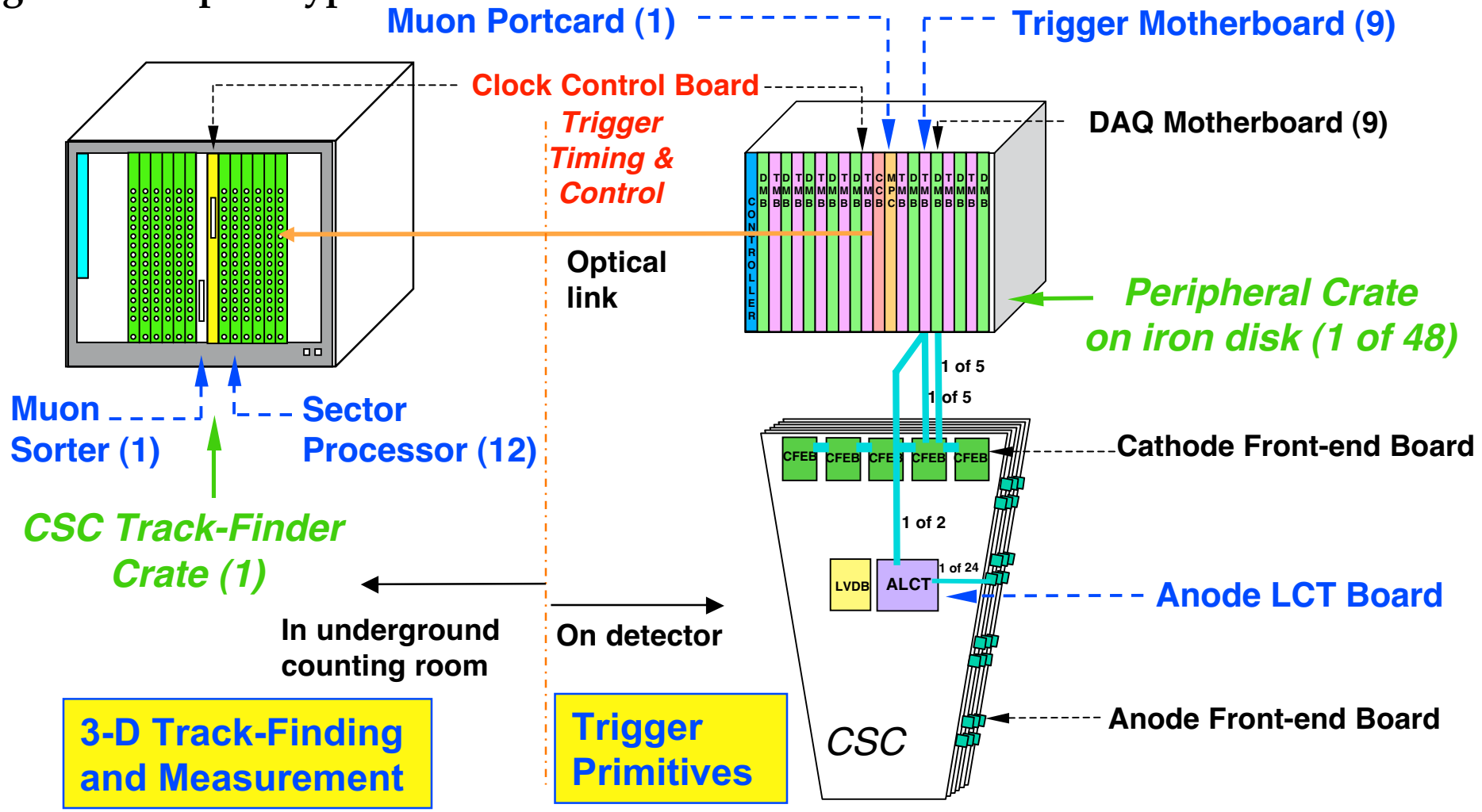


⇐160 MHz TTL clock with data into 200 MHz Memories (2 ns scale)

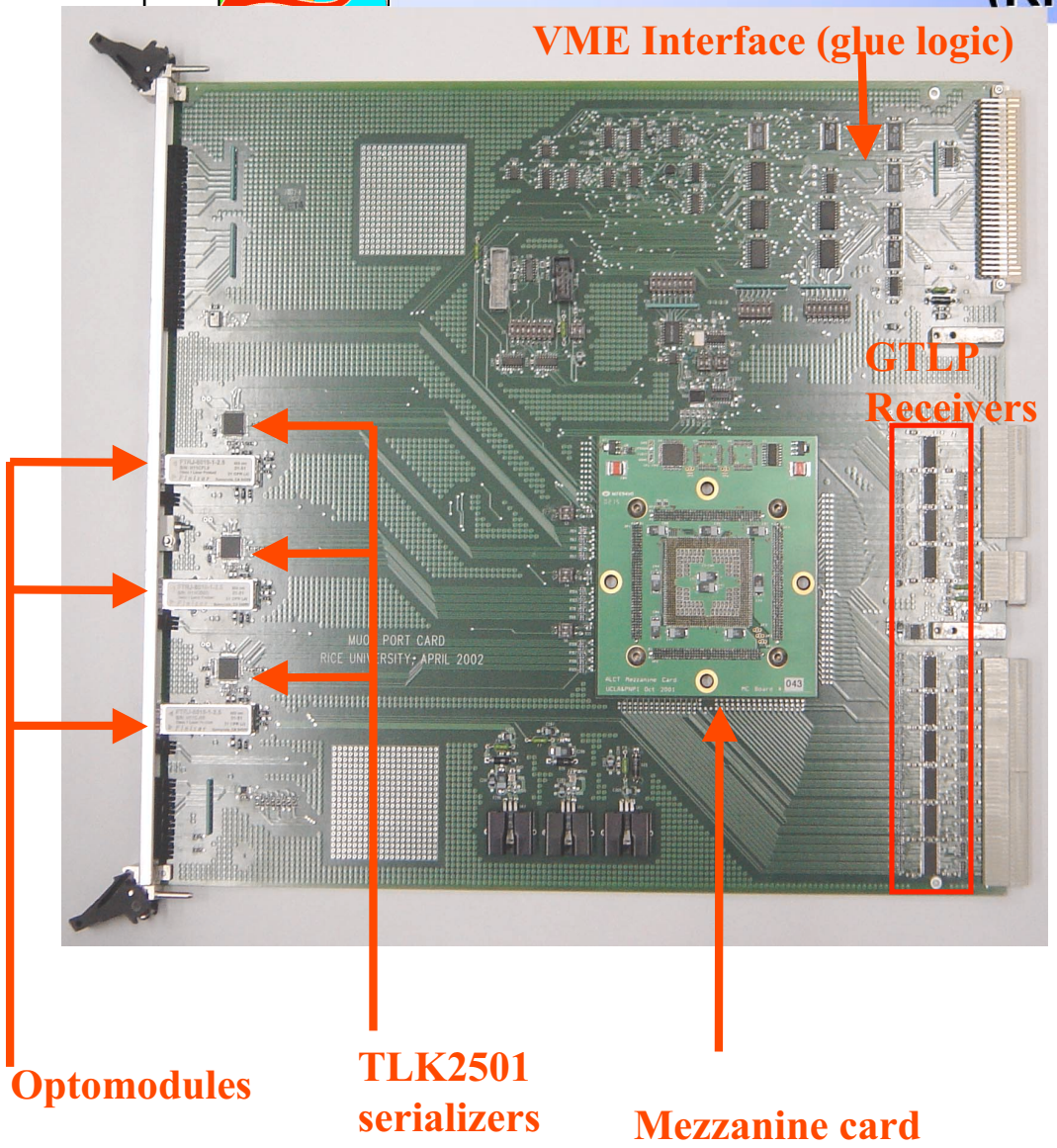
CSC Muon Trigger Scheme

TriDAS part: Second generation prototypes

EMU part: mostly in production



Muon Port Card
(Rice)

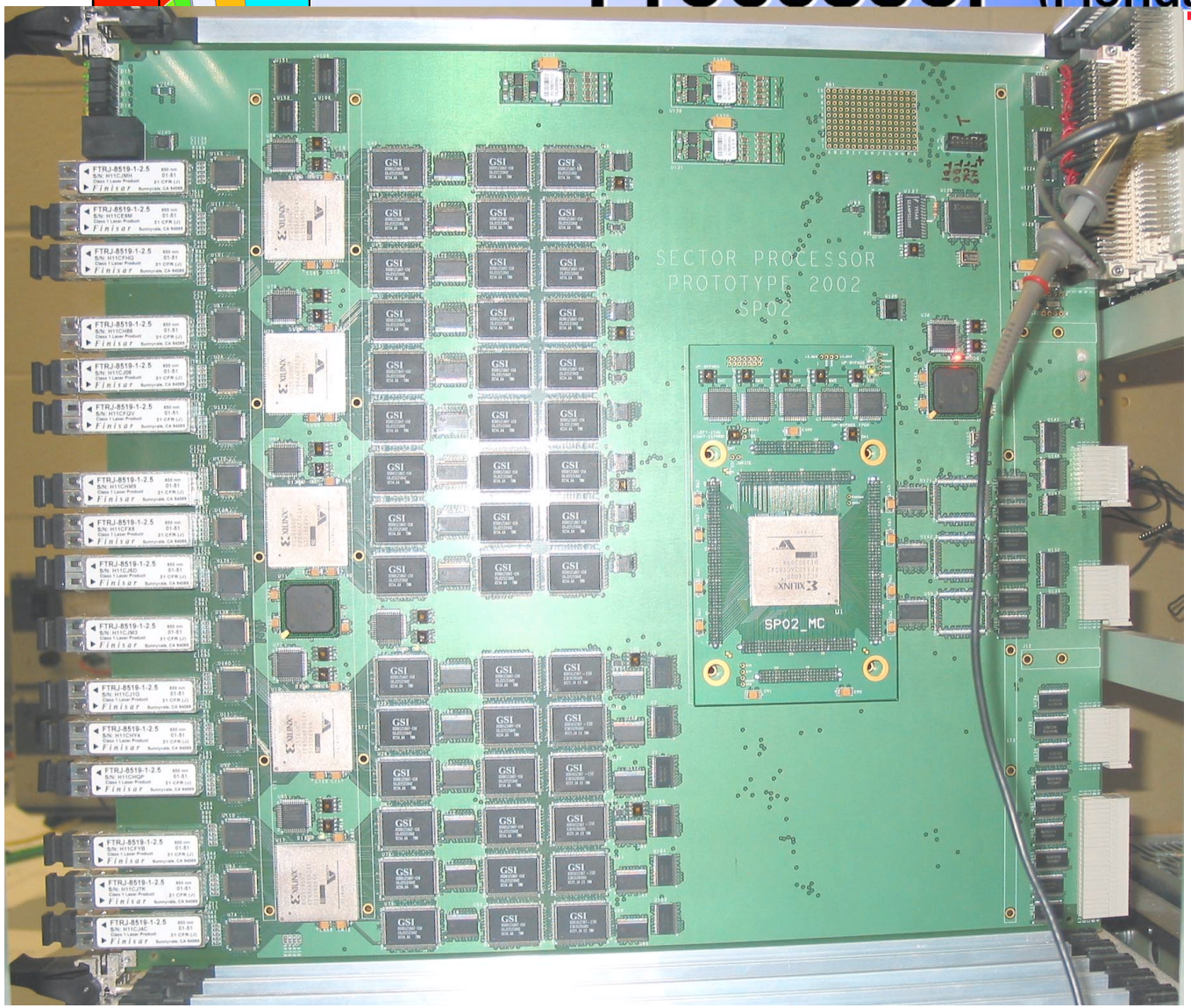


3 boards were fabricated and assembled in summer

- Have 6 UCLA mezzanine cards
- Tested MPC standalone (sorter logic) & w/1 &2 Trigger Motherboards & full-size custom backplane
  - patterns sent from TMB to MPC at 80MHz
  - feedback "winner" bits from MPC to TMB
  - periodic FPGA reconfiguration from EPROMs
  - measured the board latency

Waiting to test with Sector Receiver/Processor

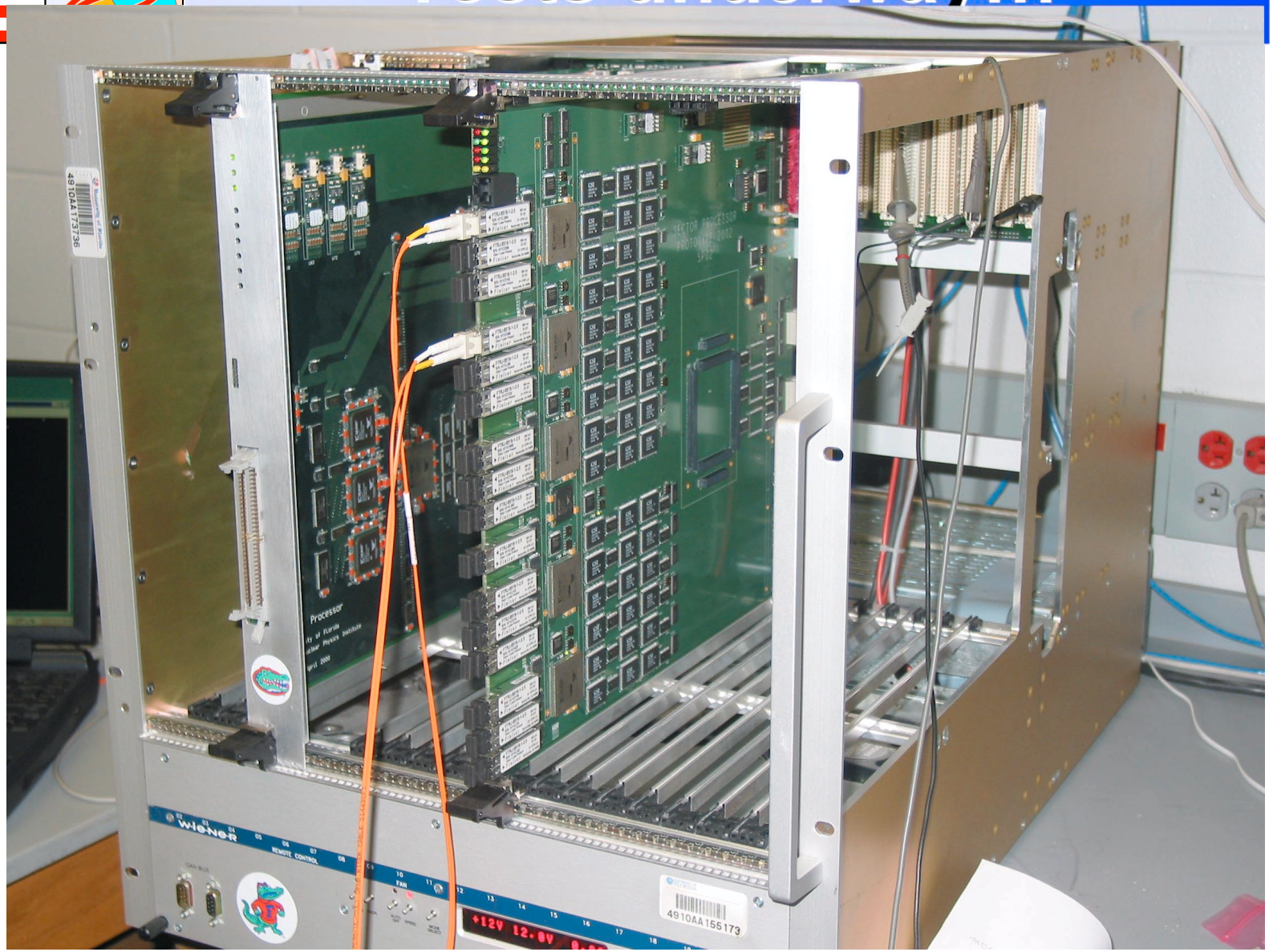
Next Generation Sector Processor (Florida)



Tests

- Both SP main board and mezzanine board pass power-up and initial FPGA programming tests
- Validation of VME interface is underway
- Optical link tests underway

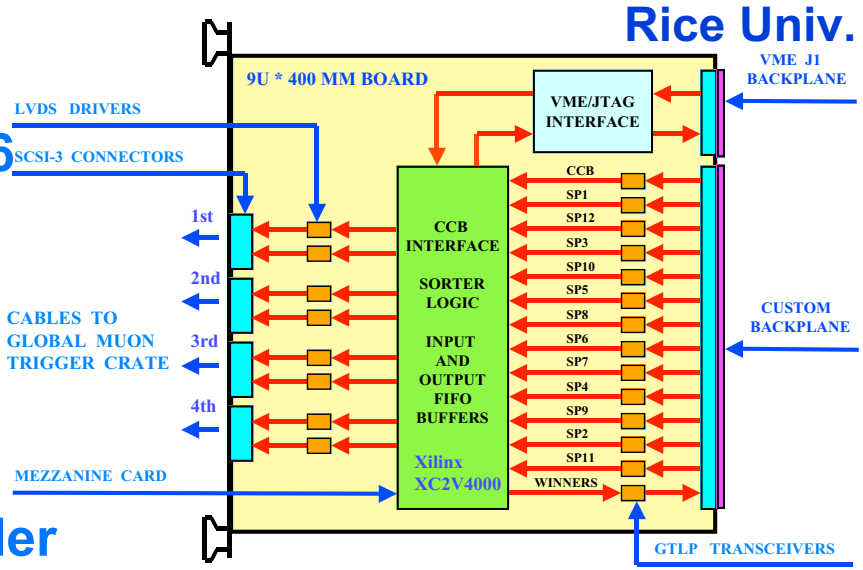
Tests underway…



CSC Muon Sorter

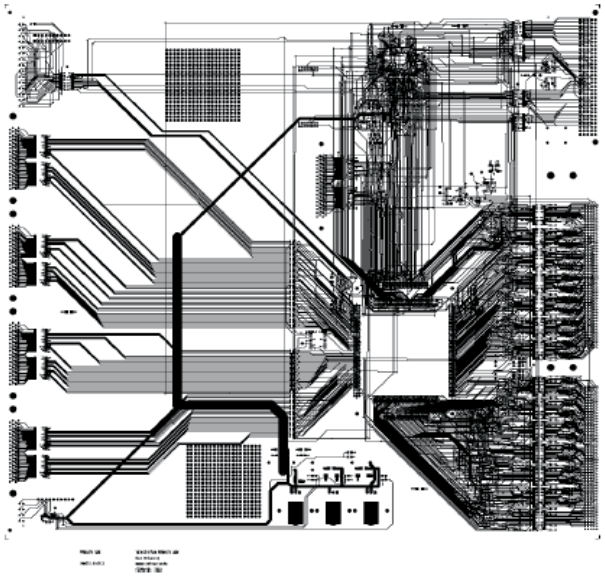
Functionality

- Selects 4 best muons out of 36 arriving from 12 Sector Processors
- Sorting is based on 7-bit Rank
- Transmits 4 best muons to Global Muon Trigger crate over LVDS links in ranked order



Status

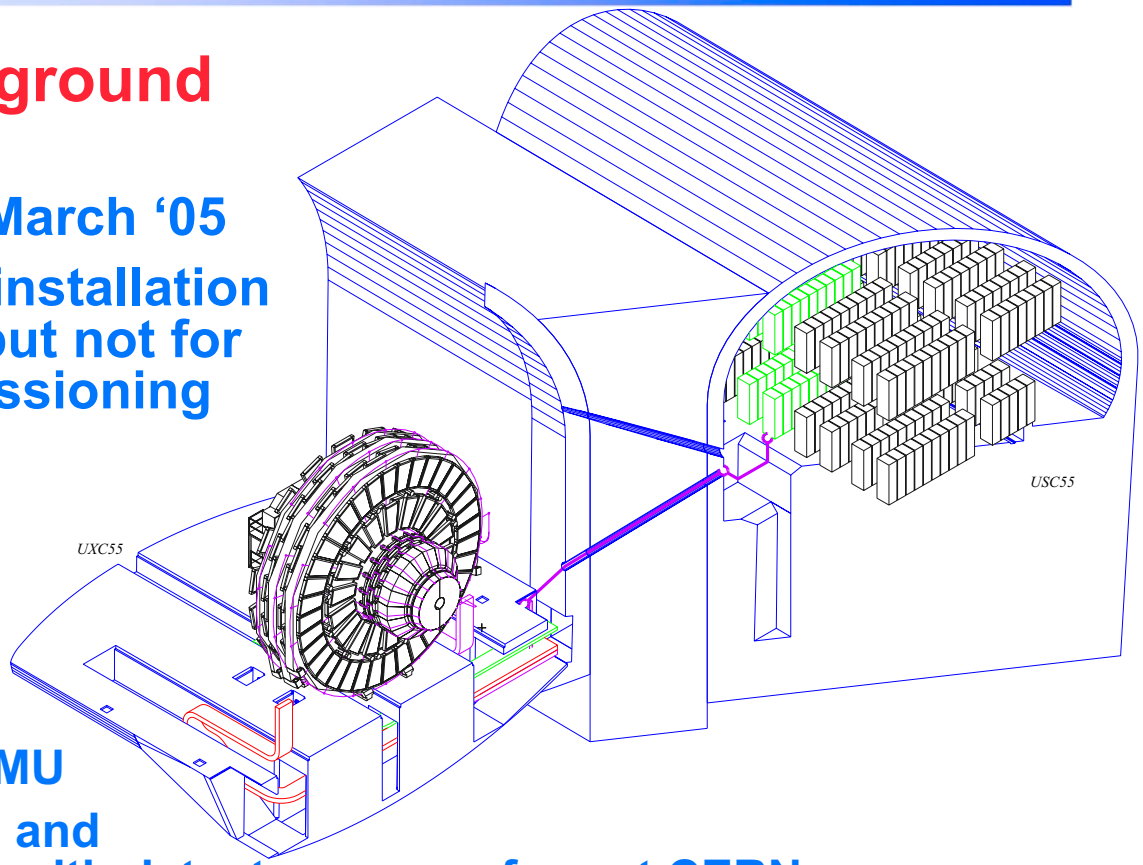
- Have 3 PCBs in hand
- Uses same mezzanine card as SP
- Standalone tests underway
- Tests with SP starts in summer



Define Trigger Completion

Installation in Underground Counting Room

- Expect access by March '05
- Sufficient time for installation and some testing but not for completing commissioning with detectors



Slice Test (on surface)

With Both HCAL and EMU

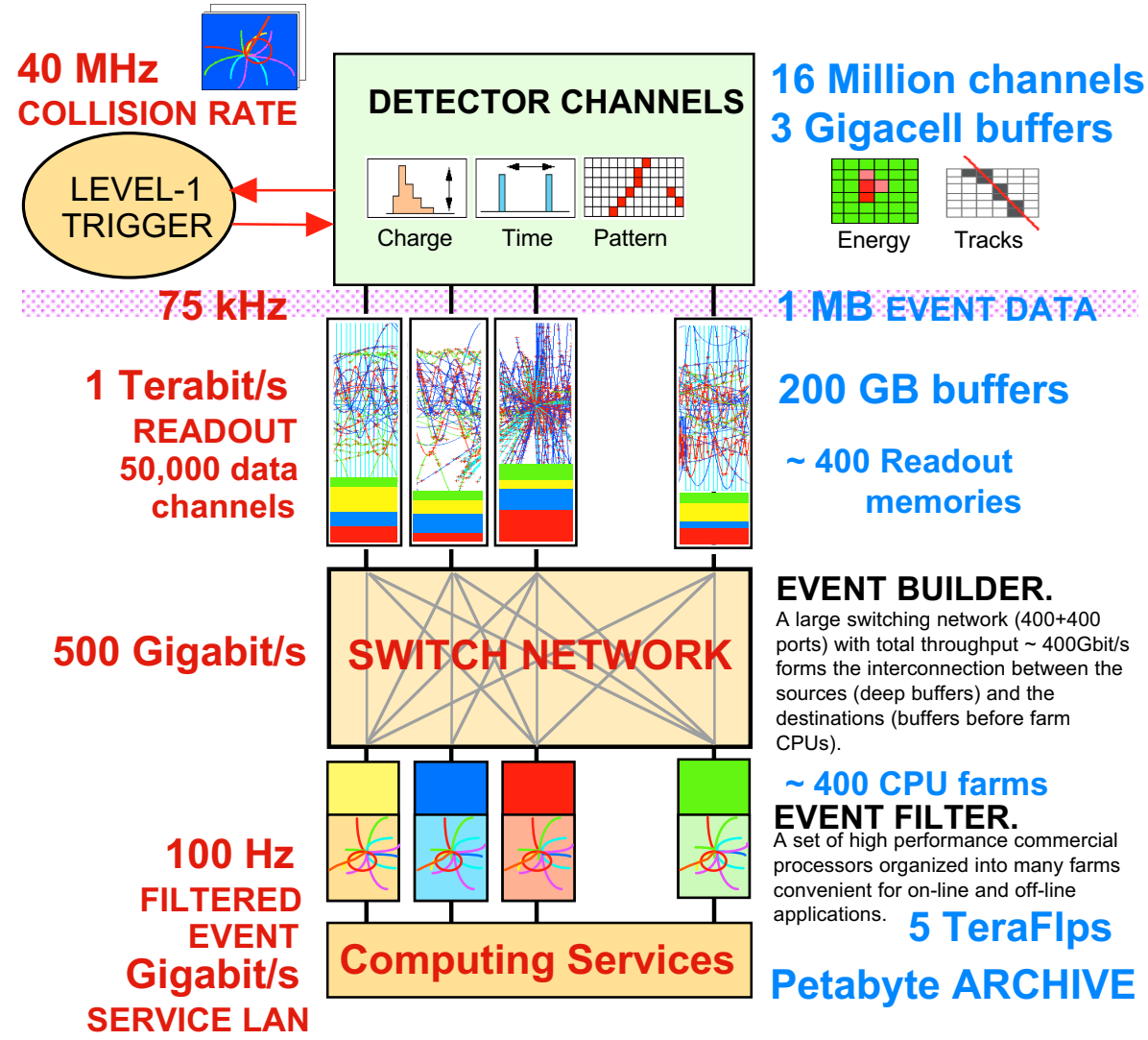
Verify trigger functions and interfaces by testing with detectors on surface at CERN.

Suggest as substitute for commissioning completion step.

Will check as much on surface before gaining access to underground facilities.

Milestone (HG1018) planned for completion November '04

DAQ System Overview



Original design:
L-1 @ 100 kHz

Rescope:
1997: 75kHz

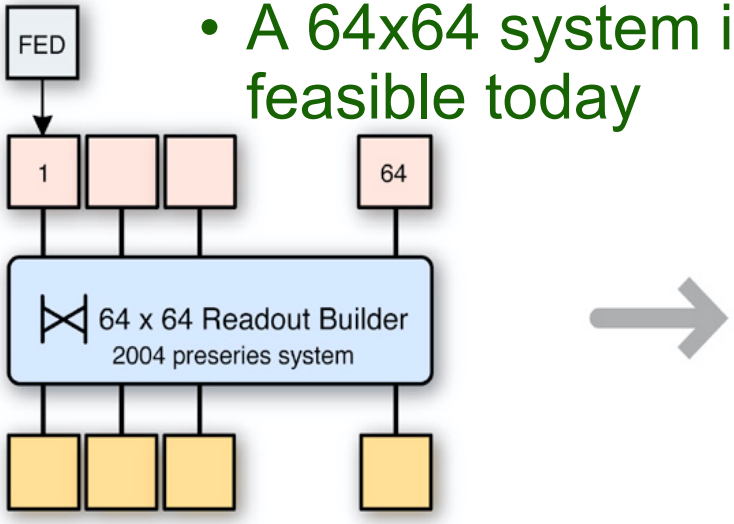
2001: Initial
L-1 @ 50 kHz

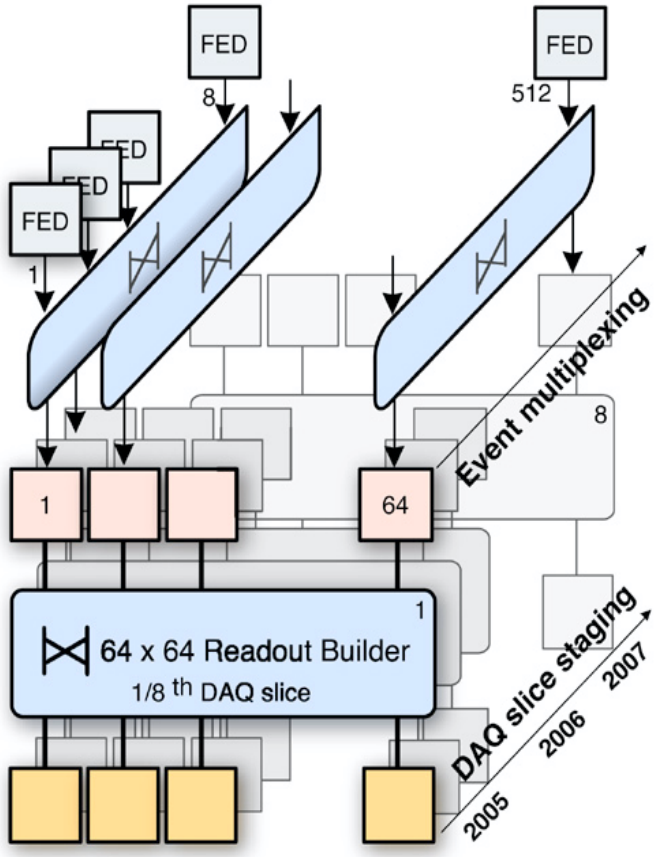
But design all elements to be able to do 100 kHz

New DAQ design: principle

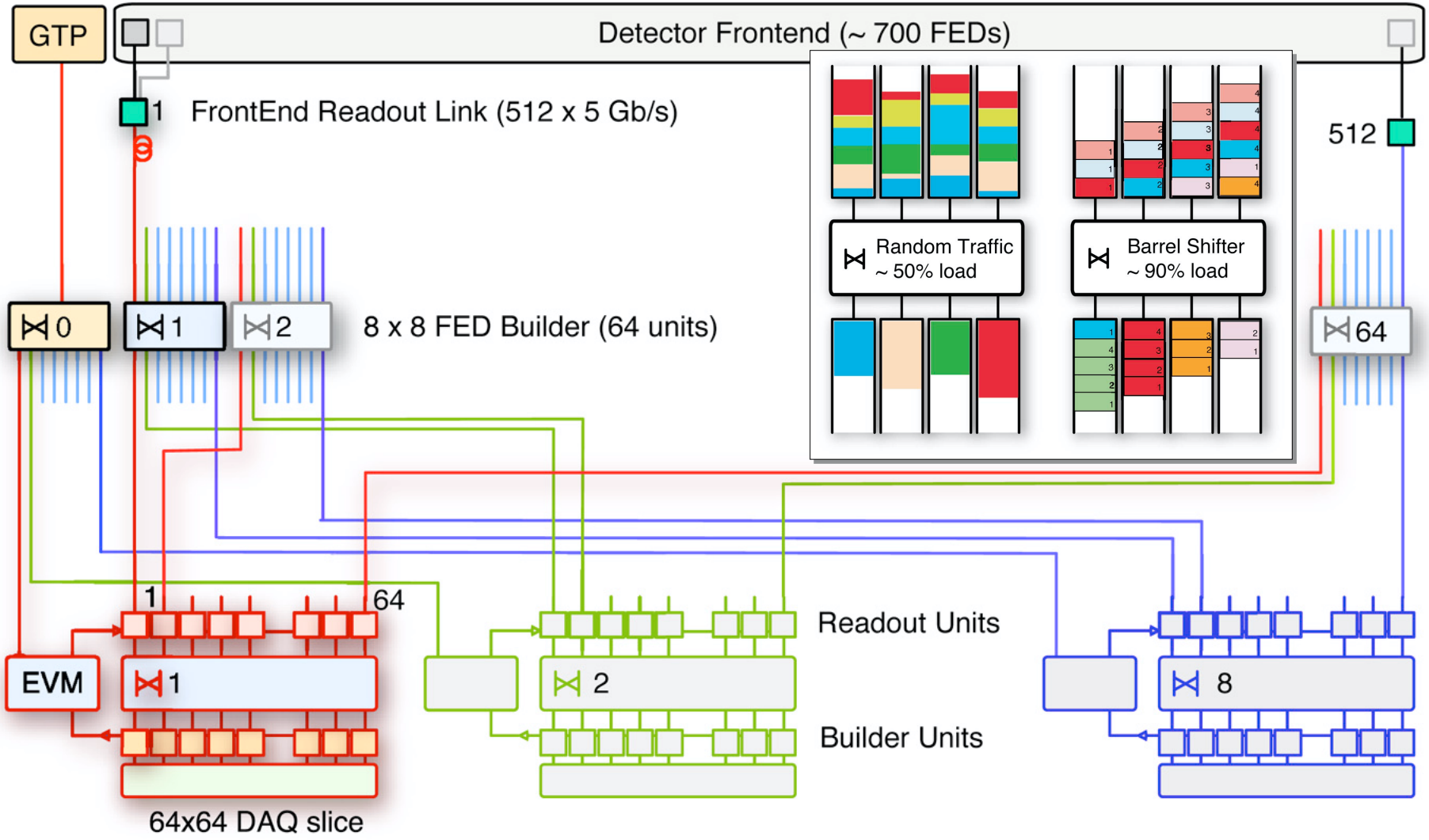
Basic principle:

- **Break DAQ into a number of functionally identical, parallel, smaller DAQ systems**
  - A 64x64 system is feasible today

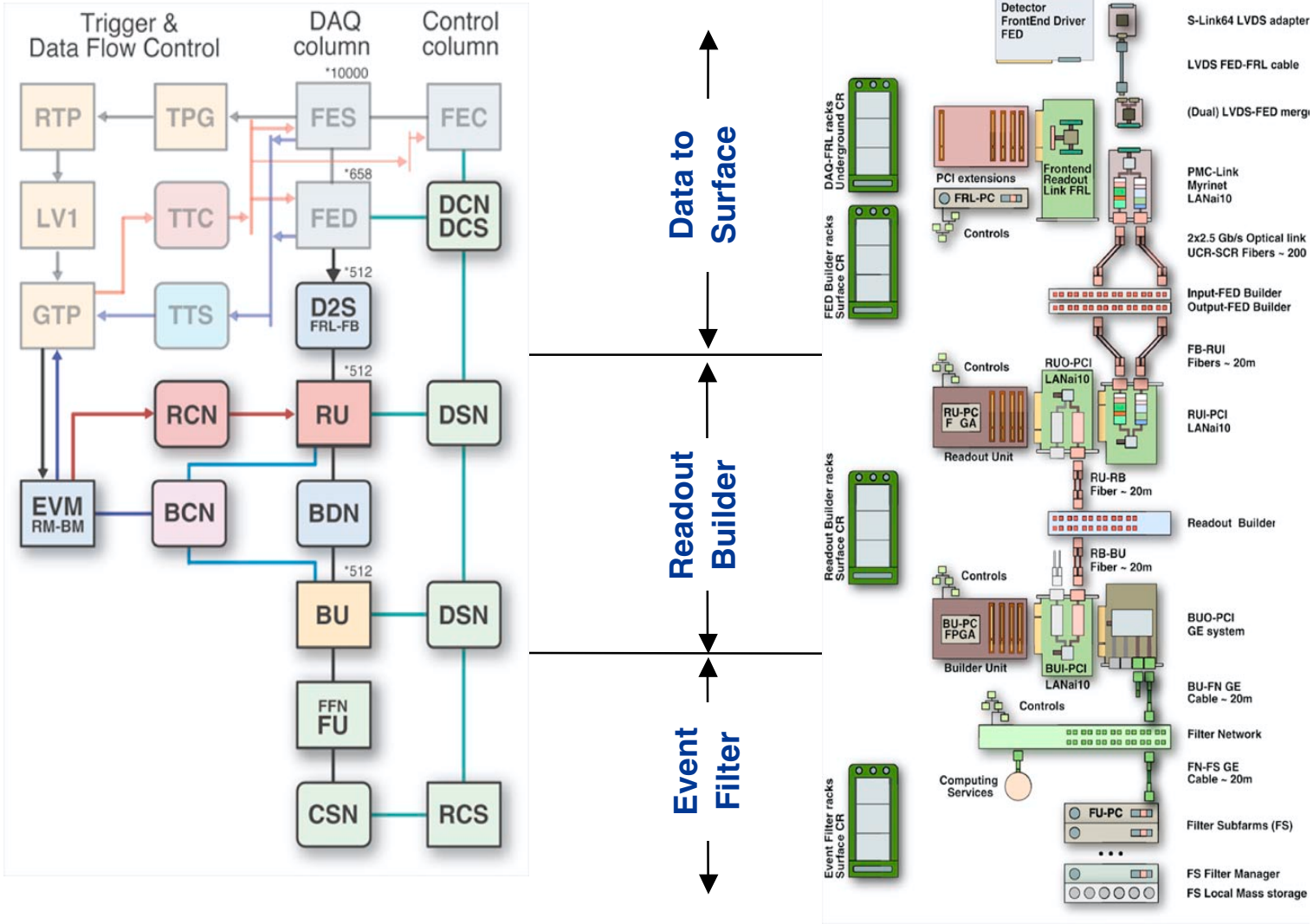




Detector readout to surface



D2S + RB + EF breakdown



US contribution

Cover one segment (1/8) of the CMS DAQ plus _ of the Data-to-Surface system (plus the associated prototypes – "preseries")

- **Segment: 1 Readout Builder + 1 Event Filter**
- **US_CMS detector electronics is ~1/4 of the total**
- **Delivery of the system can be accomplished by the end of the US_CMS project (FY05)**
- **Aids the experiment most in the current phase where cash flow is very tight**
  - US R&D program can remain ~ unchanged (to the extent that the basic modules are the same)

Roughly speaking, the US

(a) works on/delivers prototype system (to 2004)

(b) delivers the "startup DAQ" for CMS (2005)

Milestones*

Prototype DAQ (US Contribution)

D2S Prototype	July, 2004
"Slice Test"	November, 2004 (*)
Readout Builder Prototype	April, 2005

Startup DAQ (US Contribution)

Filter Farm Ready	May, 2006
Readout Builder Ready	August, 2006

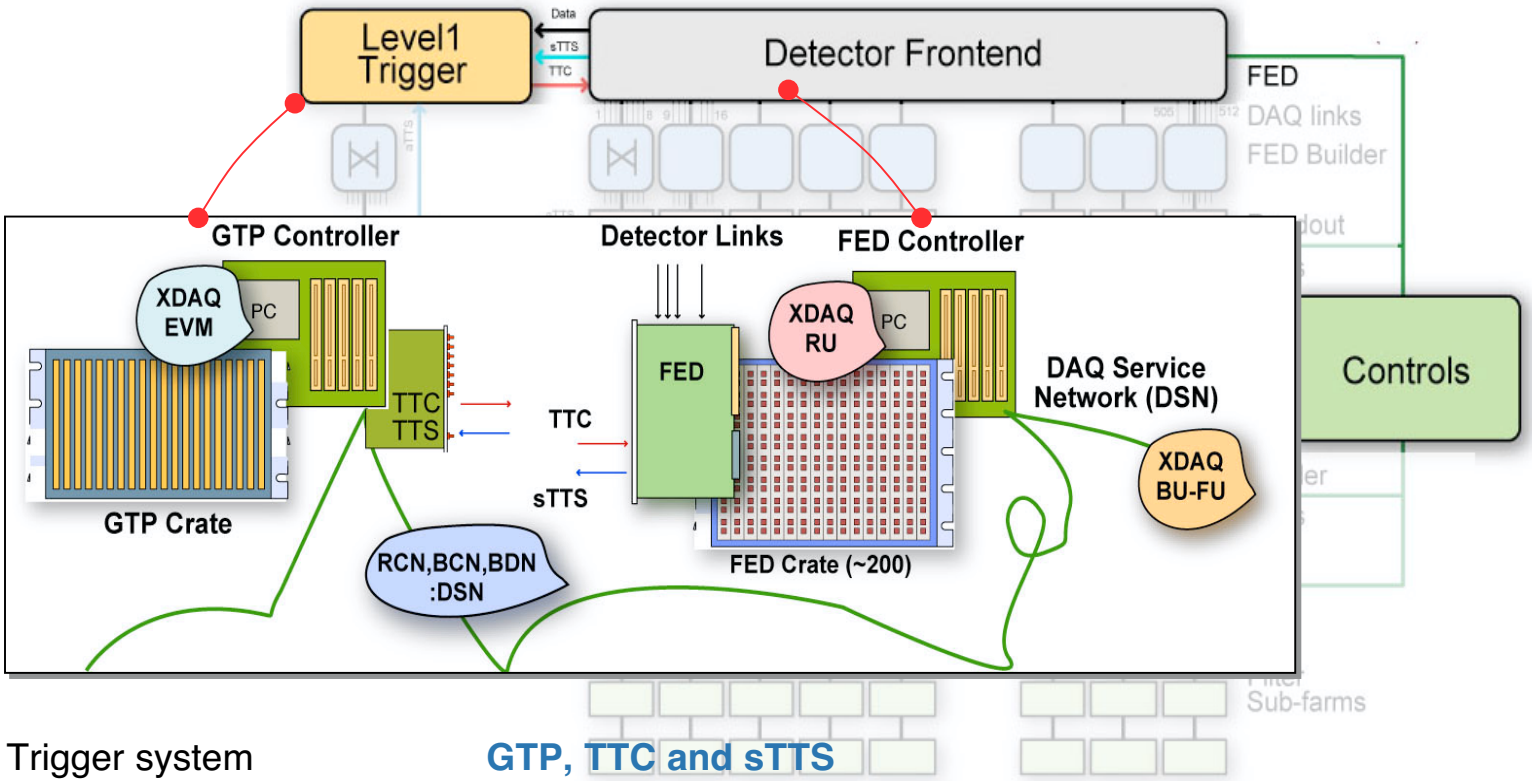
Declaration of Completion (US Contribution)

Startup DAQ ready for beam	September, 2006

(*) "Slice" Test for US-CMS detectors – DAQ will have full D2S proto + a few RB elements

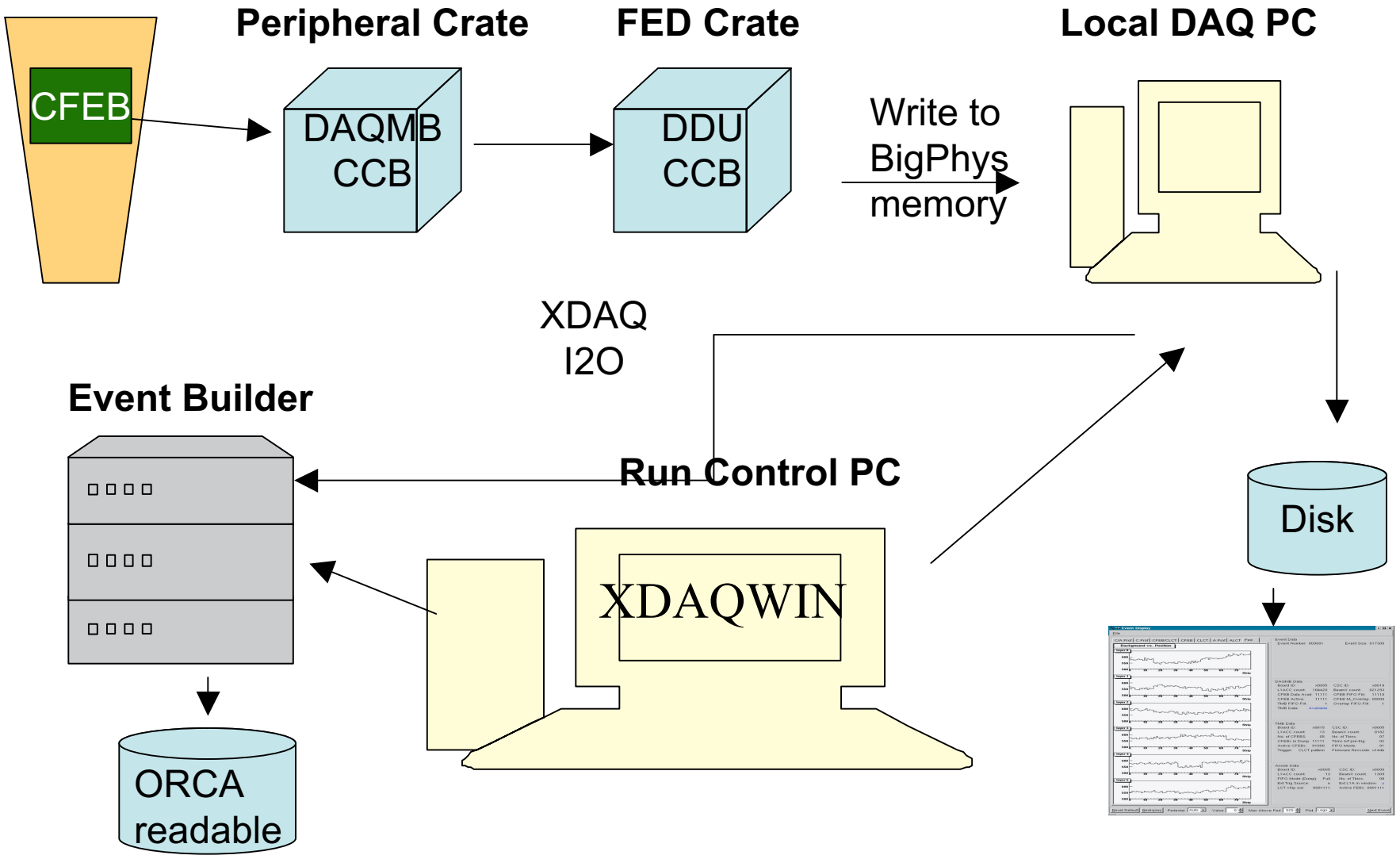
*(Version 33)

Slice Test DAQ (10-100 Hz)



Trigger system	**GTP, TTC and sTTS**
Detector readout	Complete **FED crate systems** (FED-TTC-TTS, Controller CPU+DSN)
Readout Units	XDAQ **RU-VME-tasks** running in all the **FED controllers**
Data to Surface	None just the **FED-VME bus** of FED crates
RCN, BCN, BDN networks	DAQ Service Network (**DSN** e.g. GEthernet)
Event manager	XDAQ **EVM-task** running in the **GTP controller**
Builder/Filter Units	XDAQ BU-task running in **any DSN(WAN) CPU**
Performances	**Few 10 Hz (up to 100s when using GE switches in DSN as EVB)**

Draft Configuration for EMU Slice Test

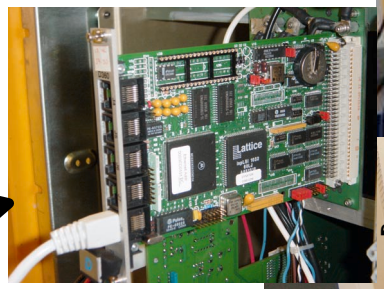


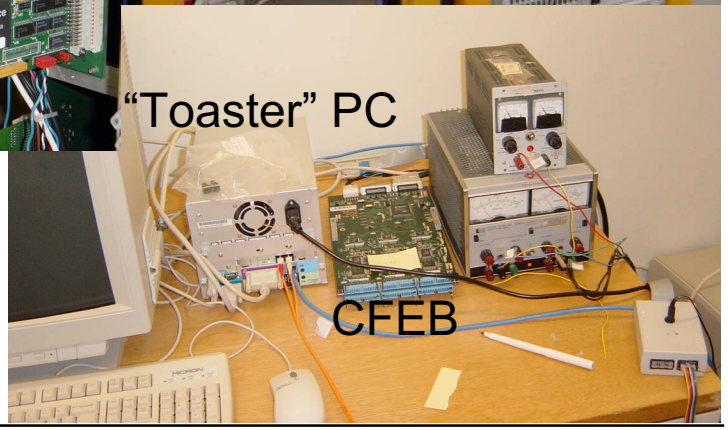
CMS Slice Test DAQ Work at Fermilab

Starting this January a group (Davis, Fermilab, Florida, OSU, Rice) worked at US CMS DAQ test stand with EMU Electronics, gaining experience & first pass at design.

Test Stand Consists of:

- **Fermilab CMS Event Builder farm**
- **UC Davis test crate:**
  - One VME crate
  - One DAQ Motherboard
  - One Dynatem 360
  - One Cathode Front End Board
  - Two toaster-shaped PC's for Local DAQ control





Preparing for May Test Beam