5   Calorimeter Regional Trigger

5.1   System Requirements

5.1.1   Physics requirements overview

The level 1 calorimeter trigger must provide triggers based on the presence of physics objects such as photons, electrons, taus and jets, as well as global sums of ET and missing ET (to find neutrinos). It must also provides additional information for the muon trigger system for isolation and minimum ionization signal identification. The ET thresholds for each of these objects are required to be tunable such that tolerable rates must be realized for discovery physics while providing sufficient sample of control events. At high luminosity, some of these discover modes place stringent requirements on the required thresholds. For example Higgs (100 GeV) decays to two photons, charged Higgs production in association with top or W decays to electron, Higgs (~200 GeV) decays to tau pairs (single prong hadronic or electron decays), SUSY sparticle (~300 GeV) decays to multi-jet events, etc.. For example, the required thresholds are about 50, 25 GeV with full efficiency for single and double electrons, 100, 50 GeV for single, double taus and 200, 100 GeV for single, double jets respectively. At low luminosity reduced thresholds are needed to study lower mass particles. The trigger system must be designed such that the efficiency is measurable.

5.1.2   Data acquisition requirements

The CMS data acquisition system is designed to function at 100 kHz while it is expected operate at 75 kHz. This 75 kHz bandwidth needs to be shared by triggers based on the candidates found solely in calorimeter or muon system and those based on combination of the two systems. Sufficient programmability should be present in the system so that the trigger rate can be tuned effectively during the data-taking period to account for luminosity and background variations. Further the physics simulations needed to estimate the rates are reliable only to a factor of 2 or 3. Therefore, our target rate for electron and jet triggers combined is about 12.5 kHz.

In order to understand the trigger system in detail output from every trigger subsystem is required to be readout by the DAQ system.

5.2   System Specifications

5.2.1   Input specification

Input to the regional calorimeter trigger for each trigger tower of the CMS calorimeters consists of 8-bit non-linear ET and a tower characterization bit. There are 52 η x 72 ϕ trigger towers matching in size for both barrel and endcap electromagnetic (EB, EE) and hadronic (HB, HE) sections of the calorimeter. The trigger tower segmentation in the very forward calorimeter (HF) is 2 (F/B) x 4 η x 18 ϕ. The input signals are organized such that there are two towers worth of data and error detection code bits per link, i.e., 18 bits data and 5 bits EDC. The 5 bit Hamming code

generated from the 18 bits of data is sufficient to detect all single and double bit errors as well as many multiple bit errors. The present design uses transmitter and receiver links capable of handling 24 bits of information in 25 nsec with a baud rate of 1.2 Gbaud. The link technology being considered for this design is based on the VSC7214 chip made by Vitesse which has 4 full duplex channels capable of running between 1.2 and 1.3 Gbaud. We will run it at 1.2 Gbaud, transferring 24 bits of information per crossing per channel. Copper cables under 20 m length are used for these gigabit links between calorimeter front-end electronics and trigger crates. The data across all the ECAL and HCAL trigger towers is expected to be synchronized.

5.2.2   Output specification

Regional calorimeter trigger output consists of lists top 4 candidates of various types and energy sums. The candidate lists are provided separately for isolated and non-isolated electron/ photons, central and forward jets, and taus (isolated narrow jets). Each of these candidates is specified by a 6-bit rank based on candidate ET and location information 4 or 5 bits to uniquely identify the 4x4 trigger tower region that the candidate belongs to. Eighteen ET sums covering all η and 20° ϕ segments are reported. All of these data are sent to the global calorimeter trigger using 80 MHz parallel differential ECL signals on 34 pair copper cables. In addition, muon isolation and MIP deposit identification bits are sent to the global muon trigger system via the global calorimeter trigger system.

5.2.3   Latency

The total latency of the level-1 trigger is set to be 3 μs or 120 crossings. The latency is expended in propagation of particles from the interaction (4 crossings), transmission of signals between various subsystems that make up the trigger decision and the trigger decision logic itself. A significant fraction, i.e., 38.3% or 46 crossings is expected to be spent just in the data transmission on cables. This estimate includes 18 crossings in optical link between calorimeter front-end and trigger primitives subsystems, 4 crossings in copper link between trigger primitives and regional trigger subsystems, 4 crossings in copper link between regional and global calorimeter trigger subsystems, 2 crossings in copper link between global calorimeter and final trigger subsystem and finally 18 crossings in the link back to the front-end. This leaves 70 crossings for processing in all five subsystems and any contigency. About a third of this latency is allocated for the regional calorimeter trigger processing as it is used for bulk of the data reduction process.

5.3   System Overview

5.3.1   System functionality

The calorimeter level 1 trigger system receives digital trigger sums from the front-end electronics system, which transmits energy on an eight bit compressed scale. The data for two trigger towers of the same calorimeter (EB, EE, HB, HE or HF), for the same crossing, will be sent on a single link in eight bits apiece accompanied by five bits of error detection code and a 'fine-grain" bit characterizing the energies summed into the trigger towers, i.e. isolated energy for EB,

EE or an energy deposit consistent with minimum ionizing particle for HB, HE. Presently the fine-grain bit is undefined for the HF calorimeter.

The calorimeter regional crate system uses 20 regional processor crates covering the full detector. Eighteen crates are dedicated to the barrel and two endcaps. These crates cover the region |h|<3. One special crate covers both HF Calorimeters that extend missing ET and jet finding coverage to |h|<5. The remaining crate collects regional information from these 19 trigger crates and clusters their regions to find jets and taus. It also continues the summation tree to provide sums of ET in various ϕ regions.

Each calorimeter regional crate transmits to the calorimeter global trigger processor its 4 highest-ranked isolated and non-isolated electrons. The cluster crate sends its 9x4 highest energy central and forward jets and tau candidates along with information about their location and sum Et for 18 f regions covered by it. The global calorimeter trigger then forms Ex and Ey using look-up-tables and sums the energies, separately sorts the electrons, jets and taus, and sends the top four calorimeter-wide candidates, as well as the total calorimeter missing and sum Et to the CMS global trigger. The muon isolation and identification bits formed using the HB, HE information are passed to the global muon crates via the global calorimeter trigger system.

Eighteen crates of the Calorimeter Regional Trigger use three custom board designs which are dedicated to receiving and processing data from the barrel and endcap calorimeters. In these crates there are seven rear mounted Receiver cards, seven front mounted Electron Isolation cards, and one front mounted Jet Summary card for a total of 15 processor cards per crate. These cards and an additional clock and control card are plugged into custom "backplane" which provides point-to-point links between the cards. VME bus is also provided to these cards using high density connectors in top 3U section of the backplane. In addition there are two slots with standard VME backplane connectors for crate processor and monitoring cards. The 19th crate covering the HF calorimeter houses special cards that use portions of circuitry of the Reciver and Jet Summary cards to drive the signals out for forming jets and ET sums. The 20th cluster crate is similar to the 18 barrel and endcap crates but is fit with a different backplane and set of cluster processor cards which implement jet and tau finding algorithms and ET sums.

5.3.2   Calorimeter trigger tower mapping

(Description of calorimeter trigger tower mapping to the region calorimeter trigger system showing crates, cards. Quantify the backplane and inter-crate data link bit counts ...)
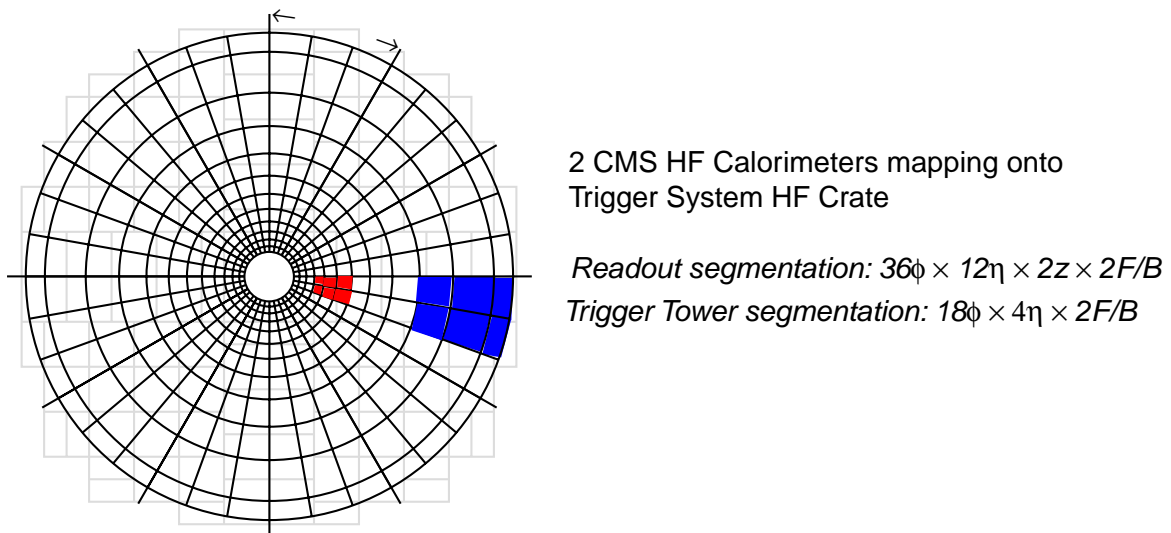
The barrel and endcap trigger towers in the region -3 < h < 3 and 0 < f < 2p, are processed in 18 regional crates. The mapping of the calorimeter to the trigger crates is shown in Fig. 5.1. Each crate covers a 40° f region and one half of the h. Each crate has 7 fully occupied cards covering fourteen 4x4 trigger tower regions. The neighbor data needed for seamless coverage of the electron

isolation algorithm is either obtained on the crate backplane or by using inter-crate cable connections.
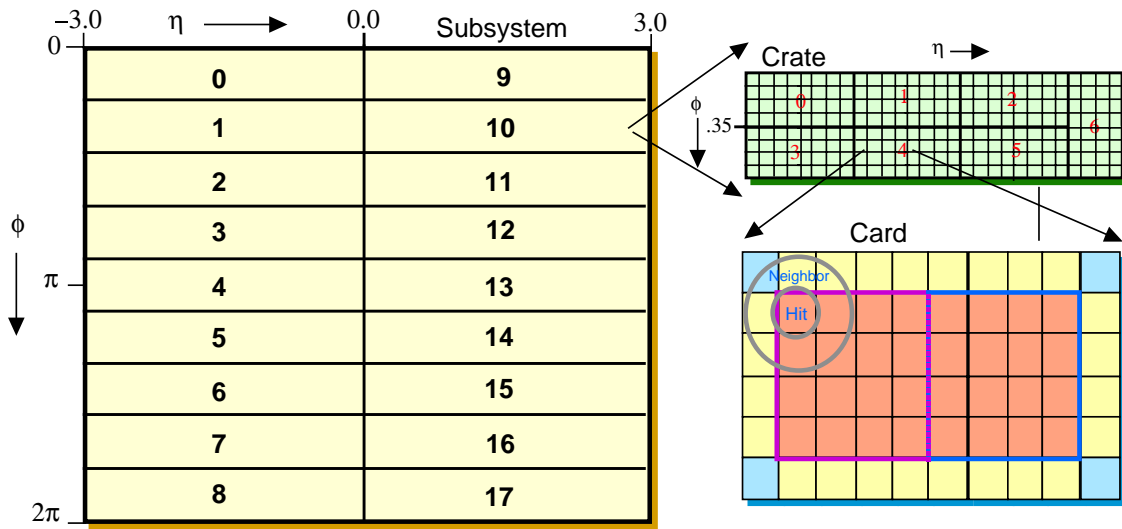
Fig. 5.1: Calorimeter trigger tower mapping for the barrel and endcap region.

The very forward HF calorimeter mapping is shown in Fig. 5.2. 9 HF Cards are used to receive the HF signals and to drive them to the cluster processor crate.

2 CMS HF Calorimeters mapping onto Trigger System HF Crate

Readout segmentation: 36$\phi \times$ 12$\eta \times$ 2z $\times$ 2F/B
Trigger Tower segmentation: 18$\phi \times$ 4$\eta \times$ 2F/B

Fig. 5.2: HF mapping

The mapping for cluster processor crate which serves the entire calorimeter is shown in Fig. 5.3.
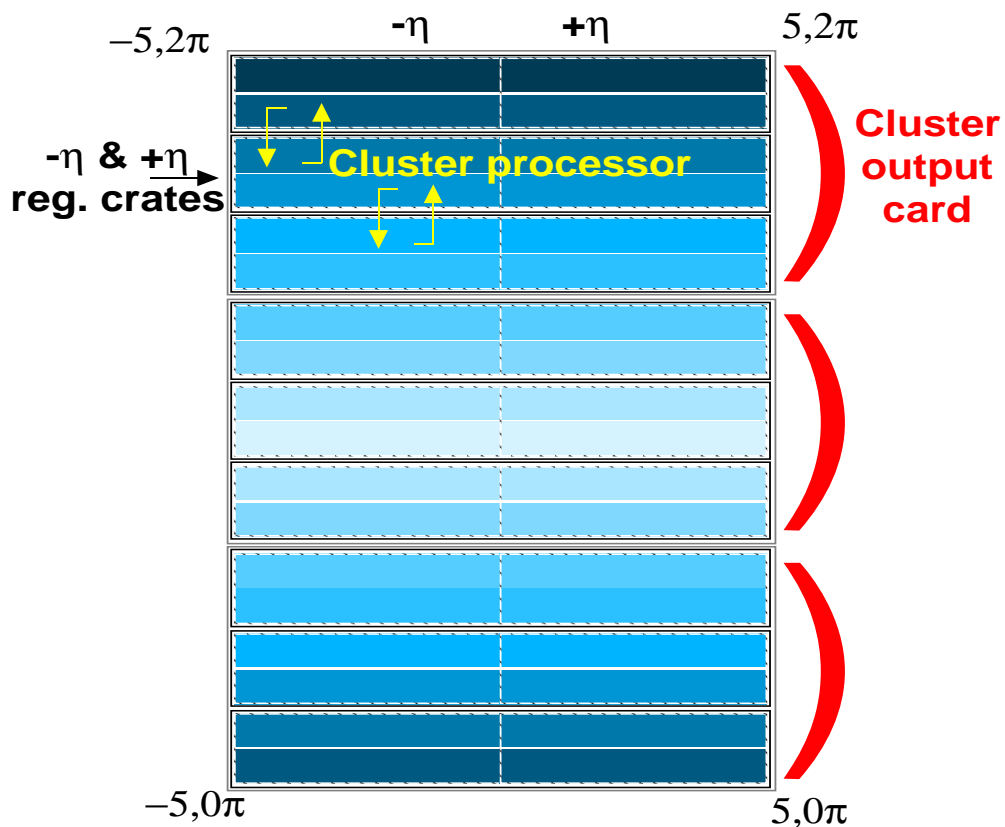
**Fig. 5.3:** Cluster crate mapping

5.3.3   System design issues

Calorimeter trigger system design is dictated by the large number of input channels and the inter-crate sharing required to implement the algorithms. A fine balance is struck between the latest advances in high speed communication and data processing technology and their reliability in large scale parallel processing, to design this system. At the outset we decided to use currently available technologies in which our engineers have expertise.

5.3.4   Crate, backplane and cards

The 20 regional trigger crates will be located two crate pairs in Aleph-style racks. The remaining rack front panel space will be occupied by fans, heat exchangers, and crate power

supplies. Front panels will be used at all card locations to provide an enclosed environment for the chilled air.
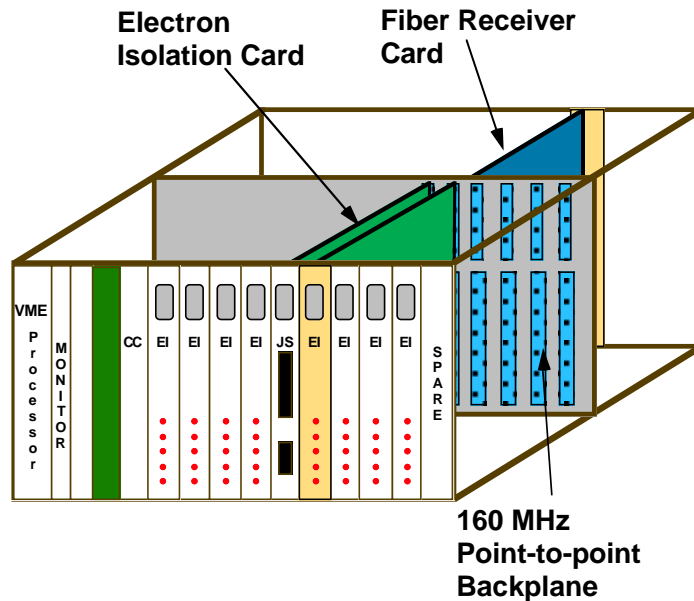
**Fig. 5.4:** Schematic view of a typical calorimeter regional trigger crate.

The crate, shown schematically in Figure 5.4, is based on standard Eurocard hardware. The height is 9U and the depth approximately 700mm, as determined by the front and rear card insertion. The Aleph rack dimension (900mm deep) can handle the crate depth with some reserve for cabling, plumbing, and other services. The backplane is completely custom with a full 9U height. The top 3U is reserved for a 32 bit VME interface. The remaining 6U is used for the high speed data paths between individual cards. The front section of the crate is designed to accommodate 280mm deep cards, leaving the major portion of the volume for 400mm deep rear mounted cards.

Eighteen regional trigger crates use three custom board designs which are dedicated to receiving and processing data from the barrel and endcap calorimeter. There are seven rear mounted Receiver cards, seven front mounted Electron Isolation cards, and one front mounted Jet Summary card for a total of 15 cards per crate dedicated to processing data from the calorimeter. In addition, there are several support cards. The first of these is a readout crate controller and communication module (ROC) selected by the DAQ group. The second is a crate environment monitor (CEM). Finally, the third card will be dedicated entirely to clock distribution and logging status for the cards in the data processing path. Similar design is adopted for HF and Cluster crates. The cards used in the crates offer different functionality desired in those crates.

5.3.5   Crate power, cooling

Power supplies will be mounted in a separate chassis above each crate. They will be located in the forward 280mm of the volume in consideration of the lower heat load (per unit area)

of the forward cards. It is desirable to put the supplies above the crates to place the cards closer to the heat exchangers. Testing is required to determine whether this up and down arrangement will be successful. On board DC - DC converters are used for power distribution.
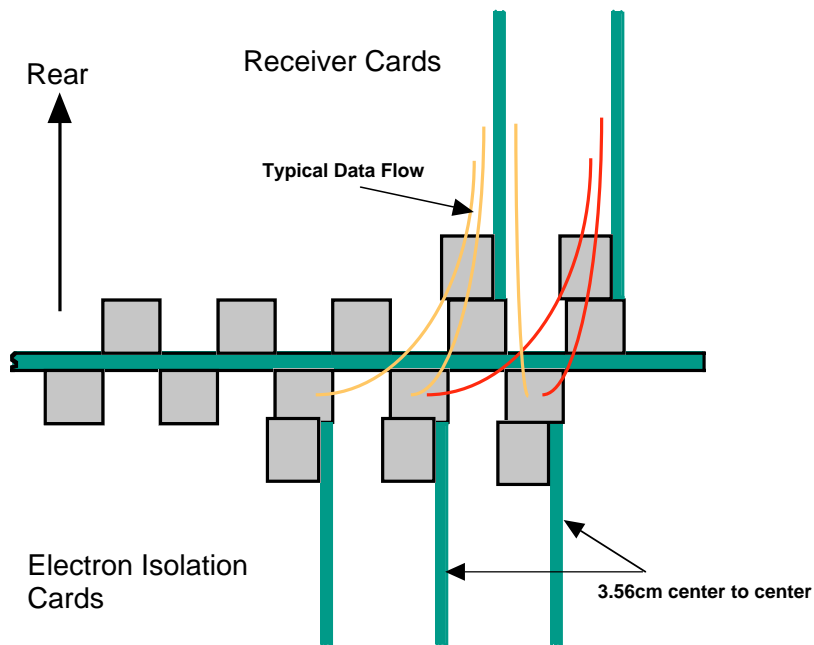
Fig. 5.5: Card spacing.

The front and rear insertion of cards in the data processing section of the crate was chosen to allow greater separation between cards and to provide a more protected environment for the cables connected to the rear mounted Receiver cards. The increased separation promotes better cooling of the cards, and will enable a wider selection of front panel components. The staggering of the slots between front and rear cards, shown in Figure 5.5, is as much a result of the style of connector selected as the fact that piggybacking of connectors is inappropriate in this situation. Almost half of the signals entering the Electron Isolation board come from neighboring Receiver cards. The spacing between cards, in the data processing area, is 3.56cm front or rear, with a 1.78cm stagger front to rear. Therefore, the seven Receiver cards, seven Electron Isolation cards, Jet Summary card, and Clock distribution card occupy 16 slots with a span of only 32.04cm across the front of the crate. The remaining 8.61cm will be allocated to a DAQ Readout card (ROC) (4.06cm), Crate Environment Monitor (CEM) (2.03cm), and a transition region for the change in form factor between the standard and non-standard VME.

5.3.6   Clock and control distribution

The Local Timing, Trigger and Control card (LTTC) will interface to a TTCrx ASIC located on a card in a separate crate. A single TTCrx ASIC is used in a separate crate and signals relevant to regional calorimeter trigger are extracted from it and are distributed synchronously to all processing crates. Within a crate the Clock card will distribute the signals to all processor cards in the crate using differential point-to-point links on the custom backplane.

5.3.7   **Backplane**

The crate backplane is completely custom with a full 9U height. The top 3U is reserved for a 32 bit VME interface. The remaining 6U is used for the high speed data paths between individual cards. The backplane is a 42.52cm x 39.70cm multilayer printed circuit board ~.34cm thick. The other dimensions are fixed by the physical size of the crate. There are on board VME terminations, multiple studs for power supply connections, bypass capacitors, and mounting holes.

The design impedance is 50ï for the lower 2/3 of the backplane which contains all the trigger data paths. This impedance matches the AMP connector impedance and the impedance of the individual boards. The wiring in this section is all point to point, making for a fairly straightforward transmission line. Terminations for these lines are on the receiving cards. The multi-drop transmission line of the VME backplane in the upper 1/3 of the backplane has an impedance of 100ï – before holes and connectors are added. The effective impedance of this section will drop to a little less than 50ï after connectors and trace stubs on the individual boards are taken into account.
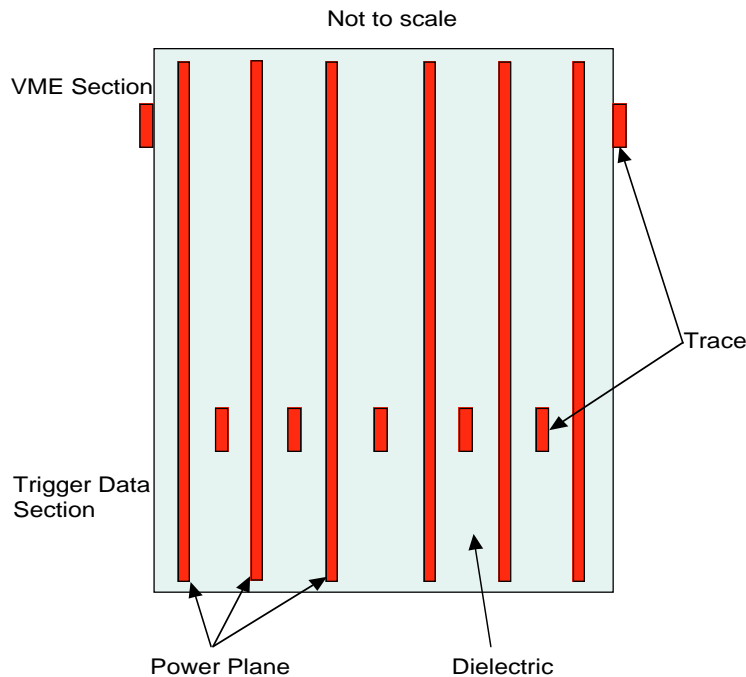
Fig. 5.6: Board stack-up.

In order to ensure there are sufficient wiring channels and to maintain symmetry, five buried layers are used in the trigger data section. A picture of the board stack-up is given in Figure 5.6. An alternating power plane/signal plane structure produces a buried stripline design and surface micro-strip traces. The stripline structure provides good control over crosstalk and general noise immunity. The outside signal layers will be used mostly in the VME section of the backplane. Signals in the trigger data portion are constrained, but not strictly limited to, the buried stripline layers.

5.3.8   VME implementation

The VME specification is written for crates containing no more than 21 cards. In addition, the specification requires that VME signal stubs on individual boards be no greater than 5.08cm in length. The present design for the trigger processor crates contains 20 cards with a VME interface. Reducing the VME interface from two connectors to one has increased the difficulty of staying within the 5.08cm requirement. Special care has been taken throughout the design process to stay within the VME standards.

5.3.9   Backplane data sharing

All signals in the trigger data portion of the backplane will be transmitted on point to point links at 160 MHz. This data rate was chosen because it offers the opportunity to compress the number of data lines on the backplane and in the pipelined data logic by a factor of four and because it should be realizable by available technology. All signals in this section, including clocks, are transmitted point to point. In the present design, all signals are differential.

5.3.10   Inter-crate data sharing

Inter-crate data sharing required for seamless coverage of h-f plane is done using differential ECL signals transmitted at 80 MHz on copper cable. The data is sent from crate-to-crate after any deserialization, phase adjust and linearization, in parallel format. No major effort for resynchronization of signals is expected to be needed.

5.3.11   Implementation of algorithms

Both electro-magnetic and hadronic calorimeter data are needed for electron/photon trigger algorithm implementation. However, the EB, EE data is needed at 7-bit resolution to calculate the candidate energy whereas the HB, HE data can be compressed as it is only needed to veto if the energy profile is not consistent with that of an electron/photon. Look-up-tables on the Receiver cards are used for linearization of energies and to form veto bit and compressed data is driven to the electron identification card. The electron identification card implements the algorithm which includes formation of the candidate electron energy and four identification criteria. These data are used to form ranked isolated and non-isolated electron/photon candidates. These ranked candidates from all electron identification cards in the system are sorted to obtain top 4 candidates of each type seperately and forwarded to the global calorimeter trigger.

The jet and energy triggers need data from all calorimeters. The tau trigger uses the same data but in the central h region only. The input signal processing from the calorimeter is shared by the EM and jet logic upto the phase adjustment phase. After this stage separate look-up-tables are used to linearize the energy and count active towers per region. The Reciver card is also used to make 4x4 trigger tower region sums of ET in both electromagnetic and hadronic calorimeters. The Jet/Summary card recieves ET and active tower counts from all Reciever cards in crate, thresholds the active tower count for each region and stages all data out to the Cluster crate. The Cluster crate also recieves ET from HF towers. The Cluster crate makes overlapping 3x3 sums of these regions with the requirement that the central region is larger than neighbors, spanning the entire h-f plane seamlessly, defining "12x12" sums. These sums are classified as t objects or central or forward jets and separately sorted to find top 4 candidates of each type and forwarded to the global calorimeter

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trigger subsystem. The sum of ET in each 20 degree f strip is also formed and staged to the global calorimeter trigger subsystem for calculating missing ET, total ET and making luminosity monitor histograms.

5.4   Receiver Card

5.4.1   Receiver card overview

The Receiver card is the largest board in the crate. It is 9U by 400mm. The rear side of the card receives the calorimeter data on serial copper cables, and converts from serial to parallel format. The front side of the card contains circuitry to synchronize the incoming data with the local clock, and check for data transmission errors. There are also lookup tables and adder blocks on the front. The lookup tables translate the incoming information to transverse energy on several scales. They are also used to test for Quiet and Minimum Ionization thresholds for each trigger tower. The energy summation tree begins on these cards in order to reduce the amount of data forwarded on the backplane to the Jet Summary card. Separate cable connectors and buffering are also provided for inter-crate sharing.

Each card is designed to receive 32 high speed copper links from the calorimeter readout electronics. Each link transmits either two towers of hadronic or electromagnetic information per crossing for a total of 64 channels from 32 ECAL and 32 HCAL towers per card. The present design for the data uses a 24-bit frame including 18 bits of data and 5 bits of error detection code. The data consists of 8 bits of energy on a compressed scale and one bit of fine-grain information per tower. The error code is sufficient to detect all single and double bit errors as well as many multiple bit errors. The error bits are necessary for error logging and to zero problem channels. The 24-bit word uses 8/10 bit encoding, which implies a 1.2 GHz serial link. The cable length to the calorimeter electronics is estimated at 20 m.
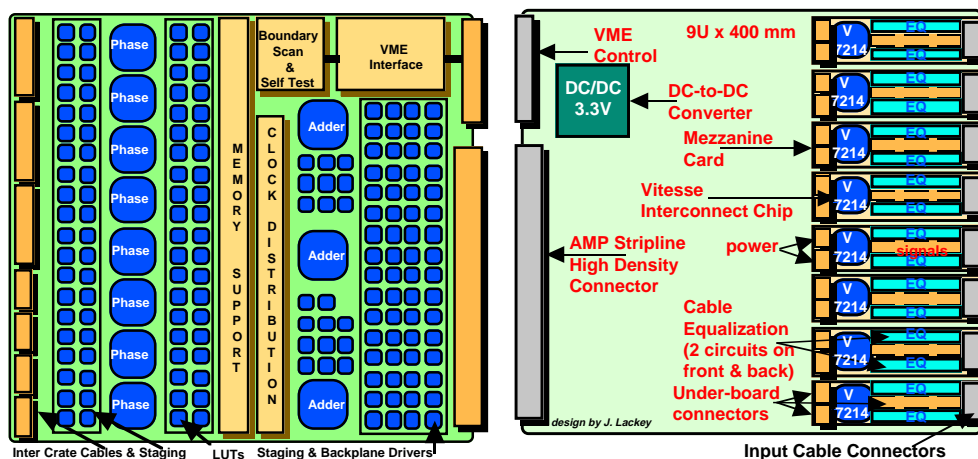

Fig. 5.7: Receiver card views.

The rear side of the Receiver card has serial receivers based on the specifications of the Vitesse 7214 4-channel Interconnect Chip. The design provides for cable/connector equalization and the option of transformer isolation on daughter cards. The front side of the Receiver card

contains the synchronization circuitry followed by the memory look up tables, adder tree and backplane drivers. The outputs of the receivers are not only unsynchronized with the local clock but are also not necessarily aligned to the same bunch crossing. The phase alignment circuitry is contained on an ASIC (Phase ASIC). The Phase ASIC deskews the data, decodes the error detection codes and multiplexes the output at 160 MHz. The Phase ASIC also provides test vectors for board and system diagnostics.

In order to achieve maximum utilization of board space, all the logic following and including the Phase ASIC is run at 160 MHz. There are also four Error Detection Codes (EDCs) associated with the four input channels of each Phase ASIC. After synchronization, each EDC is checked against the data. If an error is detected a single bit is set, one for each incoming channel, and appended to the original EDC code.

Lookup tables are required to translate the information coming from the calorimeter readout electronics, in compressed format, onto the several different scales used by the energy adder tree and the Electron Isolation logic. The Hadronic and Electromagnetic energies are individually translated into eight bits of linear ET with a resolution of approximately 1 GeV. These values are summed to provide total energy in 4 x 4 trigger tower regions of the calorimeter. The summation is performed by an Adder ASIC. Thirty-two towers, in a 4 x 8 array, are processed on each card. The transverse energy for each of the two 4 x 4 trigger tower regions is independently summed and forwarded to the Jet Summary card. These two 13 bit numbers will be multiplexed onto a single set of 13 differential pairs at 160 MHz.

The data required for electron/photon finding algorithm is transferred from the Receiver cards to the Electron Isolation cards at 160 MHz. In order to retain point to point transmission data must be transmitted through separate drivers on separate backplane lines. Every Receiver card shares its data with at most 6 Electron Isolation cards within the same crate. In addition each Receiver card sends some of its data off crate at 40 MHz to two or three neighboring crates. Crate to crate communication is handled by special cables running between the Receiver cards. This distributes the inter-crate buffering among the eight Receiver cards in a crate rather than attempting to put it all on one or two special cards at the ends of each crate.

5.4.2   Serial links

The serial data arriving at the inputs to the Receiver Cards is generated in neighboring Calorimeter Readout crates and received over 20m of cable. We believe this length sufficient for the area containing the HCAL, ECAL, and Trigger racks. All cables will be cut to the same length. Equal length is required by equal timing and a single design for the equalization circuit on the receiving end of each cable.

The serial links are implemented using VSC7214 made by Vitesse which has 4 full duplex channels capable of running between 1.2 and 1.3 Gbaud. It is designed to support Gigabit Ethernet. The data is encoded 8B/10B on the chip. The serializer and deserializer is also included. The parallel data I/O is eight bits wide per channel. 3.3V bias is required for power. Inputs and outputs are low voltage TTL except for the serial data path which is PECL. Power dissipation is approximately 3.3W. The chip comes in a 160 pin PQFP package. We run this chip at 1.2 Gbaud, transferring 24 bits of information per crossing per channel.

The receiver chips are placed on a mezzanine card along with the cable connector and an equalization circuit. The mezzanine card provides a certain amount of power supply isolation and

allows for the replacement of faulty receivers with minimal trauma to the Receiver Card itself. There is also less conflict between the routing requirements of the receiver circuitry and the dense high speed ECL circuitry resident on the front side of the Receiver Card. Mounting the connectors for the serial link on the mezzanine card also avoids a collision between those connectors and the intercrate data connectors on the front side of the main card. Surface mount board to board connectors with locating pins are used to mount the mezzanine cards to the Receiver card. Two of these connectors are dedicated for power from the Receiver card to the mezzanine card. A DC/DC converter on the back of the Receiver card provides the required 3.3V bias.

The Vitesse chip is capable of treating its four channels as a single word. Each channel has a deskewing buffer of ï2 bit times. This buffer can compensate for different delays in cable routing and small phase drifts between transmitting and receiving ends. The four channels can also be treated independently. The data is transferred from the mezzanine card to the Phase ASIC mounted on the front side of the Receiver Card shown in Figure 5.7.
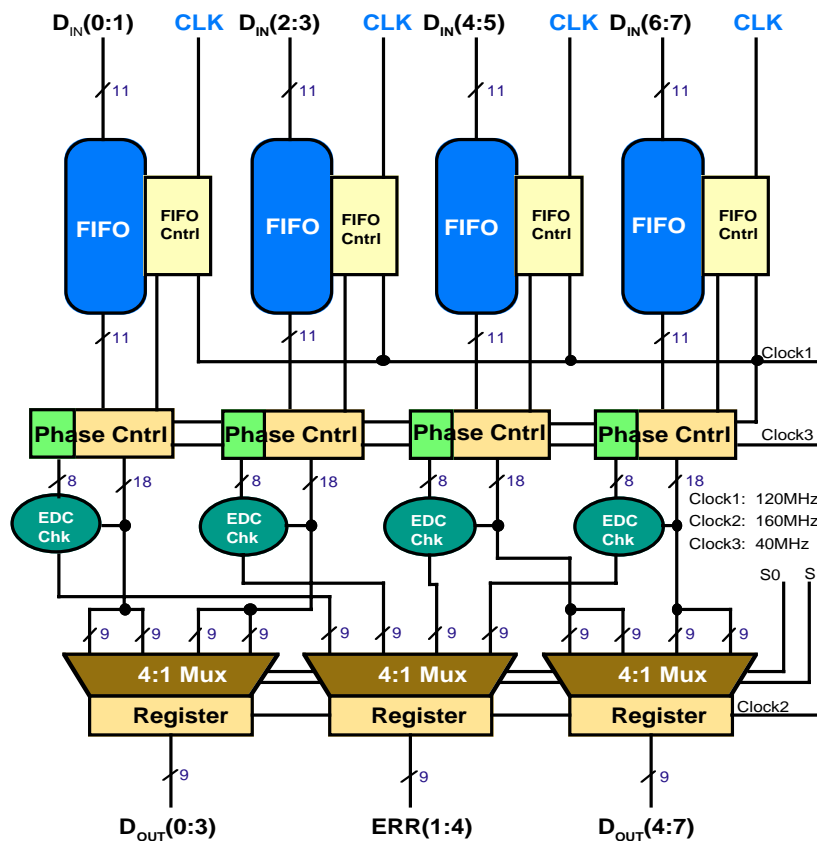
5.4.3 Phase ASIC

Fig. 5.8: Phase ASIC block diagram.

The block diagram of the phase ASIC is shown in Figure 5.8. This ASIC receives four channels of two tower data, multiplexed onto two output channels. Each of the four input channels is comprised of 8 bits of data, from the 10bit/8bit decodes, and 3 bits of status. One of the three

status bits is an error bit set by the receiver as a result of several illegal conditions that might occur. The remaining two status bits can either indicate the current operating mode of the receiver chip or qualify the error bit. Each channel's parallel output is arriving at 120MHz. Three frames, or 24 bits of data per channel, complete the data transfer for a single bunch crossing. The four channels, taken together, produce 44 bits of information every 8.33ns. These 44 bits are clocked into the input stage of the Phase ASIC using the clock recovered from the VSC7214.

The input stage of the Phase ASIC is a 44 bit wide FIFO that is six frames deep. The FIFO can accommodate minor phase shifts between the transmitter and local clocks and is kept approximately half full. The FIFO is followed by a circuit which establishes the proper phase between the incoming data and the local bunch crossing clock. This circuit makes use of status information from the VSC7214 to set the final phase. Once properly phased, the data and error bits can be separated into 18 bits of data (two channels) and 5 bits of Hamming code.

The Hamming code is recomputed from the data and compared with the received Hamming code bits. The data leaves the Phase ASIC in two data channels, 9 bits apiece, and one 9 bit error channel. The error bits are made up of the transmitted EDC, a subset of the status bits from the VSC7214, and an overall error indiactor. The status bits from the VSC7214 provide sufficient information to determine the state of the serial links at any point in time.

As we have four input channels, each handling two towers per crossing, the two output channels produce four towers of information per crossing. The outputs are clocked at 160MHz. This rate was chosen to match the processing circuitry on the rest of the board. By running the Receiver Card at 160MHz we realize a substantial savings in the amount of logic required to process the data.

The last storage element of the Phase ASIC will be implemented as a loadable counter. During normal operation the counter will be loaded with data each 6.25ns. During testing the counter can be reset and enabled to count synchronously with the rest of Phase ASIC outputs. The counter outputs will address the look up tables just as detector data would. The combination of these counters and look up tables can be used to provide any data pattern necessary to test the remainder of the Trigger Processor system. The error outputs will be idle during testing.

The Phase ASIC will have a JTAG controller and scan cells on all the outputs. Total signal pin count, including JTAG should be around 80. The technology for the Phase ASIC is expected to be the same Vitesse 0.6 micron GaAs process as used for the Adder ASIC described below.

5.4.4 Link error handling

Error counting and reporting.

5.4.5 Look-up-tables

Lookup tables are required to translate the information coming from the calorimeter front end electronics, in compressed format, onto the several different scales used by the energy adder tree and the Electron Isolation logic. The Hadronic and Electromagnetic energies are individually translated into eight bits of linear ET with a resolution of approximately one GeV. The processor on the Electron Isolation (Electron ID) card requires electromagnetic and hadronic transverse energy with several dynamic ranges. The reference tower needs 7 bits of electromagnetic transverse energy with a resolution of .5 GeV. Additionally, a HAC/FG Veto bit which

characterizes the tower based on comparison of electromagnetic to hadronic ET and fine-grain profile veto that accompanies each EM tower input is formed using another look-up-table. The corner towers for each 4 x 8 region are reduced to 3 bits with a resolution of .5 GeV. To guard against wrap-around when the 3 bit electromagnetic values and 4 bit hadronic values are generated, any value greater than the maximum of the bit range is set to the maximum three or four bit value. Spare bits in these memories are used for thresholding ETs to determine number of active towers. These towers are counted to later determine tau like energy deposits. A block diagram of these LUTs is shown in Figure 5.9.
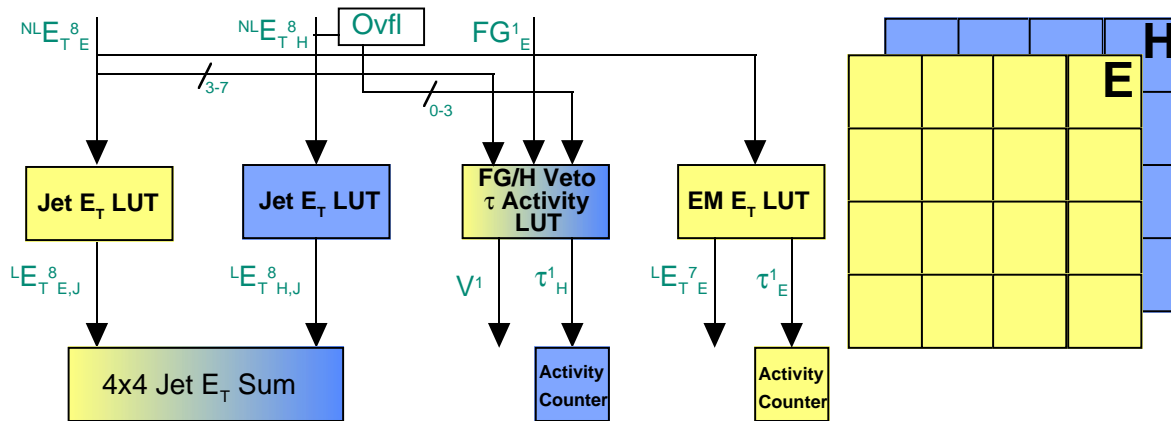

Fig. 5.9: A block diagram of the Receiver Card LUTs.

With a 6.25 nsec period the memories must have access times less than or equal to 3.0 nsec in order to provide margin for the usual board propagation and setup and hold times. Data is downloaded to the memories and read back through the VME interface. This requires support circuitry located in the area of the memory chips. The data inputs to the memories can be tied in parallel for writing the chips, but all the address lines (128) need to be individually buffered. The buffering is located near the memory in order to maintain short board traces in the high speed section of the logic. Reading the data out of the memories back to the VME interface requires buffering for all the data output lines. For example, this buffering is provided by an 8:1 multiplexer within each Adder ASIC.

5.4.6   Energy sums

The beginning of the energy summation tree is on the Receiver card. The transverse energy for each of the two 4 x 4 trigger tower regions is independently summed and forwarded to the Jet Summary card. Though the input values at the top of the adder tree have only 8 bits of range, the adder tree has been designed to handle a dynamic range of 10 bits for either positive or negative values. This implies an overflow at approximately 1000 GeV. The exact value will depend on the resolution required of the input transverse energy for other trigger functions. Any overflow (or underflow) generated as the result of an arithmetic operation (AOV) will stay in time with the data and be ORed with any other overflow that might have occurred in the same crossing. All values are handled as 11 bit 2's-complement numbers.

A second overflow condition can also occur. The value sent to the trigger processor from the calorimeter front end electronics may be at the highest possible count. The lookup tables will be programmed to output FFH for this particular input. This output code is recognized, at the top level of the adder tree, as indicating an input data trigger tower overflow (TOV). It is handled much like the arithmetic overflow in that is it ORed with other TOV overflows and passed down the tree in time with the data that generated it. If the overflow is caused by a hardware failure, the lookup table can be re-written to zero out the affected channels. The arithmetic and tower overflow bits are handled separately through to the end of the adder tree. TOV recognition can be disabled. These summations are made using an Adder ASIC.

5.4.7   Adder ASIC

The adder ASIC is implemented as a 4-stage pipeline with eight input operands and 1 output operand. There are only three stages of adder tree, but an extra level of storage has been added to ensure chip processing is isolated from the I/O. We have determined that the ASIC must work reliably at a clock period of 5.0 nsec in order to ensure safe operation at an in-circuit period of 6.25 nsec.

This ASIC uses 4 bit adder macro cells to implement twelve bit wide adders. Eleven bits are wired, left justified, to each operand of an adder. The LSB of each adder will be internally set to ZERO. The MSB is treated as a sign bit. Therefore, although the adder tree may be constructed from three 4 bit adders, the width of the operand data paths has been limited to eleven bits. An Adder ASIC chip is designated as 'master' if it is in the top rank of the adder tree and as 'slave' if it is further down. Masters can generate Tower overflow (Tov), but slaves can only propagate Tov. Both masters and slaves can generate and propagate arithmetic overflow/underflow (Aov). These bits are appended to each input and output operand, making all operands 13 bits wide. Tov becomes the twelfth bit of the output result and Aov the thirteenth bit. The data outputs of the chip are forced to 3FFH when either an overflow or underflow occurs.

The top of the adder tree is composed of four 12 bit adders and includes the logic required to detect and propagate Tov and Aov. The Tov generate circuitry is a filter designed to detect the input code 3FFH. The Aov generate circuitry examines the sign bits of the input operands and the results operand, together with the carry out, to determine whether or not an overflow or under flow has occurred. All eight of the Tov bits are ORed together and all four of the Aov bits are ORed together to form two separate overflow bits that are forwarded with the data in the pipeline. Edge triggered registers are used to store the results for the next stage of the adder tree. A block diagram of the Adder ASIC is shown in Figure 5.9.
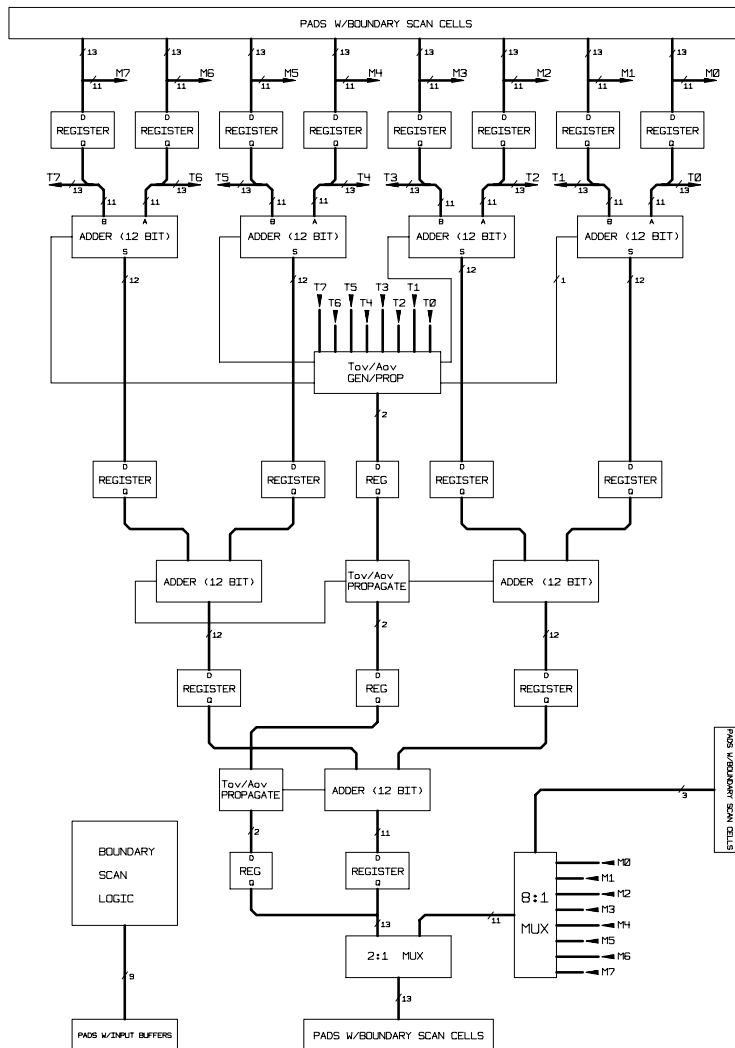
Fig. 5.10: Block diagram of the Adder ASIC.

The second stage contains two more 12 bit adders and includes the logic needed to propagate Tov and to detect and propagate Aov. From this point on, Tov is forwarded down the pipeline from register to register. Aov is generated in the same manner as in the first stage and the resulting two bits are ORed with the Aov from the previous stage. Edge triggered registers are used to store the results for the next stage of the adder tree.

The third stage contains the final adder as well as a continuation of the Tov/Aov circuitry. The register at this level is the last storage element before the ASIC output. If either Tov or Aov have been detected, the output operand stored in this register has the value 3FFH. Tov and Aov are stored along with the operand. Adder Tree ASICs further down in the tree are designated "slaves" and are blocked from using the operand 3FFH to generate Tov. Thus we retain the identity of the tower overflow bits through the entire tree.

The last register is presented to one input of a 2:1 multiplexer before leaving the chip through the boundary scan cells and pads. The other side of the multiplexer is fed by an 8:1

multiplexer which passes any one of the eight input operands, less the two overflow bits, to the output of the ASIC. This feature was provided to minimize the external logic needed to read back the values of the lookup tables that feed the first stage of the adder tree logic.

The chip also contains boundary scan support described later. The Adder ASIC implementing all the above features was manufactured by Vitesse in 0.6ï GaAs technology and is packaged in a 195 pga. It requires approximately 4 W of power.

5.4.8   Backplane drivers

Thirty-two towers, in a 4 x 8 array, are processed on each Electron Isolation board. Data from twenty-eight neighboring towers is required to determine isolation for towers on the edge of the 4 x 8 region. Data is transferred between the Receiver card and the Electron Isolation card at 160 MHz. In order to retain point to point transmission, data going to a neighboring Electron Isolation board must be transmitted through separate drivers on separate backplane lines.

Every Receiver card shares its data with at most 6 Electron Isolation cards within the same crate. In addition each Receiver card sends some of its data off crate at 80 MHz to a maximum of three neighboring crates. Crate to crate communication is handled by special cables running between the Receiver cards. This distributes the inter-crate buffering among the eight Receiver cards in a crate rather than attempting to put it all on one or two special cards at the ends of each crate. The maximum amount of intercrate information that can enter and leave a Receiver card is carried on 120 twisted pair cable.

The order in which the data is transmitted to the Electron Isolation card is important. Since connector pins are at a premium, it is necessary to ensure that all lines have useful data for each of the four 6.25 nsec cycles making up a 25 nsec crossing. Board space is also at a premium, so it is necessary to limit the amount of circuitry committed to staging the data for the backplane. The most efficient way to satisfy these goals simultaneously is to pay careful attention to the order of cabling between the detector front end electronics and the input channels of the Receiver card. This, in conjunction with the multiplexing of data in the Phase ASIC, handles most of the data staging. Some of the data transmitted between the Receiver card and Electron Isolation (Electron ID) card comes from neighboring crates. This data has been delayed in time with respect to the data originating on the local Receiver card. The local data must be delayed to allow the shared data to "catch up". This function will be incorporated into an ASIC that includes the differential drivers for the backplane data and the JTAG boundary scan.

5.4.9   Boundary Scan ASIC

Boundary Scan ASIC has several functions. Firstly, it provides control for board level boundary scan functions. Secondly, it provides drivers for sending data over the point-to-point links on the backplane and inter-crate cables. Thirdly, it provides simple algorithms needed for manipulating data, e.g., to reduce the corner tower data from 7 bits to 3 bits while ensuring that the setting of any upper bits in input saturates the 3-bit scale. This ASIC is also implemented in Vitesse 0.6 μm GaAs technology. (Packaging and power)

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5.5   Electron Identification Card

5.5.1   Overview

Electron Identification algorithm within each 4x8 trigger tower region is performed on a smaller 240mm deep card. Data for thirty-two central towers and twenty-eight neighboring towers is required to determine isolation for towers on the edge of the 4 x 8 region. This card receives linearized transverse energy on 7-bit scale for ECAL and 4-bit scale for HCAL and ECAL fine-grain bit from corresponding receiver card. It also receives neighbor tower data from up to three other receiver cards in the crate. Neighbor crate data is transferred through the receiver cards where it undergoes any realignment of phase. The algorithm which finds isolated and non-isolated electron/photon candidates is implemented in an ASIC. Candidate with highest ET of both types in each of the two 4x4 regions covered by the card are transmitted to the Jet/Summary card.

5.5.2   Electron Isolation Card Input

All data received by the Electron Isolation card comes from local Receiver cards in differential mode. Terminations for the lines will be on the cards rather than the backplane. Each card processes 32 towers of electromagnetic and hadronic information organized in a 4 x 8 array. Data is also required from the neighboring 28 towers to determine isolation on the boundaries of the 4 x 8 region. The 306 input lines required by the Electron Isolation card are serviced by a 340 pin AMP stripline data connector. The additional pins beyond 306 will be used to forward the results to the Jet Summary card and to input clock and control information. As in the case of the Receiver card, the top part of Electron Isolation card will use a 128 pin DIN connector to interface to a 32 bit VME bus.

5.5.3   Electron Isolation ASIC
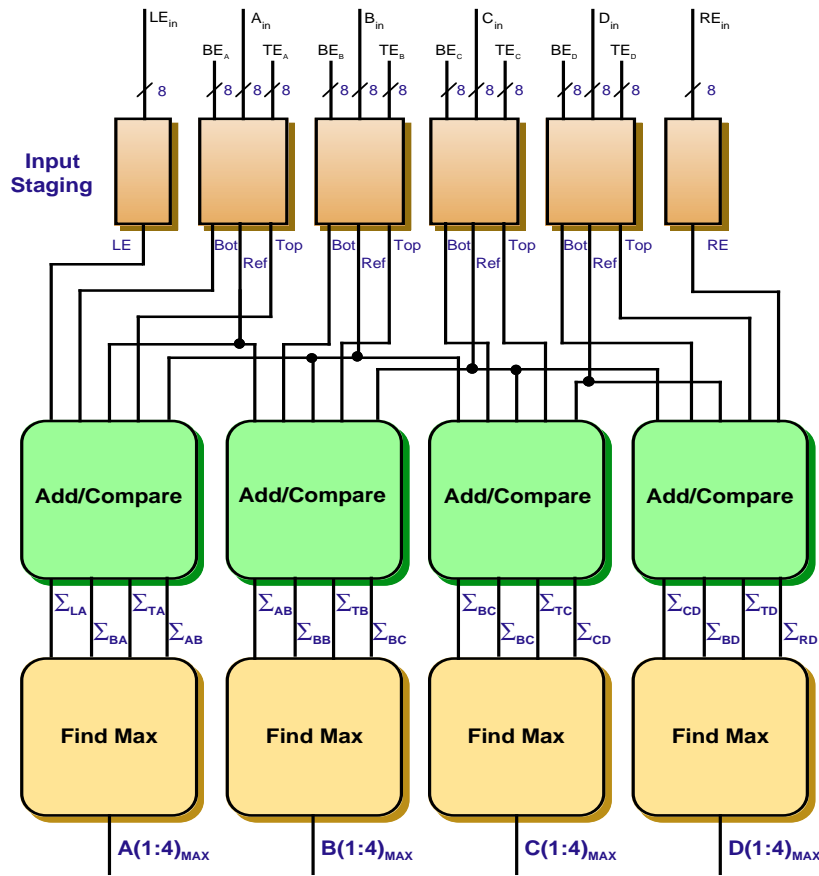
Fig. 5.11: Electron Isolation ASIC block diagram.

The Isolation ASIC, shown in Figure 5.11, handles four electromagnetic energies on an 7 bit scale along with the corresponding HAC/FG Veto bit, every 6.25 nsec. These inputs are designated as Ain, Bin, Cin, and Din in the figure. Nearest neighbors are also included in the data flow. During the first cycle of every crossing the four neighboring energies (TEA, TEB, TEC, TED) from the adjacent 4 x 4 region (top) are also be strobed into the ASIC. The neighbors along either edge of the 4 x 4 region (LEin, REin) are also included, two at a time (left and right edges), during each 6.25 nsec period. Finally, the last cycle strobes in the four neighboring towers of the bottom edge (BEA, BEB, BEC, BED). Thus, in one bunch crossing time, a total of 36 towers are clocked into the Isolation ASIC.

Separate inputs are used to clock in the top and bottom neighboring towers in order to avoid unfavorable routing or extra components on the board due to board level multiplexing. The top and bottom neighboring edges require a total of 2 x 4 x 8 = 64 input pins. The central region needs 4 x 8 = 32 input pins, and the left and right edges need 2 x 8 = 16 pins. The total number of data inputs is 112 pins, for 36 towers of information. In addition pins are allocated for three bits of EM threshold, reset, and clock inputs. All signal I/O, with the exception of the clock, is single-ended. The single maximum two tower sum for the full 4 x 4 region is obtained by comparing the

four values output by the Find Max block to determine the largest of the four values in each 6.25 ns time frame and retaining the largest of four values generated over the four 6.25 ns cycles required to process the region.

The main data flow of the Isolation ASIC processes the data through three separate blocks. The purpose of the first of these, the Input Staging, is to receive the data at the time when it is available and change the time relationship to one suitable for the processing that follows. At the beginning of a crossing, the first row of the 4 x 4 array is available, along with the top edge. The signal Cycle 1 selects the Top Edge input on the right hand multiplexer. After the first 6.25 nsec clock, the first rank of registers contain one of the towers in the 4 x 4 array (a reference tower) along with its top neighbor. The leftmost register in the top rank is undefined at the beginning of the sequence. After a second clock cycle, the reference tower is in the middle register of the bottom rank of registers and its top neighbor is in the right hand register. The left-most register in the bottom rank contains the next successive reference tower, as does the middle register in the top rank. This value is the bottom nearest neighbor for the first reference tower. The sequence continues through to the cycle where the last reference tower in a column of 4 towers is clocked into the middle register in the bottom rank. During the same cycle the Bottom Edge data is available from the neighboring card. It is clocked into the bottom left register during Cycle 1 at the beginning of the next sequence.

Once the pipeline has been filled, data will continue to be output from the Input Staging block four towers at a time each with their corresponding top and bottom neighbor. The left and right neighbors are either the adjacent reference towers in the 4 x 4 array or the left and right columns of data from neighboring boards.

The Input Staging block places each reference tower and its neighbors in the same time frame. The remaining blocks in the chip can now handle the processing in parallel. The function of the Add/Compare block is to form four sums between a reference tower and its top, bottom, left and right neighbors. At the same time the sums are being formed, four compares are made to determine for each pair of towers whether the reference tower is larger than or equal to its neighbor ("equality check"). When a reference tower and its neighbor satisfy the "equality check" the sum of the pair is enabled to the Find Max block. When the sum is disabled, a value of zero is passed on to the next block. If the adder has overflowed (carry out equals one) the result

The next to last stage in processing the electromagnetic information is the Find Max block. The four sums are presented, in parallel, to two comparators. The outputs of these comparators are used to select the maximum of each pair which are placed in intermediate storage. These two maxima are presented to a single comparator during the next clock cycle. The output of this comparator is the maximum two tower sum for an individual reference tower. The single maximum from the original four values is stored in a register. The HAC/FG Veto, neighbor HAC/FG Veto, and neighbor EM Veto bits described below are stored with each of these sums. A final stage of logic sorts through all 16 maxima generated over a bunch crossing time and places that value, along with its Vetos, on the outputs of the ASIC. The total latency for the electromagnetic data path is 12 x 6.25 nsec or 3.0 bunch crossing times.

Three isolation criteria, central tower HAC/FG Veto, HAC/FG neighbor Veto and EM Veto computations are performed within the ASIC in parallel with the max two tower logic described above. A tower's HAC/FG Veto enters the ASIC in the same time frame as the 7 bit Et information. The same staging circuitry used to equal time the neighbor Et information for a single

reference tower is also used to put the HAC/FG Vetos into the proper time sequence. Once all eight neighbors are timed in an eight way OR is performed to arrive at the HAC/FG neighbor Veto.

The EM neighbor Veto requires a little more processing than that used on the HAC/FG neighbor Veto. The Et information has already been timed in by the staging circuitry. It is presented to a bank of comparators where each value is compared against the same three bit threshold. The single bit results from each of the compares is passed on to a large OR - AND array. The ORs check that each group of five towers, centered on one corner of a reference tower, are all below threshold. The ANDs gather the four results from the ORs for each reference tower and form the AND. If any one corner of the five tower ORs has a value of zero, the AND (EM Veto) will be zero.

The results from the EM Veto logic are produced ahead of the two tower sums and must be delayed within the ASIC by two clock cycles. This Veto, along with the HAC/FG neighbor veto and HAC/FG veto, is appended to the two tower Et sum before it enters the Max tower circuitry. The result from the Max tower block has the correct Veto information associated with it and all 10 bits are placed on the outputs of the Electron Isolation ASIC.

We have implemented the same controller and instruction decoder for boundary scan as used in the Adder ASIC. All ASICs in the Level 1 trigger processor will have compatible boundary scan circuits.

5.5.4   Electron Isolation Card Output

Isolated and non-isolated candidates formed using the ET values and three veto bits output by the EI ASIC for each of the two 4x4 regions handled by the electron isolation ASIC are compressed to 6-bit rank using a look-up table. These 6 bits and a single position bit to distinguish the two regions handled by the card are transferred to the Jet/Summary card at 160 MHz over the backplane.

5.6   Jet/Summary card

5.6.1   Input

Jet/Summary card receives 4x4 trigger tower energy sums, active trigger tower counts and MinI bits from all Receiver cards in the crate, and, isolated and non-isolated electron/photon candidate energies from all Electron Identification cards in the crate.

5.6.2   Electron/photon processing

The isolated and non-isolated electron/photon information from each of the 14 regions covered by the Jet/Summary card are received directly into SORT ASICs. After assigning the position bits the top four ranking isolated and non-isolated electron/photon candidates are determined keeping track of their 4 bit position information. The details of sort logic are described below.

5.6.3   Sort ASIC

The Sort ASIC will have differential inputs so that data may be received directly from the backplane. This will reduce the amount of receiver logic on the Jet Summary card and allow us to use the JTAG Boundary Scan built into the ASIC to do backplane testing and to set up test data for the board itself. In addition to the data inputs we need three bits of positional information to tag the location of the 4 x 4 region providing each piece of data. These bits will be differential as well so that we may use the Sort ASIC in another application described below.
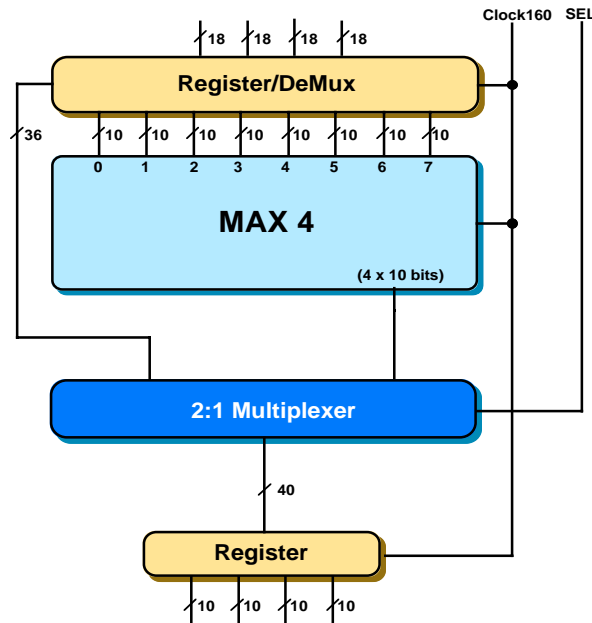
Fig. 5.12: The Sort ASIC block diagram.

The Sort ASIC is designed to find the four largest of eight 6-bit values. Six bits is sufficient to handle both the ET sums and the electron candidates. Figure 5.12 is an illustration of the major functional blocks that make up the ASIC. Rather than try to design an ASIC that will handle eight 6-bit operands in parallel, it was decided to shift the data in, four operands at a time, over two 6.25 nsec cycles. The electron candidates come from the Electron Isolation card is two groups of two. The first group will be the Isolated electrons, and the second group will be the Non-isolated electrons. The two groups are separated in time within the ASIC with the results of a sort appearing every 12.5 ns. In the case of the Et energy sums, the two regions are received from each Receiver card by the Sort ASIC in successive 6.25 ns cycles. The results from this sort appear at the output of the ASIC once every bunch crossing.

Two ASICs are required to receive the data from the Electron Isolation cards and four more are required to handle the data from the Receiver card. Each pair of ASICs generates eight values. These eight values will be muxed together in pairs and each fed into a single Sort ASIC to produce the final set of four max values. The outputs from the Sort ASIC are the four largest 6 bit values along with 4 bits each of positional information. These results are single-ended.

The algorithm implemented within the Sort ASIC is based on a simple rotation of operands. The eight operands are divided into two groups of four. The operands are compared in pairs between the two groups, with the larger of the two taking over the position of the left hand member of the pair. This comparison is performed in four stages with a rotation of compared pairs occurring between each stage. By the end of the fourth stage a sufficient number of comparisons have been made to ensure the four largest values are in the left-hand group. In order to save steps, and thus minimize the total latency, these four values are not placed in any rank order. The final four values, produced by the Calorimeter Global Trigger Processor, are ordered during the final sort.

The first functional block of the Sort ASIC is the Register/DeMux. The main purpose of this block is to provide storage for the incoming data to isolate it from board propagation delays. It is also stages two cycles of 4 operands into a parallel data path of 8 operands. In addition a single bit of position information is appended to the three bits of positional information entering the ASIC along with the data. This bit is appended, if enabled, during the second cycle of data input. The addition of this bit will be enabled for the Sort ASICs in the second level of sort.

The next block in the sequence is the MAX4 block. The MAX4 block is made up of four Compare/Select blocks. Each of the four blocks is different from its neighbor in that each has one of the four stages of pairing hardwired in the circuit. The Compare/Select block performs all four compares in parallel. Ten bits arrive and leave at the inputs and outputs. The top four bits are the positional information mentioned above. They are carried along with the data through the 2:1 multiplexers. The bottom six bits (raw data) are used by the compare to drive the select lines of the multiplexers. Each pair of multiplexers has the same operand wired to opposite inputs. The results from the compare force the left hand multiplexer to store the larger of the two values and the right hand multiplexer to store the smaller of the two. After one 6.25 nsec clock cycle the eight operands have been reorganized with the larger of each pair of values stored in the registers in the left hand column.

During the next three 6.25 nsec clock cycles the data is passed through the remaining three Compare/Select circuits. Only the left four operands are saved at the end as they contain the four maxima of the original eight operands. The output of the MAX4 block is sent on to a 2:1 Multiplexer. The Multiplexer is used to bypass the sort circuit. This feature is useful in handling the energy sums from the Receiver card. The input data requires two cycles to enter the ASIC. The sorted results only require one cycle to exit the ASIC. The multiplexer is used to pass the input data (two cycles worth) directly to the outputs of the ASIC before the sorted information is available. The two input operands are sent to memory look up tables and generate Ex and Ey values for each 4 x 4 region. They also are used in the Et adder tree to complete the energy sum for the crate. When the sorted values are available they are received, along with data from the second Sort ASIC of the pair, by a third Sort ASIC. The third ASIC completes the sort of the original 16 values.

In the case of the sort of electron candidates the inputs are used in all four cycles. The sort reduces data so that only two cycles are needed for the output data. One cycle produces four Isolated candidates, the other produces four Non-isolated candidates. Two Sort ASICs produce eight values (Isolated or Non-isolated) in the same cycle at 80 MHz. These values are Muxed at 160 MHz into a third Sort ASIC. The output from this last ASIC produces four sorted Isolated electron candidates and four Non-isolated electron candidates on two cycles every bunch crossing.

5.6.4 4x4 E_T sums

The Jet/Summary card receives 10-bit 4x4 ET sums and 1 overflow bit for each of the 14 regions covered by the crate. These data are multiplexed for transmission at 80 MHz to the Cluster Processor crate for finding jets and τ candidates.

5.6.5 τ veto bit

The Jet/Summary card receives 2-bit ECAL and HCAL activity counts for each of the 14 regions covered by the crate. If the trigger tower activity counts from ECAL or HCAL are greater than two the 4x4 region τ veto bit is set ON. There is enough room on the card to implement this algorithm in discrete logic components. The logic will be used at least twice per crossing to determine τ veto bits for all 14 regions handled by this card.

5.6.6 MIP bit handling

HCAL trigger primitives generator from HB and HE regions send on the serial links, in addition to tower ET, one bit characterizing the energy profile. This bit is expected to be set ON for towers with ET consistent with passage of a minimum ionizing particle through it. These fine-grain bits from each 4x4 region are ORed on the Receiver Card to obtain a single MinI identification bit. Two bits corresponding to the two 4x4 regions covered by each Receiver Card are forwarded to the Jet/Summary card.

5.6.7 Quiet bit generation

In addition to the MinI identification bit, the Jet/Summary card determines quiet regions by thresholding 4x4 energy sums it receives from the Receiver Cards.

5.6.8 Output Processing

It sorts the electron/photon candidates and forwards top 4 isolated and non-isolated electron/photon candidates to the global calorimeter trigger crates on copper cables. The Jet/ Summary card forwards the MinI and Quiet bits from the 14 regions handled by it to the Global Muon trigger.

5.7 HF Crate

The HF crate handles data from HF calorimeter which covers the regions -5<h<-3 and 3<h<5. For this calorimeter there are 2 (+Z/-Z) x 4 (h) x 18 (f) trigger towers each corresponding approximately to the same size as 4x4 region sums of the HE. The HF crate has 9 HF cards which combine a part of the functionality of the Receiver and Jet/Summary cards in the 18 normal crates. Each of the 9 HF cards handle 40 degree segment in f and both ends of the calorimeter. These cards receive data on Vitesse VSC7214 based Cu serial links using 2 mezzanine cards, adjust their phase to be aligned with rest of the calorimeter and provide look-up-tables to linearize the data just as it is done in the regular Reciever card. The data is then staged out to the Cluster crate on two 34-pair connectors as is done on the Jet/Summary card. The linearized data from HF is on 8-bit scale which is to be programmed the same as the jet ET look-up-tables on the regular Reciever card.

5.8   Cluster Crate

The eighteen regional trigger crates and the single HF crate send 4x4 trigger tower E_T sums to a single Cluster crate where 12x12 overlapping E_T sums are calculated to form jet and tau candidates. The Cluster crate consists of 9 Cluster Processor cards each receiving data from two regional crates and one HF crate on six 34-pin cables. The data from two regional crates covering $|\eta|<3$ and a 40° bin in ϕ consist of 10 bit E_T and 1 τ veto bit per 4x4 region are received on 80 MHz parallel differential ECL links by each Cluster Processor card. The same technology is used to recieve data from HF crate covering -5<h<-3 and 3<h<5. In order to seamlessly cover the $\eta-\phi$ plane these data are exchanged on a custom point-to-point backplane similar to the backplane of regional trigger crates. The Adder ASICs are used to make E_T sums of 3x3 trigger tower regions centered around each trigger tower region. The central 4x4 region E_T is required to be greater than the neighbors to the right and bottom, and to be greater than or equal to the neighbors on the left and top. Each Cluster Processor card produces 36 such "12x12" E_T sums. These candidates are divided into central and forward region. The central 28 sums are classified as τ candidates if they are not vetoed by any of the nine 4x4 regions contained in it. The remaining candidates are classified as central jets.

5.8.1   Jet and τ sorting

The central and forward jet and t candidate E_T sums are compressed using a LUT with a 6-bit rank and are also associated with 5 bits defining their position on each Cluster Processor card. These candidates are separately sorted based on their rank while keeping track of their position bits to find the top four candidates of each category. The SORT ASIC described earlier is used for this operation. The top four candidates of each type are staged to the Cluster Output card for sending them to the Global Calorimeter trigger. The Global Calorimeter trigger system continues the sort tree to obtain top four candidates over the entire $\eta-\phi$ plane. Additionally, it also thresholds these candidates to count numbers of jets above programmable thresholds in various h regions to provide triggers for events with more than four jets.

5.8.2   Missing and Total E_T sums

Four ET sums per Cluster Processor card corresponding to two 20° ϕ bins served by it covering $-3 < \eta < 0$ and $0 < \eta < 3$ seperately are calculated using Adder ASICs. Resulting 10-bit ET and overflow bit for each of these four strips are passed to the Cluster Output card for sending them to the global calorimeter trigger system where they are used for both missing and total E_T sums and luminosity monitoring.

5.8.3   Connection to global calorimeter trigger

Data is sent to global calorimeter from 18 regional crate Jet/Summary cards on 3 34-pair cables in parallel format at 80 MHz. In order to provide low cost and reliable solution that works on cable runs upto 20 m in length, we use ECL diffrential signals in paralle. This data includes, top 4 isolated and non-isolated electron/photon candidate ranks and position amounting to 10 bits per candidate and muon isolation and identification bits for 14 4x4 regions handled by the card. The muon data is simply passed on to global muon trigger by the global calorimeter system. Twenty four such 34-pair cable at 80 MHz are used to transfer 36 counts each of central, forward and tau

jet objects and ET sums, with 11-bit datum each, from the Cluster crate to the global calorimeter trigger subsystem.

5.9   Error Detection

5.9.1   System test errors

Automatic power up test setup. LEDs, diagnostics etc.

5.9.2   Boundary scan

The chip also contains boundary scan support. The ASIC boundary scan implementation, along with a proper board level implementation should provide full testing capability of the ASIC while it is in circuit. The boundary cells can also be used to verify circuit integrity (shorts, opens, and stuck at one/zero) at the board level. IEEE standard 1149.1 has been strictly adhered to in order to ensure compatibility with other ASIC and board level boundary scan controllers. The full JTAG controller and a major subset of the commands has been implemented. All inputs and outputs, with the exception of the five boundary scan control signals, have scan I/O cells.

The following instructions are recognized by the JTAG controller: BYPASS, IDCODE, SAMPLE/PRELOAD, EXTEST, and INTEST. BYPASS collapses the scan loop to a single bit, thus bypassing the ASIC as seen by the board level scan loop, providing faster testing of other chips on the board. IDCODE serially outputs an identification code indicating the manufacturer, part number, and revision level of the ASIC. The four least significant bits are used to provide an address for the chip. This address will be set at the board level by hardwiring four input pins. SAMPLE/PRELOAD samples and preloads the boundary scan cells on two separate phases of the instruction. EXTEST tests the communication with the exterior by setting up values on the ASIC outputs and sampling values on its inputs. INTEST is used to test the internal circuitry. It accomplishes this by setting up known vectors on the input scan cells and capturing the results, after single stepping the core logic, in the output scan cells. The Adder ASIC implements all the above features. The other two main components to incorporate boundary scan are the Phase ASIC and the BSCAN ASIC..

An outline of features under consideration for board level boundary scan are listed here. The Phase ASIC has boundary scan on its outputs only. However, this should be sufficient to provide JTAG control over most of the circuitry on the card. The Phase ASIC can be used to set up data across all the inputs to the look up tables. The Adder ASIC can capture the resulting data on its inputs or pass it through to the downstream logic. The BSCAN ASIC has scan cells on both its inputs and outputs. The inputs can be used to capture test data set by either the Phase or Adder ASICs. The outputs can be used to set up test data for the backplane. Scan registers in ASICs on the Electron Isolation card and Jet Summary card can capture the data directly off the backplane. The BSCAN ASIC also provides the differential drivers for the backplane data and delay registers for data alignment. The delay is programmable from zero to seven 6.25 ns cycles.

The board level boundary scan controller will have a hardwired program that is entered on power-up or by command through the VME interface. This program will use vectors stored in a PROM on the board to perform a minimal test on intra-board circuit integrity and make simple tests of data paths within the ASICs. The vectors will check continuity, stuck-on ones and stuck-

on zeros, and shorts for those nets in the data processing path. The results of the applied vectors will be read back into the boundary scan controller via the scan loop and compared with the expected results, also stored in PROM.

The boundary scan controller interprets commands sent through the VME controller to perform the individual JTAG instructions implemented in the ASICs, captures the resulting data, and sends it back to the crate controller on request. Several boundary scan loops will be implemented rather than a single long loop in order to minimize the time required for tests of a specific sections of the logic.

5.9.3   Run time errors

Synchronization errors

Strategy to handle synch errors. Zeroing of data. Automatic recovery during abort gap resynch.

Data errors

Error detection. Zeroing of data bits on errors. Keeping track of error counts and enabling of error counter monitoring from VME.

5.10 Latency

The latency of the regional calorimeter trigger logic divided amongst several stages is estimated to be about 24 crossings. Since the logic is mostly clocked at 160 MHz, the operations are composed of 6.25 nsec cycles, four of which add up to a single 25 nsec crossing time. The Receiver card uses 6.25 crossings to process data. This includes the time for the serial data to enter the receiver chip, re-phasing of the data with the local clocks, intercrate sharing, and staging for the backplane. Transmission over the backplane requires .25 of a crossing. The Electron Isolation card uses 4.5 crossings to complete its processing before forwarding the data to the Jet Summary card. The sort path for electrons on the Jet Summary card requires the longest time on the card. This path, from card input to card output takes 4 crossings. The jet and tau cluster formation in the Cluster crate takes an additional 5 crossings. Contingency for latency increases due to any changes in the calorimeter regional trigger logic is set at 4 crossing adding up to a total of 24 crossings.

5.11 Prototypes and Tests

5.11.1 Overview

The goals of prototype development for this trigger system are many fold. Our strategy was to build as far as possible full-scale prototypes so that system issues are confronted up front. Pictures of rear and front views of the prototype crate holding prototype backplane and cards are shown in Figure 5.12.

5.11.2 Crate
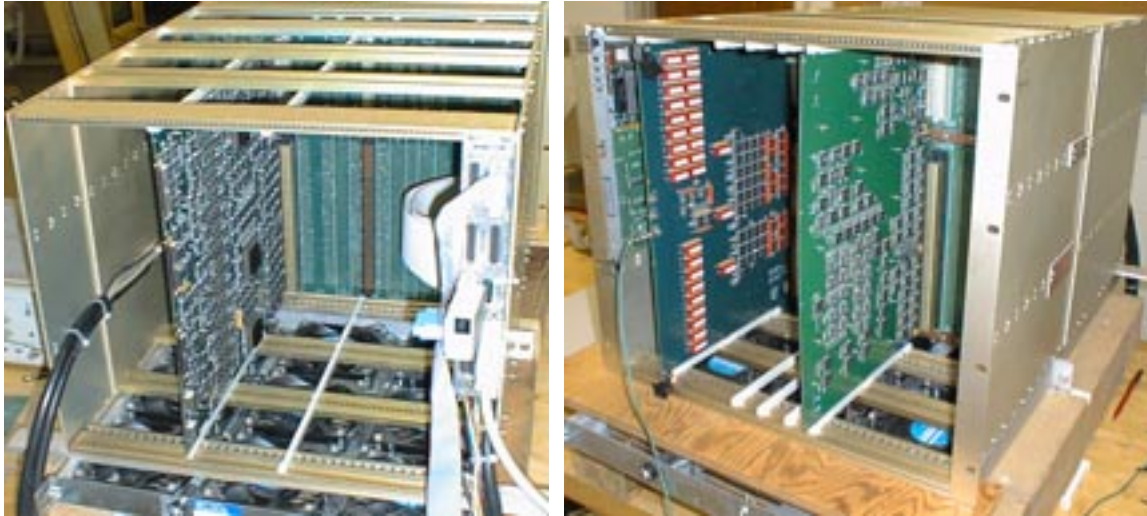
Fig. 5.13: Rear and front views of prototype calorimeter regional trigger crate showing the custom backplane, a receiver card, a clock card and an electron identification card.

(Test crate description, use and results.)

5.11.3 Backplane

To prove that high speed and high signal density can be handled, we have built a full sized backplane with point-to-point 160 MHz links and VME control. The backplane is a monolithic printed circuit board with front and back card connectors. The top 3U of the backplane holds 4 row (128 pin) DIN connectors, capable of full 32 bit VME. The first two slots of the backplane use three row (96 pin) DIN connectors in the P1 and P2 positions with the standard VME pinout. Thus, a standard VME module can be inserted in the first two stations. The form factor conversion to the remaining slots is performed on the custom backplane. The bottom 6U of the backplane, in the data processing section of the crate, utilizes a single high speed controlled-impedance connector for both front and rear insertion. The design is based around a 340 pin connector, by AMP Inc., to handle the high volume of data transmitted from the Receiver cards to the Electron Isolation and Jet Summary Cards. There are 1419 differential 160 MHz point-to-point links on the backplane between the various cards. The backplane is constructed with five ground and power planes and five signal layers with the differential pairs held to the same layer.

## 5.11.4 Clock and control card

We built a clock and control card to provide the necessary signals to drive other cards in the crate. The signals on even the longest links on this backplane preserve their characteristics well. Results from testing clock signals on the backplane show rise and fall times of 0.8 ns from 20% to 80% height with reasonable signal levels even when measured at the farthest card slot. This

performance meets the requirements of 160 MHz operation of the backplane.
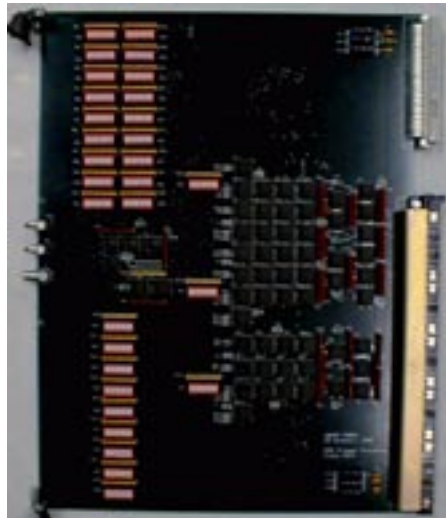
5.11.5 Receiver card

Description of implented functionality. Lessons learnt - list of changes made in the new Receiver card design and why.
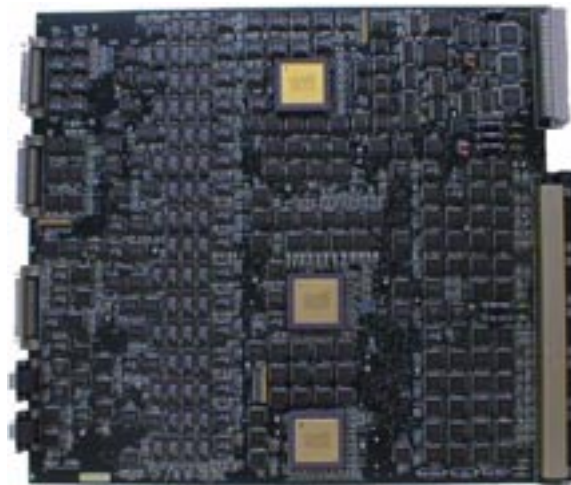
5.11.6 Adder ASIC

The Adder ASIC sums 8 signed 10-bit operands to a single signed 10-bit result at 160 MHz. We fabricated prototype adder ASICs which sums eight 10-bit signed numbers in a total of 4 25 ns clock-steps. These ASICs, built by Vitesse in 0.6 m H-GaAs technology, chosen for its speed and ECL output capability, have been tested to work at 200 MHz, well above our specifications. The Adder ASIC consists of approximately 11,000 cells and uses 4 W. The tests of the Adder ASIC on the receiver card were successful so that we deemed this design of the Adder as final and are in the process of procuring production quantities.
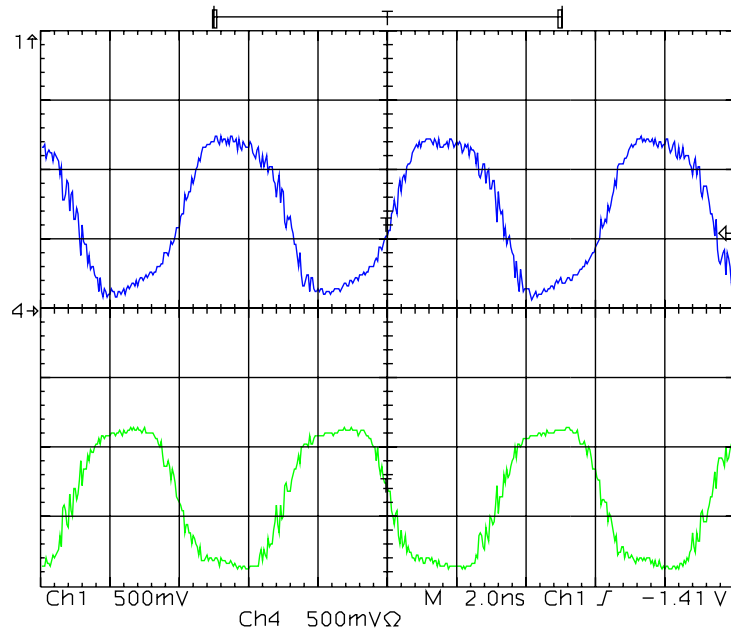
Block diagram.

5.11.7 Electron ID card

Description of test Electron ID card. Picture.

5.11.8 Dataflow tests

Results of dataflow tests between Receiver and test EID cards. Picture.

5.11.9 Receiver mezzanine cards

The receiver card uses daughter cards mounted on its rear side to receive its input from calorimeter front-end crates. We have designed these daughter cards with serial link chips (Vitesse 7214) and associated signal equalization support. These circuits along and an independent test card are in fabrication. We plan to use these cards to test the feasibility of receiving data on 20 m long copper cables at 1.2 GHz.

Pictures.

5.11.10 Serial link test card

Card description and use with transmitter and receiver mezzanine cards. Results.

Serial Link Test Card

Transmitter and Receiver Mezzanine Cards
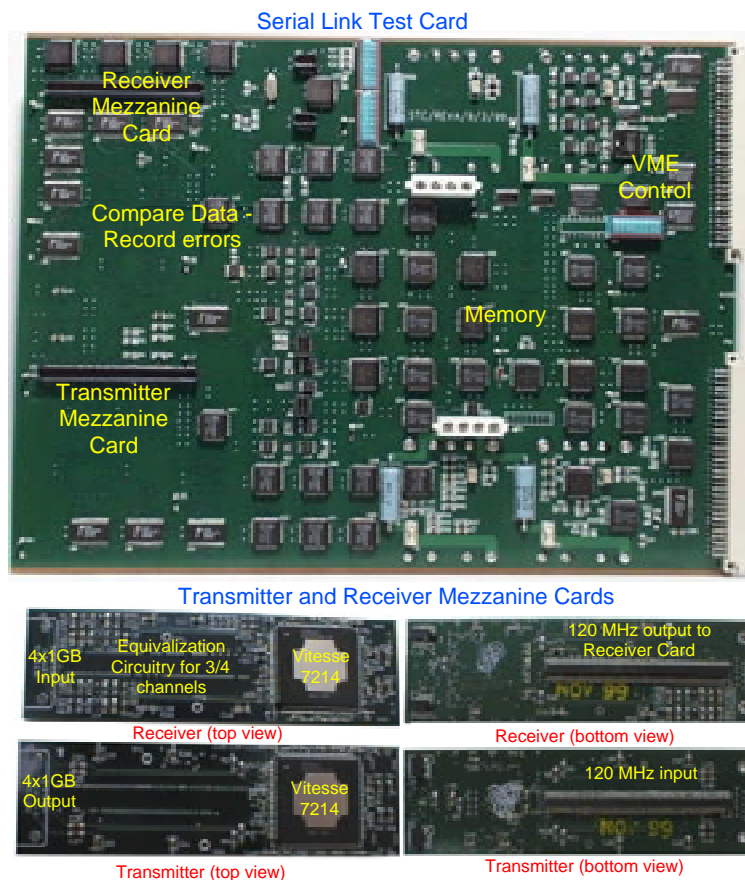
5.11.11 Prototype Summary

Success of our Adder ASIC prompted us to select the same technology for making other ASICs in our system. We have made preliminary designs of Phase ASIC described above, Electron Identification ASIC, Boundary Scan/driver ASIC and Sort ASIC and have agreement with Vitesse to produce these ASICs. Detailed design work is now in progress.

We are also carrying over the knowledge gained in making the prototypes discussed here in designing final backplane and other cards. We are incorporating the refinements made to the electron finding algorithm that resulted in some changes in the dataflow. The Receiver card prototype prompted us to move most of the discrete logic, used on that card to stage data to EID and Jet cards, into the Boundary scan ASIC. Another change we made is to use on card DC-DC converters to distribute needed power at appropriate voltages.

5.12 Status and Schedule