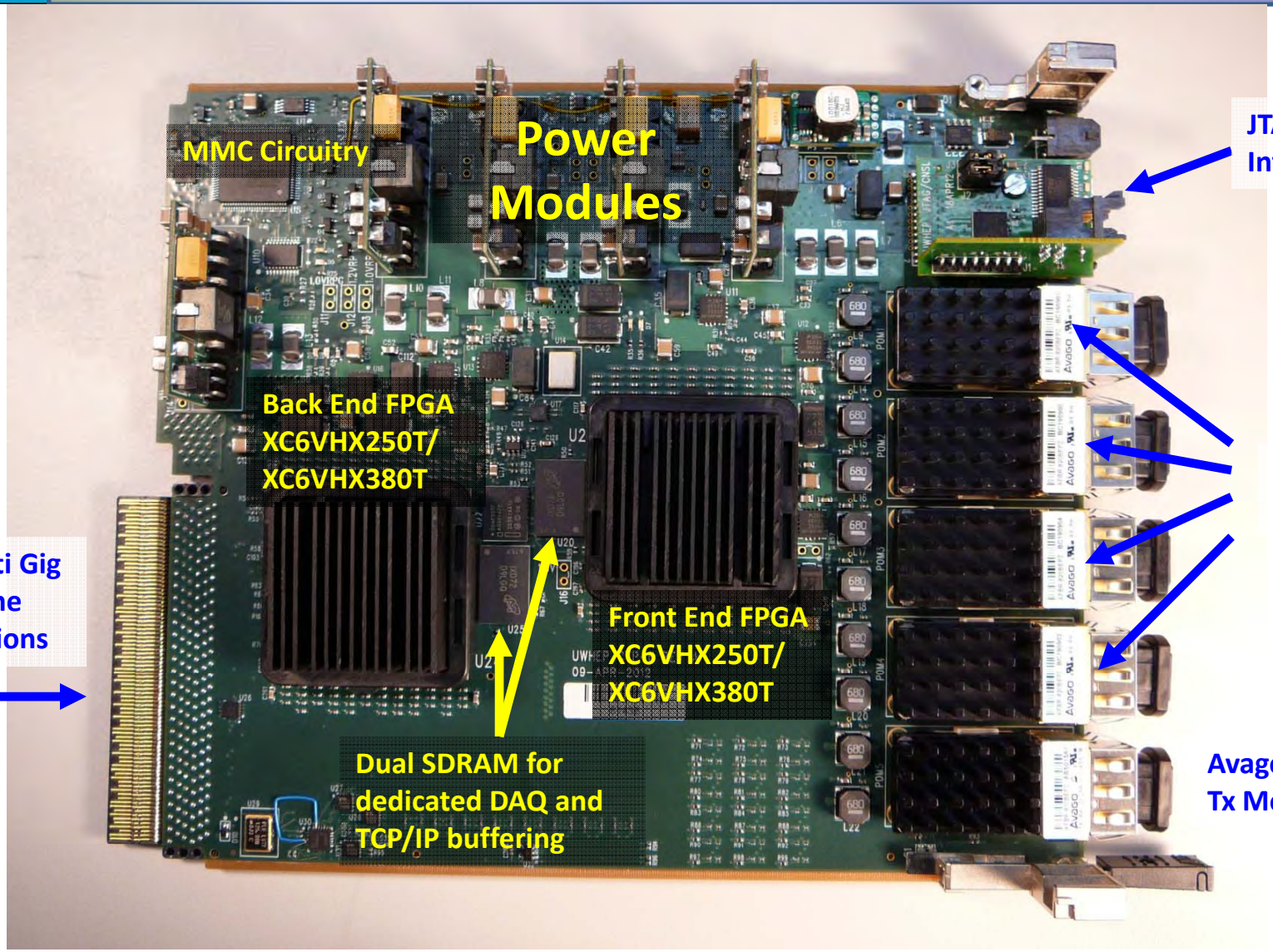
Calorimeter Trigger Hardware Update

T. Gorski, P. Klabbers, W. H. Smith, S. Dasu, , J. Tikalsky, D. Seemuth, A. Farmahini-Farahani, A. Perugupalli

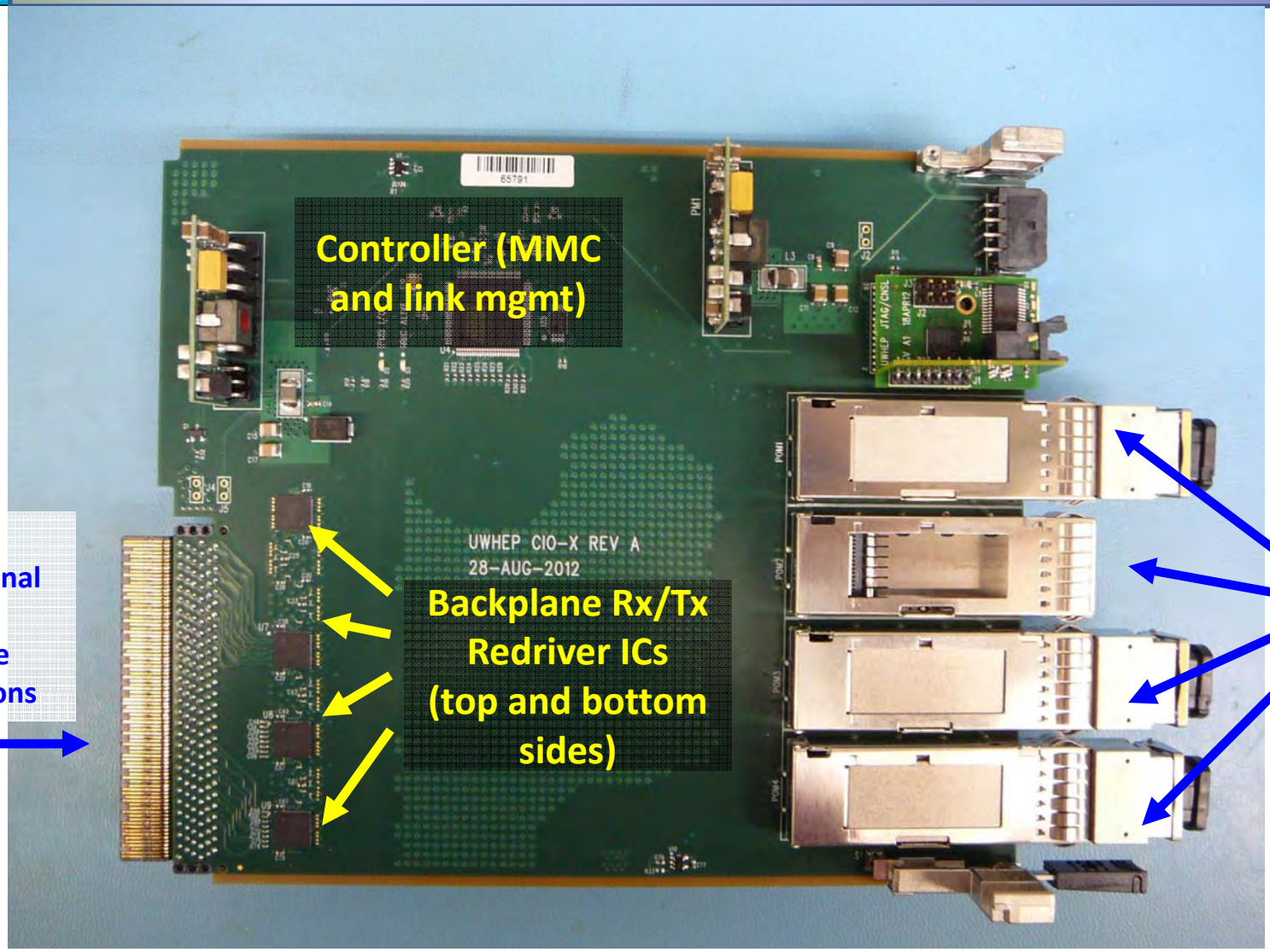
University of Wisconsin

November 15, 2012

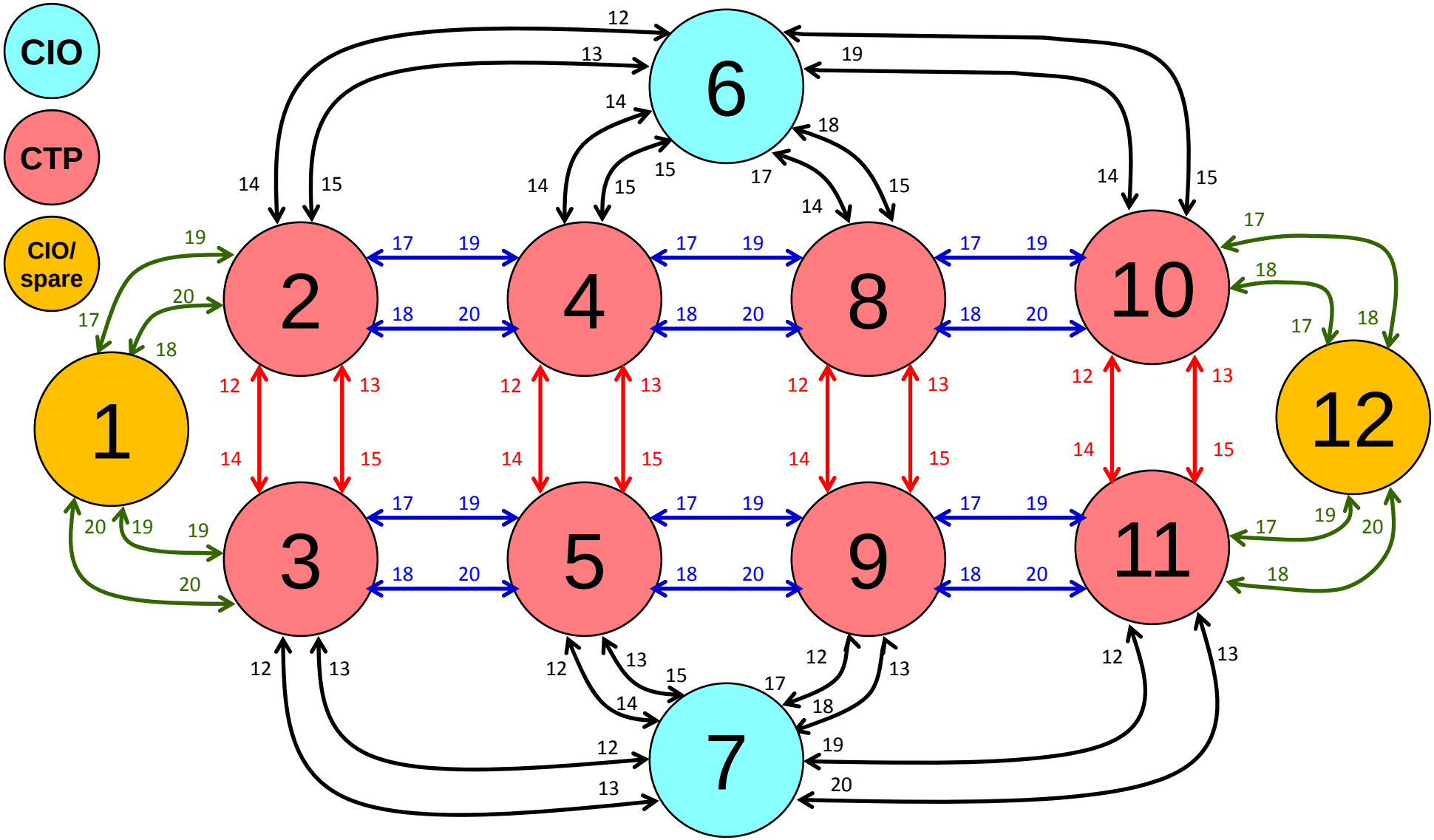
UW CTP-6


MMC Circuitry
Power Modules
JTAG/USB Console Interface Mezzanine
Back End FPGA XC6VHX250T/ XC6VHX380T
4X Avago AFBR-820B Rx Module
12x Multi Gig Backplane Connections
Front End FPGA XC6VHX250T/ XC6VHX380T
Avago AFBR-810B Tx Module
Dual SDRAM for dedicated DAQ and TCP/IP buffering

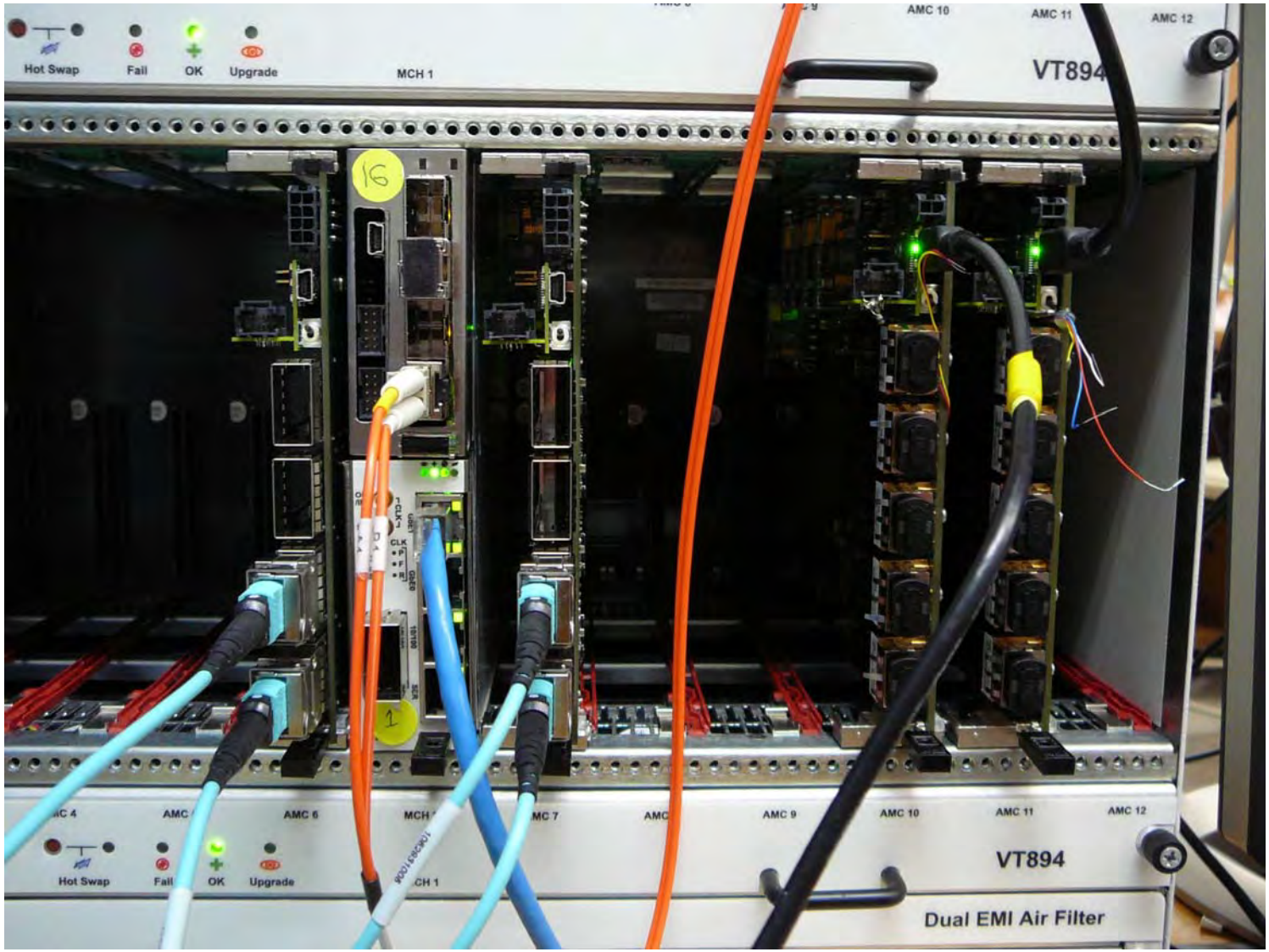
UW CIO-X


Controller (MMC and link mgmt)
UWHEP CIO-X REV A
28-AUG-2012
Backplane Rx/Tx Redriver ICs (top and bottom sides)
4x4 Lane Bidirectional Multi Gig Backplane Connections
4X Avago AFBR-79EQDZ QSFP+ Module Positions

VT894 Link Fabric—
All Paths Tested & Verified✓



CIO-X Link Test Setup

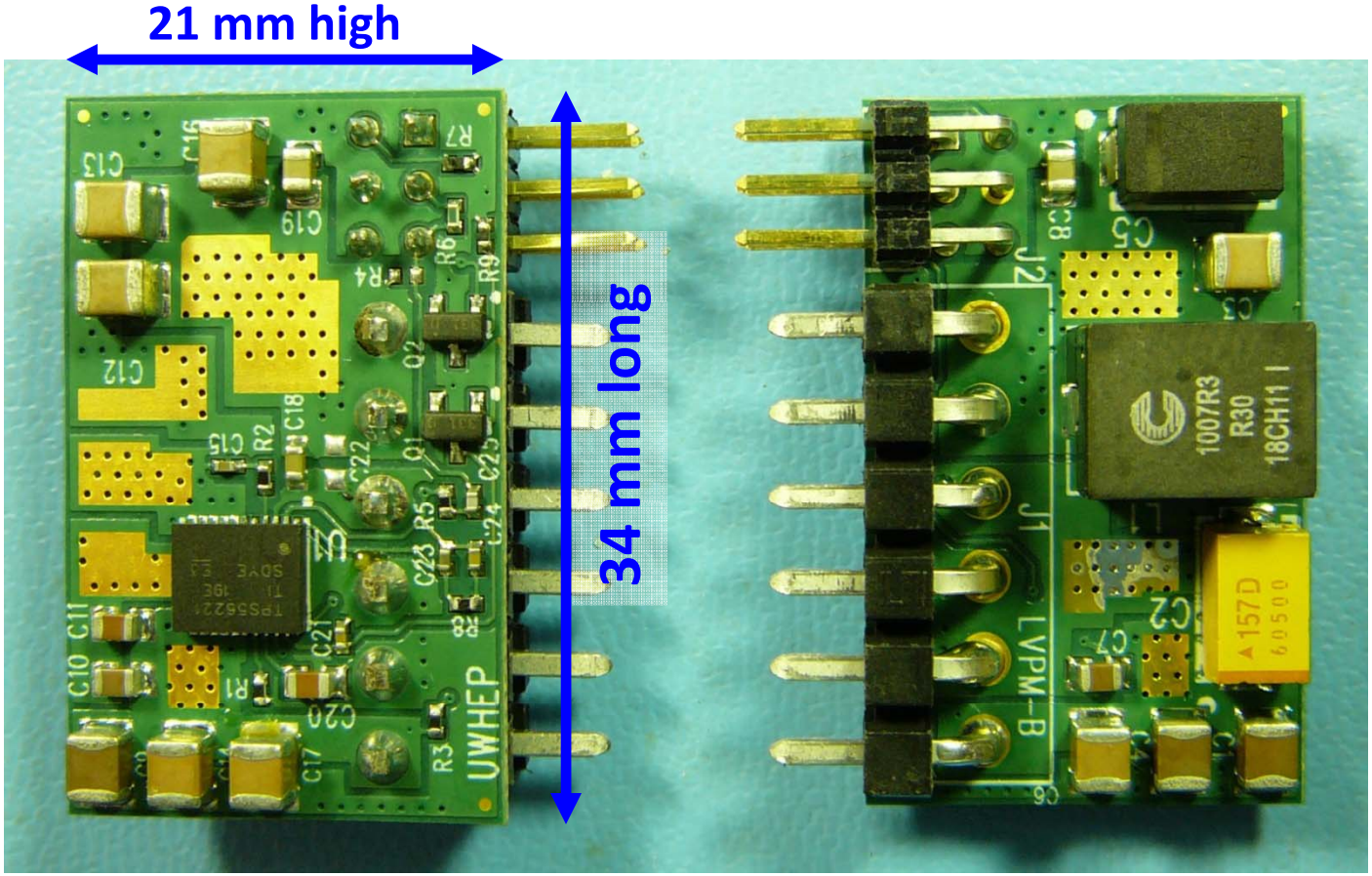


- Tests two intra-crate (backplane-only) and two inter-crate (backplane + optical) links at a time
- Move CTP cards to test all slots
- Tested at design data rate of 4.8 Gbps used in Compact Trigger architecture
- Using default settings on CIOX optical modules and backplane drivers

Link Testing Summary

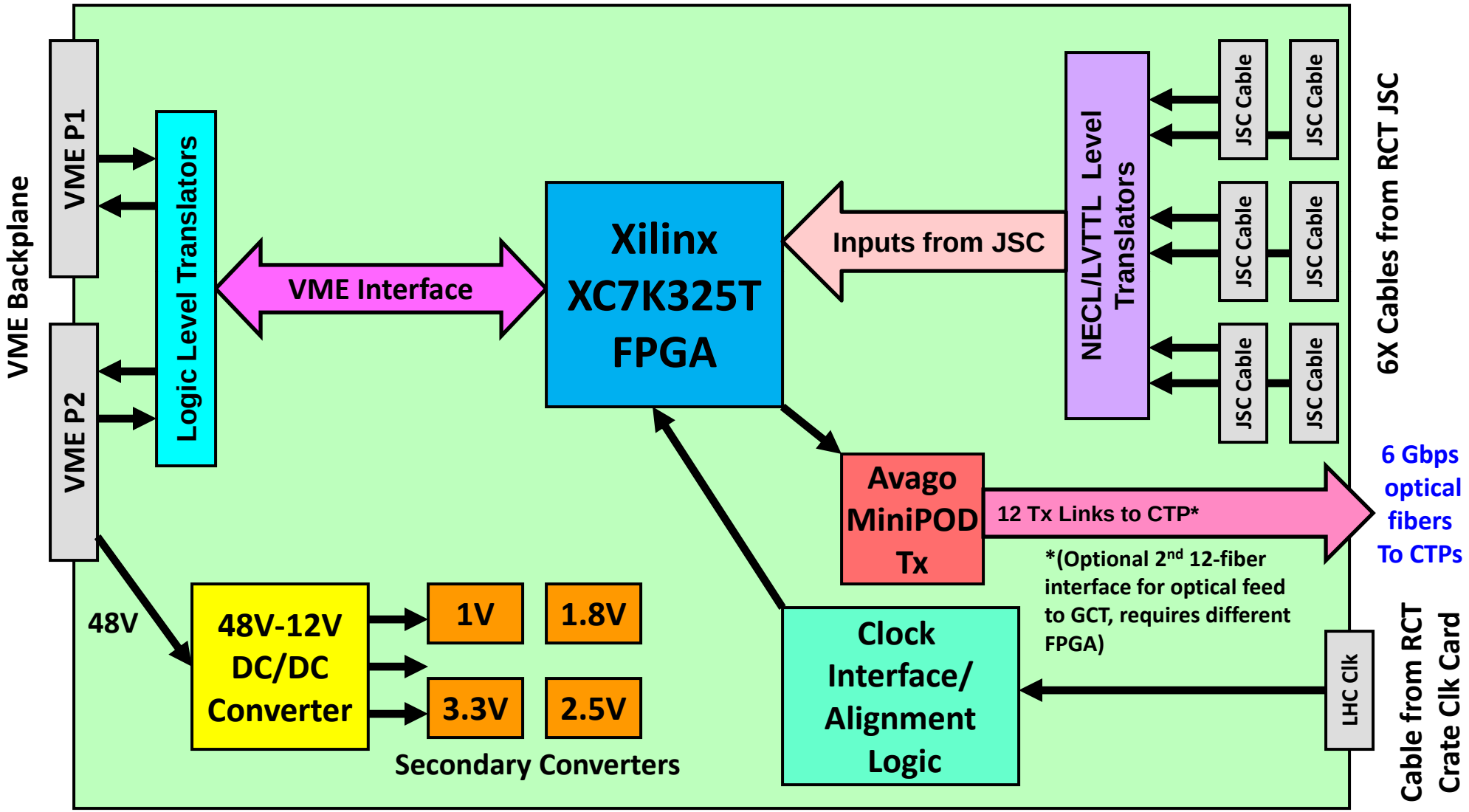
- **All CTP frontpanel optical and intra-board links tested and verified at 6.4Gbps, synchronous with LHC clock**
  - **Both intra-crate and inter-crate tests performed**
- **CTP inter-card backplane links tested and verified at design frequency of 4.8 Gbps, sync. w/ LHC clk**
  - **Includes paths through the crosspoint switch on the Vadatech UTC002 MCH**
- **All VT894 custom backplane paths tested and verified at 4.8 Gbps**

25A Custom Power Module for AMC Cards—Tested & Verified



- Rated for 25A
- Uses TI TPS56221 controller
- Voltage set by divider resistors on main board
- Prog. soft start & current limit
- Remote sensing
- 85-90% efficiency
- Heavy (2 oz) base copper
- Open-drain PWRGOOD output
- 9.5mm x 35mm CAD footprint

oRSC Card Block Diagram



UW Cal Trigger Hardware Summary

- **Prototypes of *all cards necessary for a Virtex-6 version of the Compact Trigger* have been acquired**
  - **CTP Card (2 units)**
  - **CIO-X Card (4 units)**
  - **VT894 Backplane (2 crates)**
  - **Vadatech UTC-002 MCH w/ 6.5 Gbps Xpoint Switch (2 units)**
- **All optical and backplane link paths have been tested and verified at their design speeds (6.4 and 4.8 Gbps)**
  - **No difference in test results when links run individually or in parallel with other links on the board**
  - **Only minor changes for CTP-6 Rev B**
  - **No changes planned for CIO-X**
  - **1 minor change to power module, may be put on as mod**

Upgraded Calorimeter Trigger

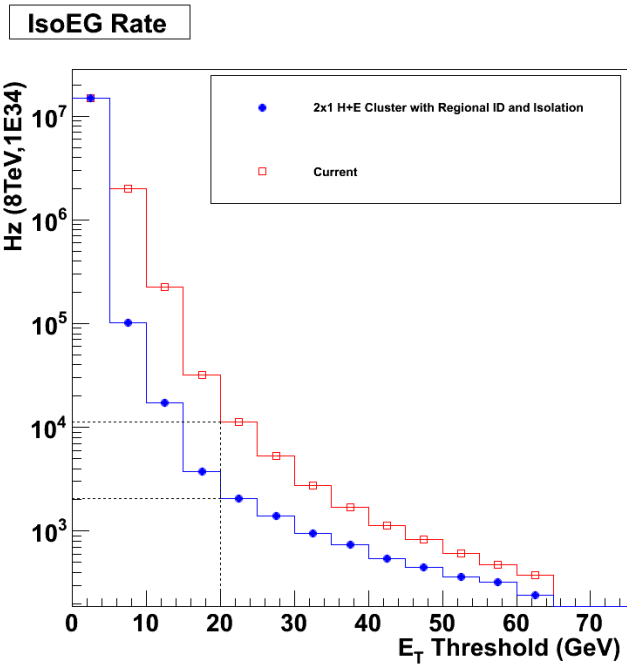
The Two Stage Plan

Stage-1 Motivation

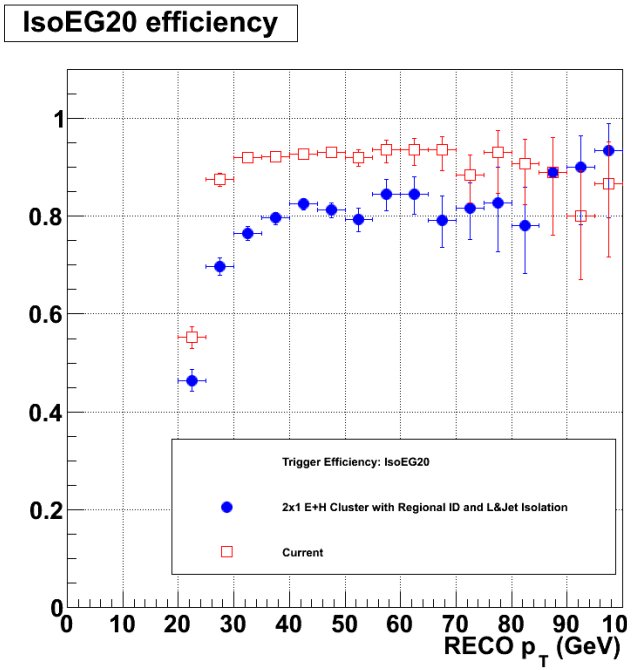
- High energy LHC run is special and improved trigger from Day-1 is highly desirable
  - Thank you for accepting this reasoning
- Stage-1 proposal is to first upgrade "essential items" – then add on …
  - Adiabatic improvements to calorimeter trigger proposed
  - Performance of the "revised" algorithms is very good
    - eGammaTau studied by Wisconsin ☺
    - eGamma and muon isolation studied by UCSD ☺
    - Muon isolation and b-jet tagging with muons studied by Ohio ☺
    - Heavy Ion jet cleanup studied by MIT ☺
  - Further improvements feasible/under study
    - Pile-up handling with lower LSB for ECAL
    - Improved jet finding with PU subtraction (UIC, Davis)
- The question in most people's mind now is simply,
  "How do we accomplish this?"

Sample Simulation Results

Isolated Electron / Photon Trigger

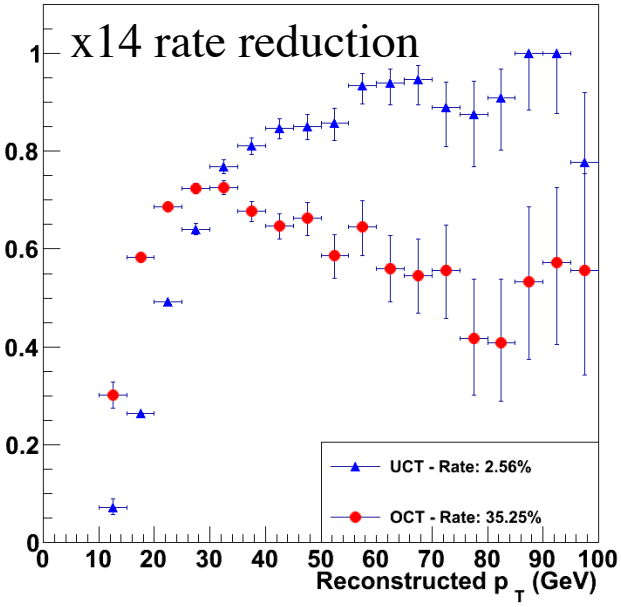


Significant rate reduction (x5) over current isoEG trigger



Efficiency drop of 20% for factor of 10 in rate. Tune as needed to trade efficiency versus rate

Isolated Tau Trigger

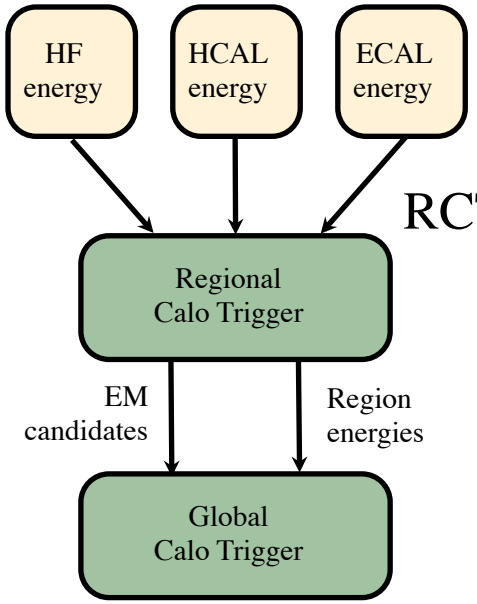


Dramatic improvement in taus by decoupling from jets – 2x1 objects in the upgraded trigger

Prior Presentations on Stage-1

- Do not wish to repeat past presentations, you may see below
- USCMS Meeting in Colorado (18 May 2012)
- Upgrade week at CERN (24 May 2012)
- L1 DPG / Upgrade Meeting (14 June 2012)
- Trigger Upgrades Workshop (12 September 2012)
  - Heavy Ion Case (MIT)
- Future Higgs Meeting (19 September 2012)
- Muon Trigger Upgrade Meeting (24 October 2012)
- L1 Trigger CDR Part 1 (31 October 2012)
- Document on Stage-1 (also tasks/schedule/people given)
- L1 DPG / Upgrade Meeting (UCSD) (30 October 2012)
- L1 TDR Simulation Task Force (2 November 2012)
- L1 DPG / Upgrade Meeting (Ohio) (8 November 2012)

Current L1 Trigger System



RCT strengths worth retaining

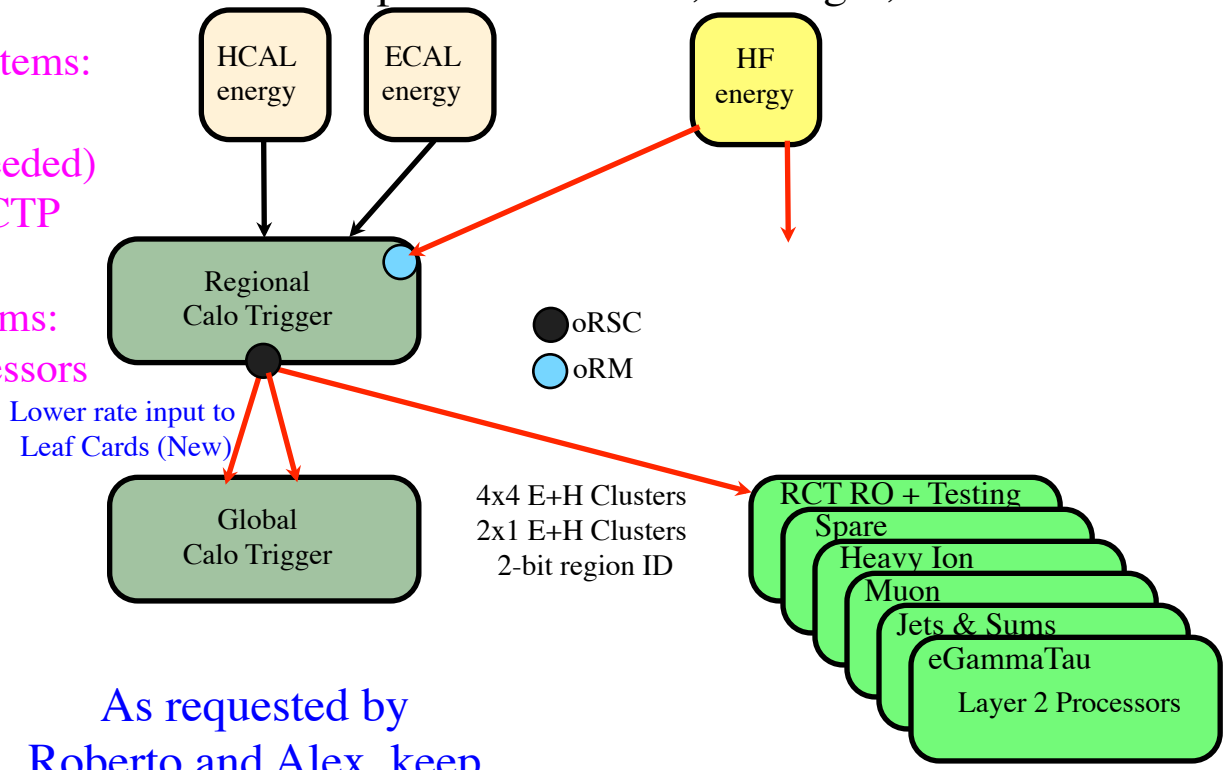
- Programmable clusters using LUTs
  - Addressed by E & H TPGs
  - Independent Jet & eGamma paths
- Adder ASICs for bulk processing
  - 4x4 sums with low latency

The Minimal Stage-1

The Minimal Stage-1 with little disturbance to working current trigger
Replace Source Card system with oRSC: x6 duplicator 6.4 Gbps + 1x leaf card compatible
More sophisticated GCT => improved isolation, tau-logic, … over current trigger

Proposed Wisconsin Items:
- oRSCs
- oRMs for HF (if needed)
- RCT RO+Testing CTP

Proposed Imperial Items:
- MP7 Layer 2 Processors



As requested by Roberto and Alex, keep GCT working alongside

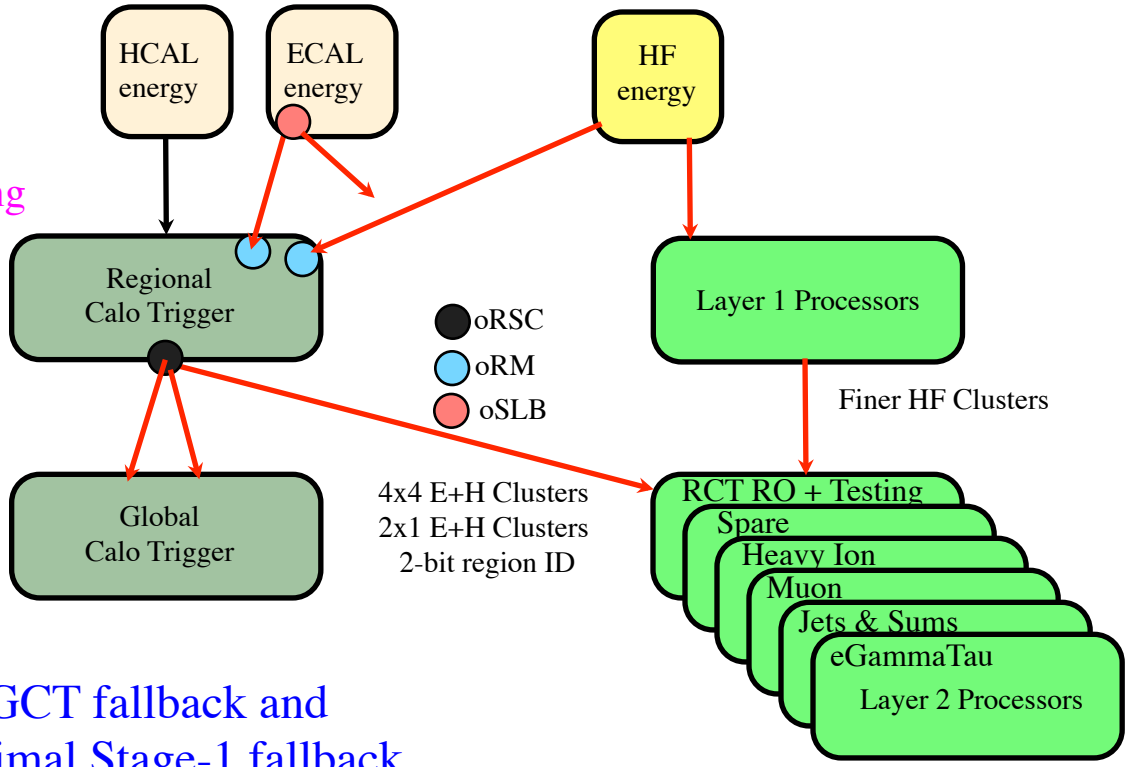
Derive all the benefits simulated so far using UCT2015 code by various groups

The "Approved" Stage-1 - HF

The Approved Stage-1 also brings in all the power of finer grain HF – "Slice Test"
Uses two Layer-1 Processor cards

Proposed Wisconsin Items:
- oRSCs,
- oSLB/oRM commisioning
- CTP Layer 1 Processors
- RCT RO+Testing CTP

Proposed Imperial Items:
- MP7 Layer 2 Processors



GCT fallback and
Minimal Stage-1 fallback
remains available

Derive all the benefits of HF

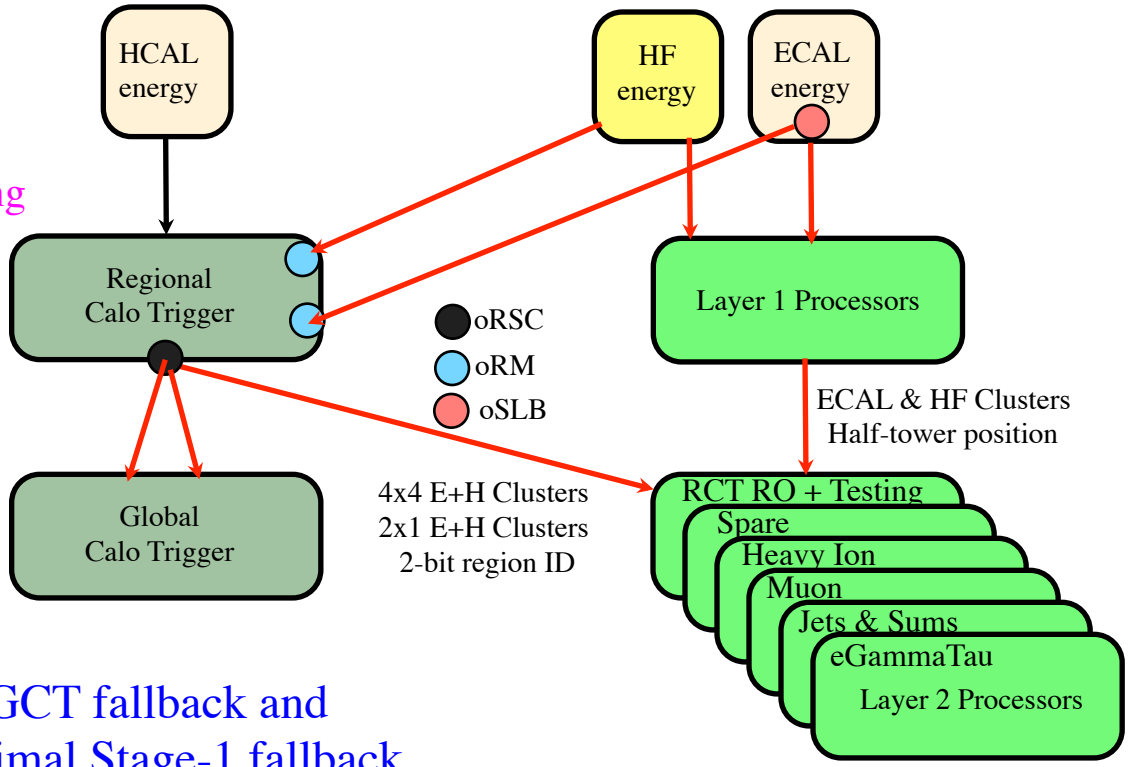
Wisconsin group agreed to deliver the Approved Stage-1

The Full Stage-1 - Better EM

The Full Stage-1 can bring in all the power of finer grain EM Clusters from 2015
Uses ~half the Layer-1 Processor cards – also used in the Final Stage-2 System
Improved PU subtraction, Isolation Calculation and Half-tower Position Resolution

Proposed Wisconsin Items:
oRSCs,
oSLB/oRM commisioning
CTP Layer 1 Processors
RCT RO+Testing CTP

Proposed Imperial Items:
MP7 Layer 2 Processors



GCT fallback and
Minimal Stage-1 fallback
remains available

Derive all the benefits seen in simulations so far

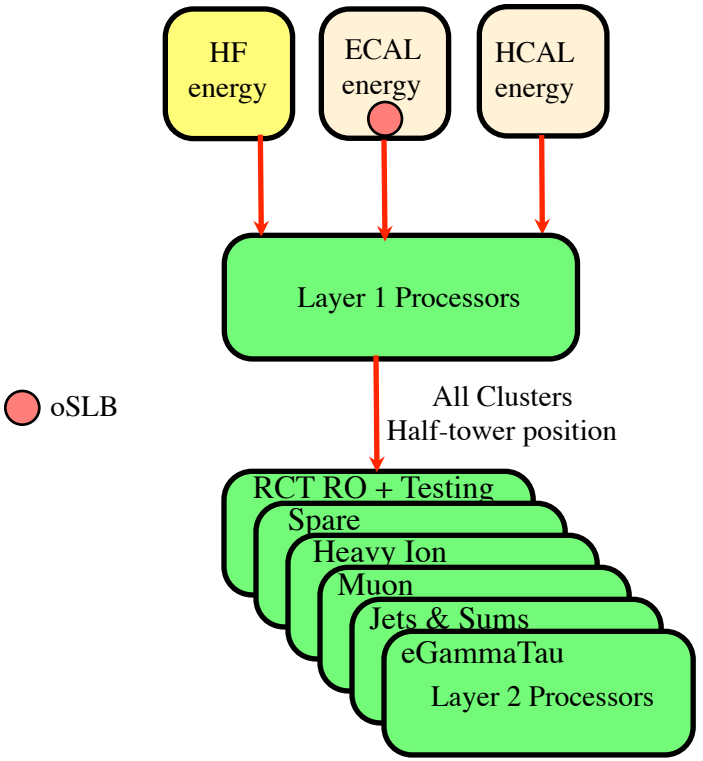
Wisconsin group committed to deliver full Stage-1 by 2015 start.

Stage-2

Stage-2 – complete upgrade including optical input from HB/HE

The benefits from HB/HE upgrade are only seen after LS2, when improved HCAL signals and trigger primitives are available.

However, we are planning to finish the Stage-2 sooner (operating in 2016 per the approved plan), because it can remove the 4x4 constraint from the RCT in Stage-1, providing some improvement to jet trigger.



Derive all the benefits promised and expected when fully upgraded frontend and backend of HCAL (HB and HE)

Summary

- With the anticipated resources of USCMS, we can deliver Stage-1 fully, (using RCT, oRSC, CTP hardware and firmware), by the end of 2014
  - Updated Stage-1 also includes better ECAL clustering
- Stage-2 can be completed as planned in 2016 assuming that the optical inputs from HB and HE are available earlier than foreseen in HCAL upgrade TDR
- We have prepared a reasonably detailed resource loaded schedule
- The proposed upgrade path has an adiabatic evolution with fallback at every stage, depending on what actually unfolds.
- Wisconsin, UCSD, UIC, FNAL, MIT … are developing algorithms and preparing results using real data from the detector
  - We believe will significantly enhance the CMS physics reach
  - We invite others in USCMS collaboration to join us
- We should have a strong TDR case!