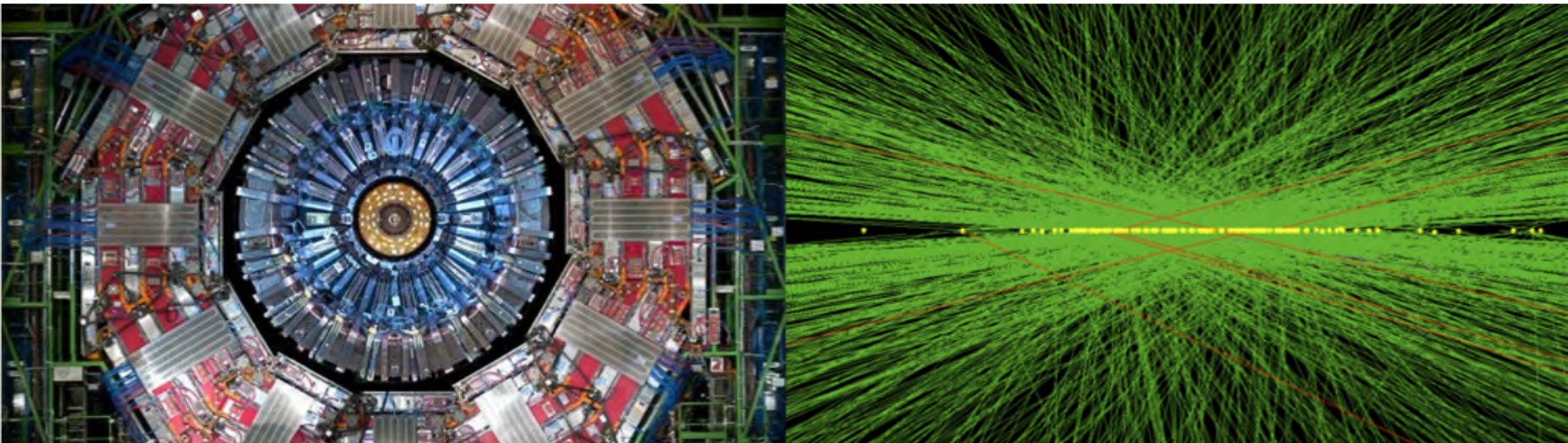# 402.2.6.3   Calorimeter Trigger Technical Overview

Wesley H. Smith, U. Wisconsin

HL LHC CMS Detector Upgrade Director's CD-1 Review

April 4th, 2018

Outline

- **Scope of Calorimeter Trigger**
  - WBS Structure

- **Conceptual Design**
  - Requirements and performance

- **Hardware platform**

- **R&D Program**
  - Algorithm R&D.
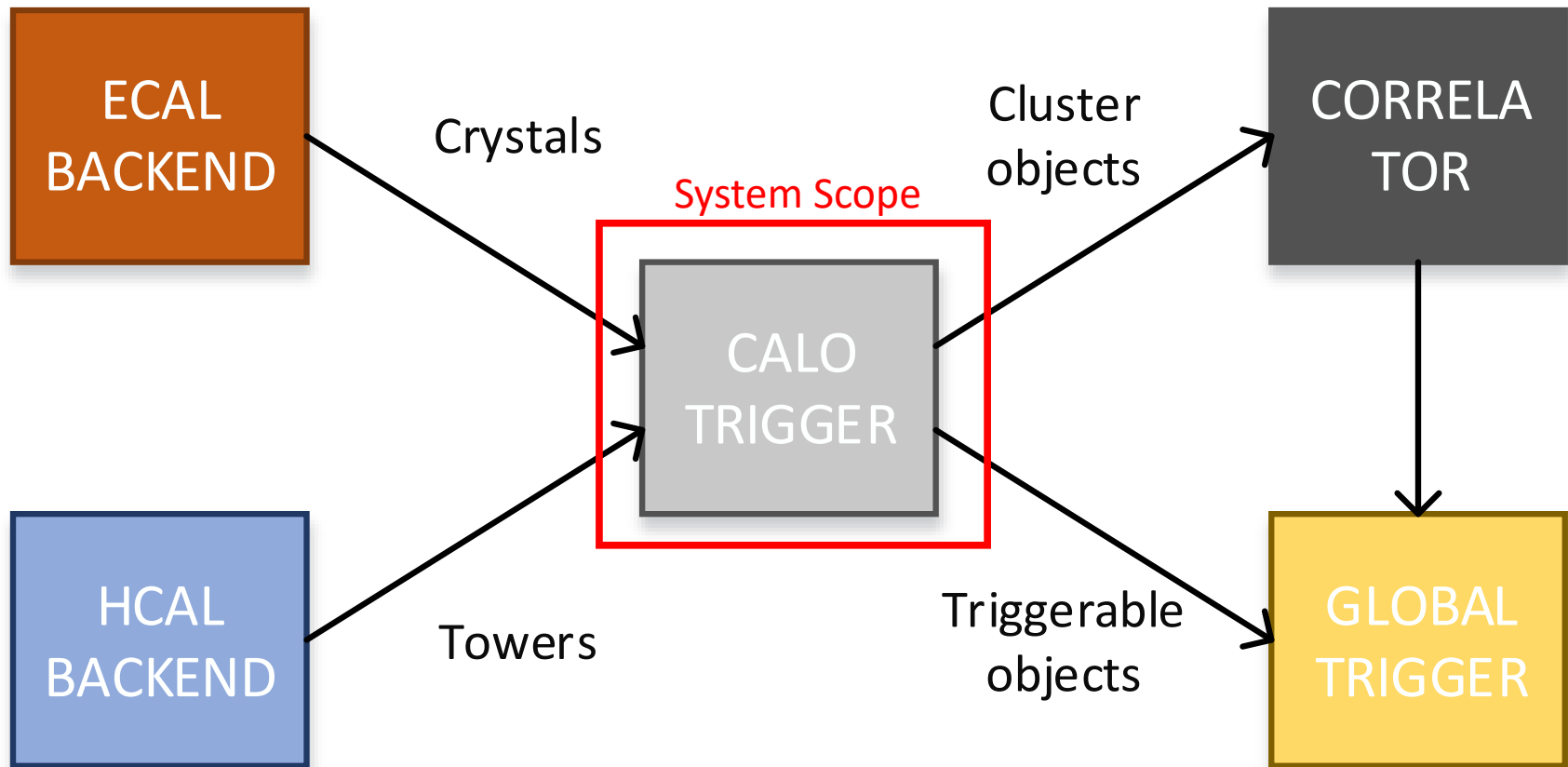 - Hardware R&D
  - Firmware R&D
  - Software R&D

Scope

Charge #1,3
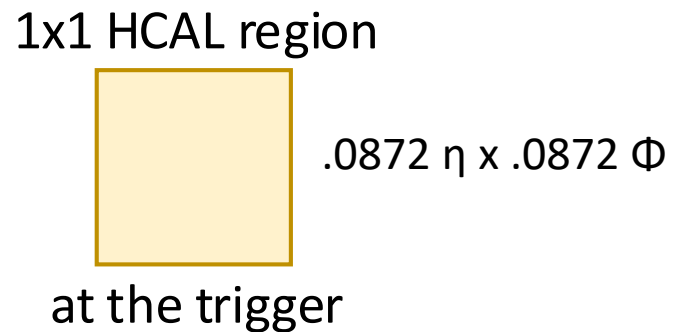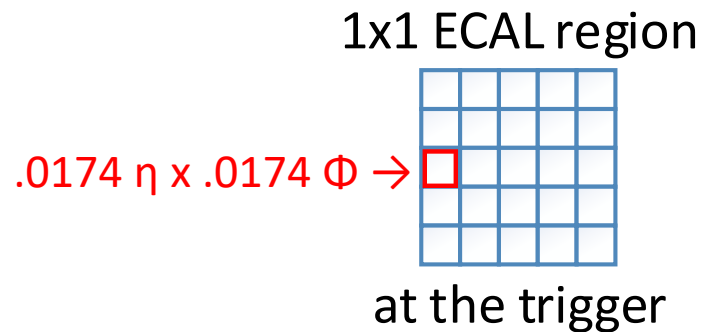
■ **L1 Barrel Calorimeter Trigger**

- Input Energies from ECAL Barrel Crystals and HCAL Barrel Towers
- Output energies, locations of clusters and candidate e/γ, τ, jets, and energy sums to track correlator and global trigger

Inputs and Outputs

- Inputs:

  - ECAL **crystal** level information (5x5 crystals per tower) - assuming **16bits/crystal** or 400bits for one 1x1 region.

  - HCAL **tower** level information – assuming **16bits/tower**.

1x1 ECAL region

.0174 η x .0174 Φ →

at the trigger

1x1 HCAL region
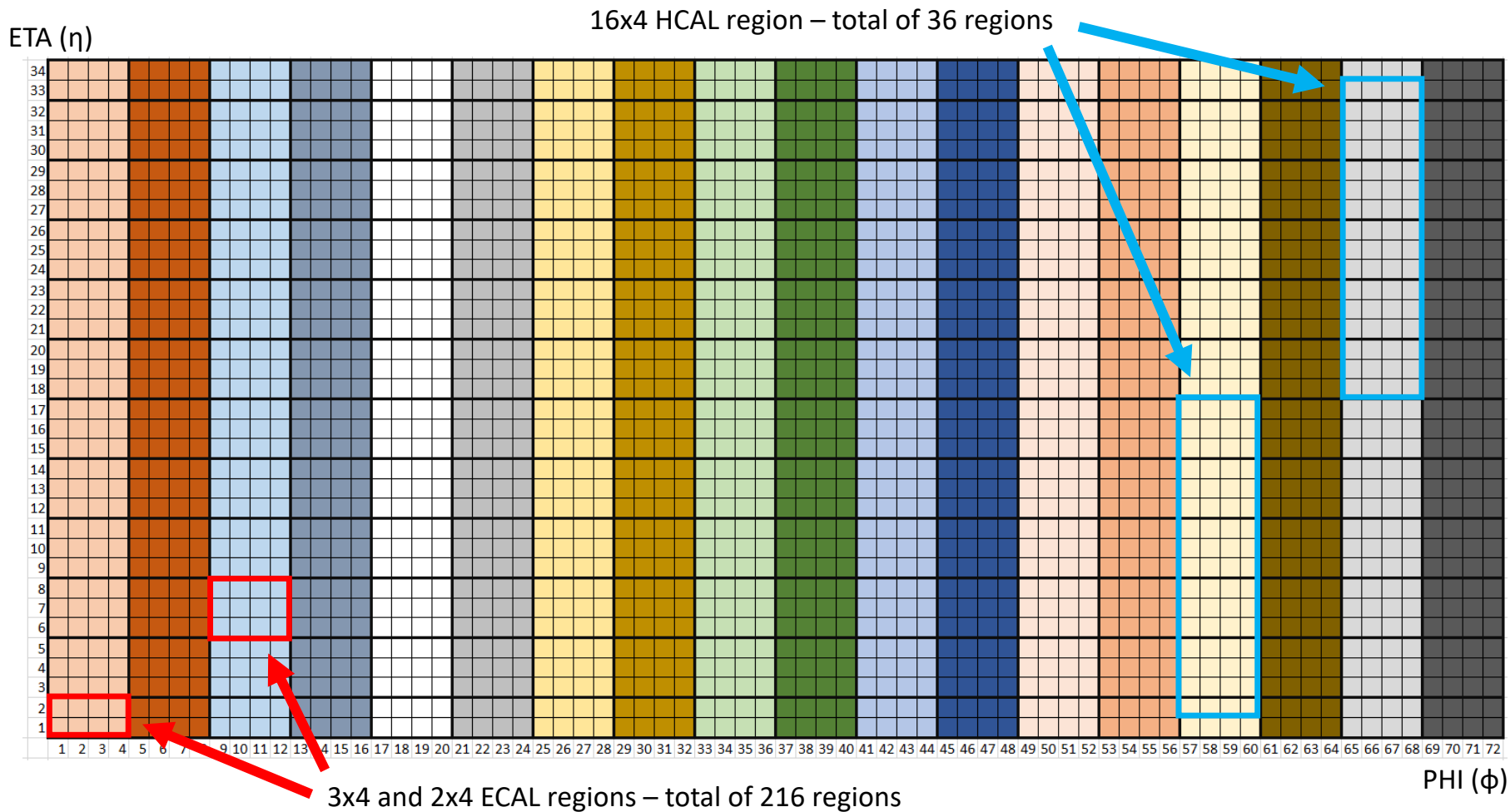
.0872 η x .0872 Φ

at the trigger

- Outputs:

  - Cluster objects will be sent to the Correlator.

  - Triggerable objects (standalone calorimeters triggers) will be sent to the Global Trigger.

ETA (η)

16x4 HCAL region – total of 36 regions

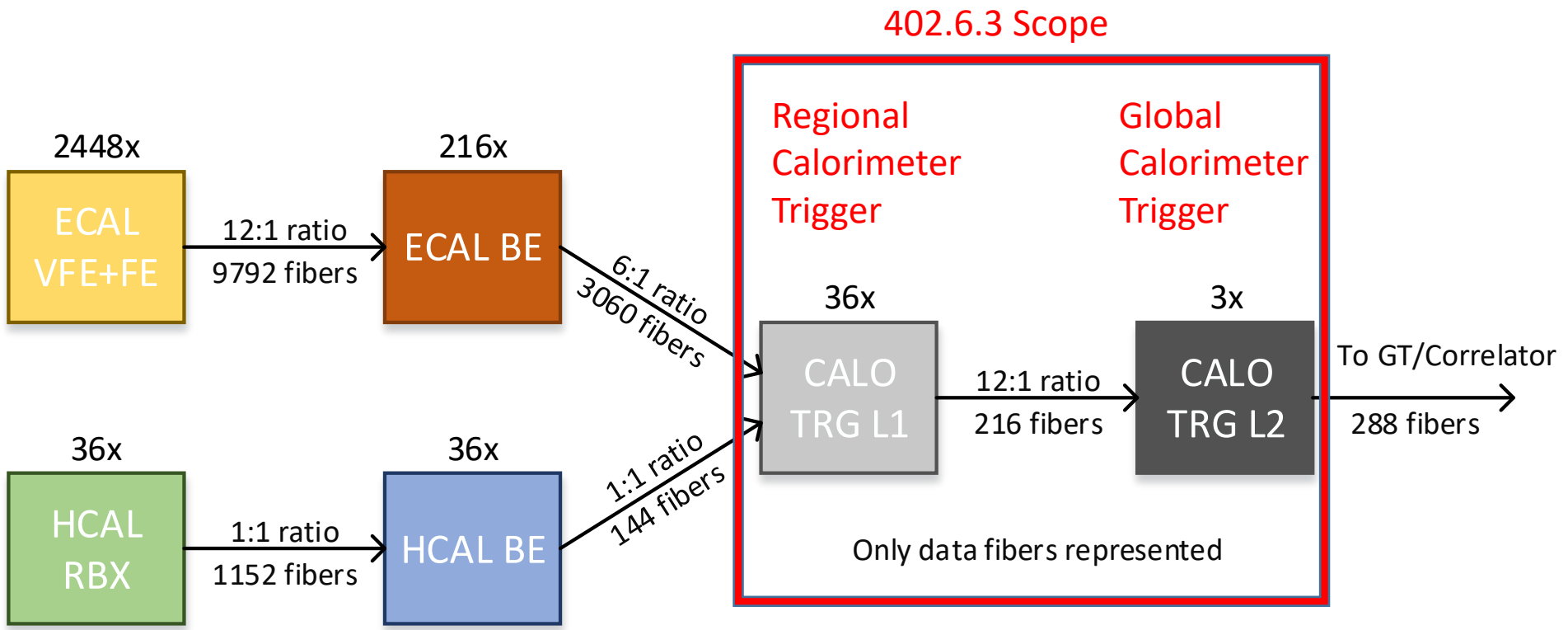3x4 and 2x4 ECAL regions – total of 216 regions

PHI (φ)

System Layout

- **Boards with 96 optical links available for data reception and transmission.**
    - **4 Additional links for DAQ readout**

- Layer-1 partitions detector in **17η x 4φ** regions – total of 36 regions.
    - ECAL inputs: 5x **3η x 4φ** and 1x **2η x 4φ** regions – 85 ECAL fibers.
    - HCAL inputs: 1x **16η x 4φ** region – 4 HCAL fibers.
    - Outputs: 6 fibers per region with regional clusters and metadata (2.1kbits/BX).

- Layer-2 will have clusters and metadata of all regions:
    - Inputs from Layer-1: 36 x [**(17η x 4φ)** on 6 fibers] – 216 Layer-1 fibers.
    - 288 outputs available for clusters for the correlator and standalone trigger objects for the Global Trigger.

- A total of 36 layer-1 and 3 layer-2 Boards are required: **39 Cards**.
    - A total of **216 fibers** are required between layers.

Full System Layout

402.6.3 Scope

2448x — ECAL VFE+FE

12:1 ratio / 9792 fibers

216x — ECAL BE

6:1 ratio / 3060 fibers

36x — HCAL RBX

1:1 ratio / 1152 fibers

36x — HCAL BE

1:1 ratio / 144 fibers

Regional Calorimeter Trigger

36x — CALO TRG L1

12:1 ratio / 216 fibers

Global Calorimeter Trigger

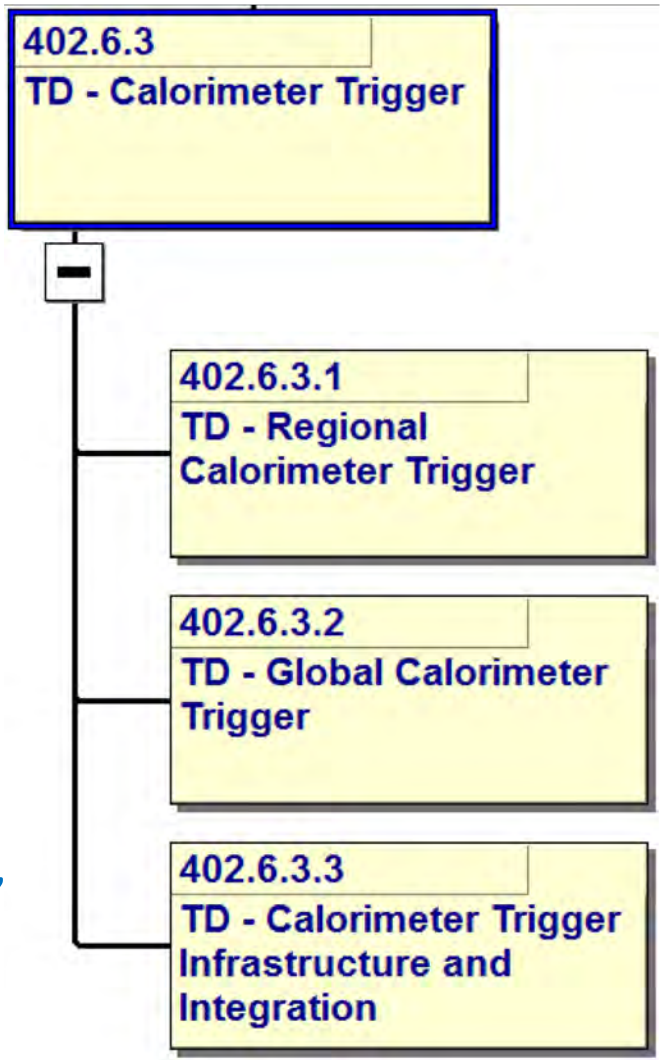3x — CALO TRG L2

To GT/Correlator / 288 fibers

Only data fibers represented

Ratios reflect ηxφ input regions to output regions

402.6.3 WBS Structure

- **WBS 402.6.3.1, 2 include design, engineering and technical labor and M&S to produce the RCT and GCT boards:**
  - Optical components, FPGAs and other components
  - Management and engineering support of board production
  - Fabrication of the PCBs and assembly of finished electronics.

- **WBS 402.6.3.3 includes all design, engineering and technical labor to produce the Calorimeter Trigger infrastructure:**
  - Crates, fibers, patch panels and DTH Card that provides the DAQ and clock/control/trigger interfaces.
  - US Responsibility: Design and technical labor, plus associated Software and Firmware costs
  - CERN Responsibility: Infrastructure M&S

402.6.3
TD - Calorimeter Trigger

402.6.3.1
TD - Regional Calorimeter Trigger

402.6.3.2
TD - Global Calorimeter Trigger

402.6.3.3
TD - Calorimeter Trigger Infrastructure and Integration

Conceptual Design

Design Considerations for CT

- Trigger with the highest possible efficiency:
  - Isolated high p_T electrons, photons, and taus
- Trigger with reasonably high efficiency for:
  - jets with vertex identification
  - inclusive quantities such as missing transverse momentum
- Accomplish this performance within the constraints:
  - Within the shortest possible latency
  - While maintaining a total trigger rate of less than 750 kHz for pileup of 200 collisions/crossing
  - Process input data provided by the upstream trigger primitive logic
  - Provide output data meeting the specification of the downstream trigger logic.
- The barrel calorimeter trigger system needs to:
  - Process trigger primitive information from individual EB crystals and HB towers on fiber optic links at 16 Gb/s.
    - NB: Phase 1 trigger used ECAL 5x5 crystal towers – same size as HCAL towers.
  - Complete calculations in less than 1 µsec - the assigned portion of total latency allowed
  - Provide trigger objects on 16 Gb/s fiber links usable by the Correlator and Global Trigger as inputs to trigger calculations included in a total L1 Trigger menu rate of less than 750 kHz with pileup of 200 collisions/crossing
  - Provide these trigger objects with the highest possible measurable efficiency and purity over the η range -1.5 to +1.5

Hardware Design

- Dimension calorimeter trigger architecture using existing or under-development technologies (Advanced Processor – AP)
  - FPGAs: Xilinx Ultrascale and Ultrascale+ families.
  - Optics: Samtec Firefly Modules – 100Mbps to **28 Gbps**.
    - Either 12 transmitters or 12 receivers per module (up to 16 Gbps)
    - Also usage of 4 transmitter and 4 receiver modules (up to 28 Gbps)
    - Each 16 Gbps link allows up to **352bits/BX** of data payload, using 64b66b encoding and 32bits/packet reserved for protocol (option → 20)
  - ATCA – Advanced Telecommunications Architecture
  - Build upon Phase-1 experience with hardware, firmware, software
- Close ties between algorithm development, simulation studies, firmware and software development and design engineering to provide a hardware platform for High-Luminosity LHC physics.
  - Exploit new High Level Synthesis (HLS) tools (later slides)

Trigger Performance goals

- Ultimate goal is to reach offline reconstruction performance at the L1 trigger level
  - Increasing efficiency of the reconstruction
  - Sharpening the trigger efficiency rising edges
  - Reducing background rates
  - Combination of calorimeter and tracking information
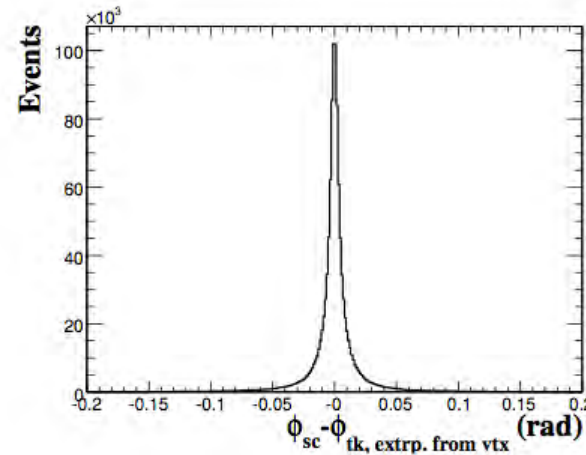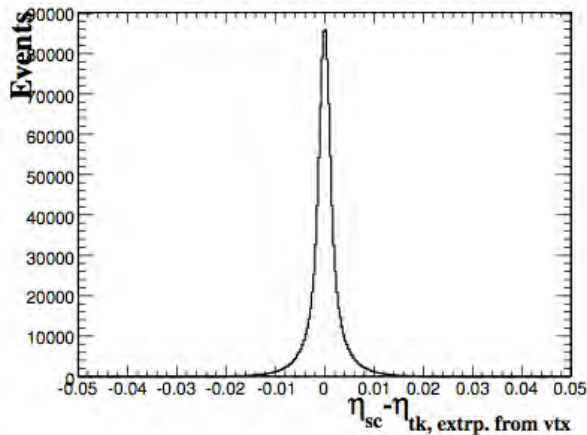
Offline ECAL Super Cluster to Track matching is shown for electrons.
Offline performance can be achieved at L1 by using single crystal information

Architecture

- Start with a tiled multi-layer architecture where:
  - Layer-1 partitions the detector and forms regional clusters.
  - Layer-2 stitches neighbouring clusters and forms detector-wide triggerable objects (e.g. MET).
  - Possibility to expand by adding additional layers or more cards to a certain layer.

- Use the following Xilinx FPGA package :
  - C2104: Maximum of 104 optical links – 96 available.
  - Assuming eight links reserved for DAQ, control, etc.

R&D Program

- **Algorithm R&D**
  - Ensure performance of algorithms implemented in design
  - Refine requirements for design performance.

- **Hardware R&D**
  - ATCA technology trigger card demonstrator
  - Calorimeter Trigger system demonstrator: Calorimeter BE → Calorimeter Trigger → Correlator

- **Firmware R&D**
  - High Level Synthesis of trigger algorithms
  - Trigger Card Infrastructure Firmware

- **Software R&D**
 - Control Infrastructure
  - Monitoring and Diagnostics Software

R&D Example: e/ɣ Algorithm

- ECal hit considered if E > 0.5 GeV

- HCal hit considered if E > 0.5 GeV

- Clusters are formed around the highest p_T ECal seed crystal of p_T > 1 GeV

- Surrounding crystals are summed in a 3 x 5 window
  - Brems correction 3x5 above bellow added if add more then 10% of energy

- Isolation and Pileup-corrected p_T calculated excluding 3 x 5 window
  - Isolation: 27 x 27 crystals
  - Pileup-corrected p_T: 13 x 113 crystals

- H/E calculated using HCal region within 0.3 η x 0.3 φ (~17x17 crystals) used only for checks, no cut on it

- Position is calculated as energy weighted sum

Calorimeter Trigger Performance

- **Stand-alone (no track linking) Calorimeter Trigger L1 e/γ Object shows both an efficiency and rate improvement over the Phase-1 algorithm at PU of <200>**
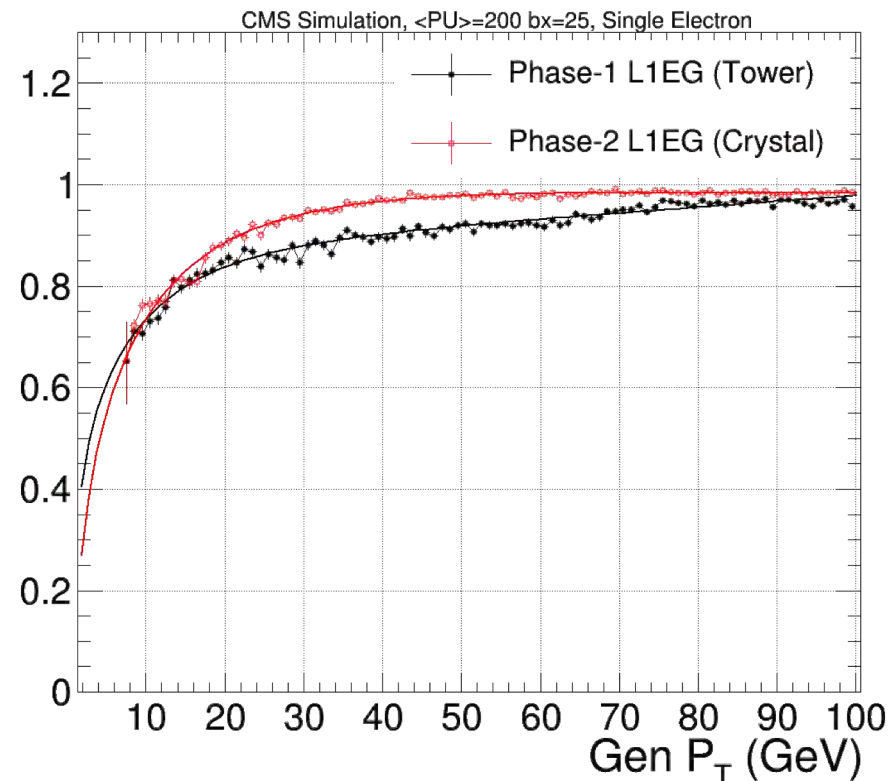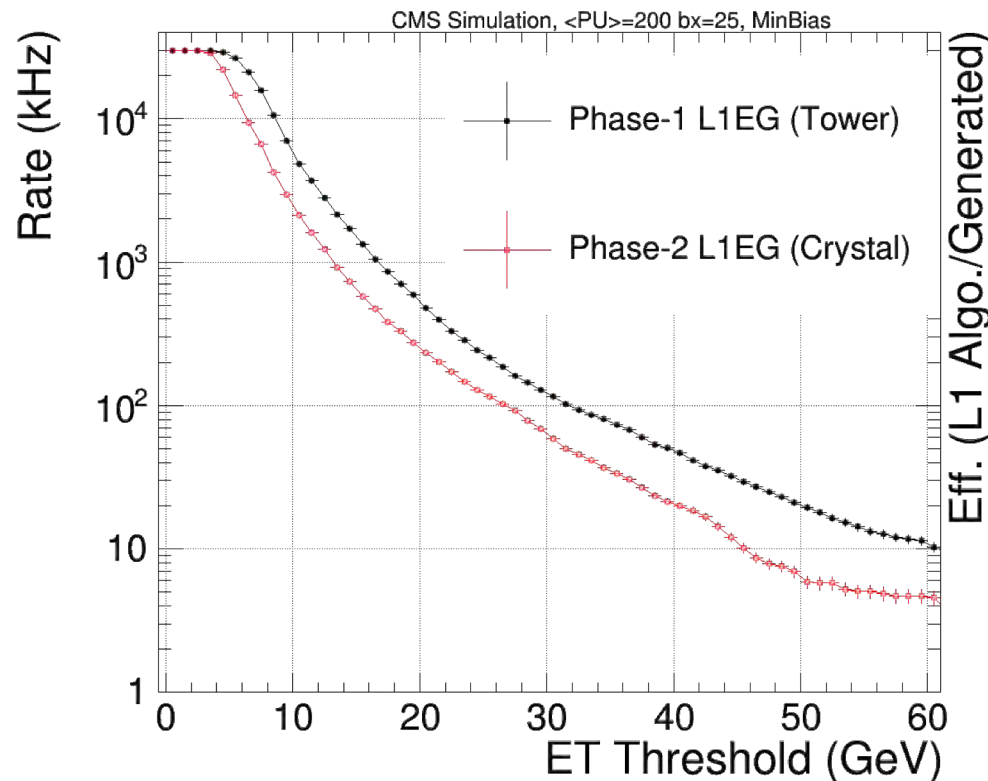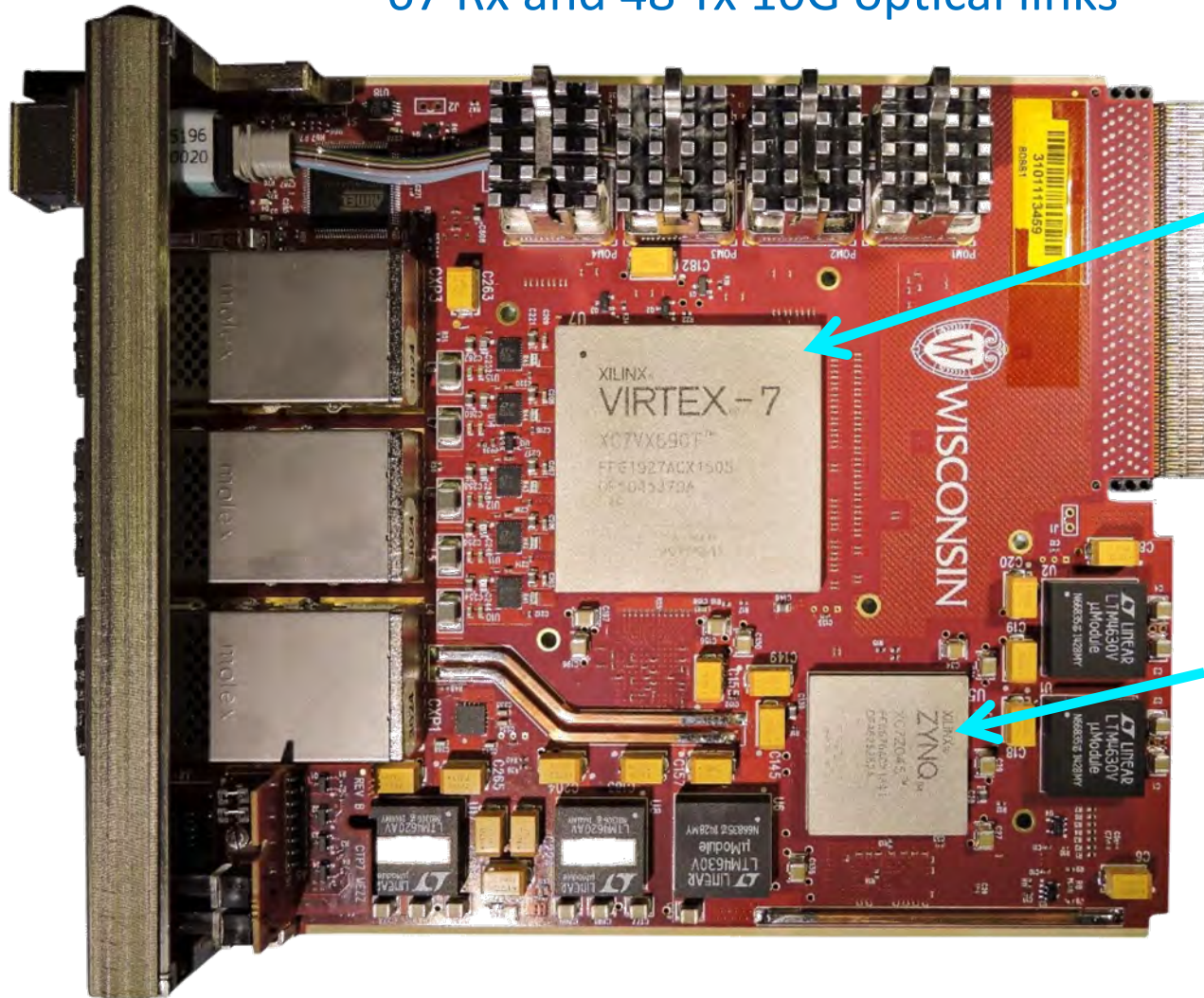
Calorimeter Trigger Performance

- **Track-Linked Calorimeter Trigger L1 e/ɣ Object shows more than an order of magnitude rate improvement over the Phase-1 algorithm at PU of <200> with 5% loss in efficiency.**
  - Tracking and Algorithm R&D is ongoing to improve efficiency
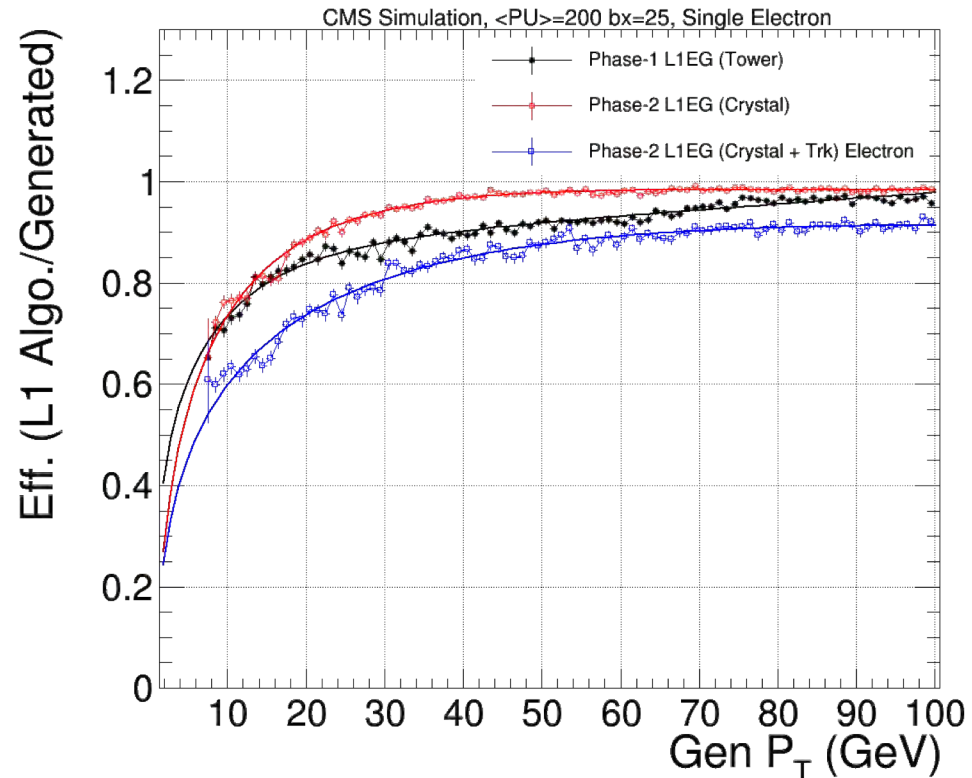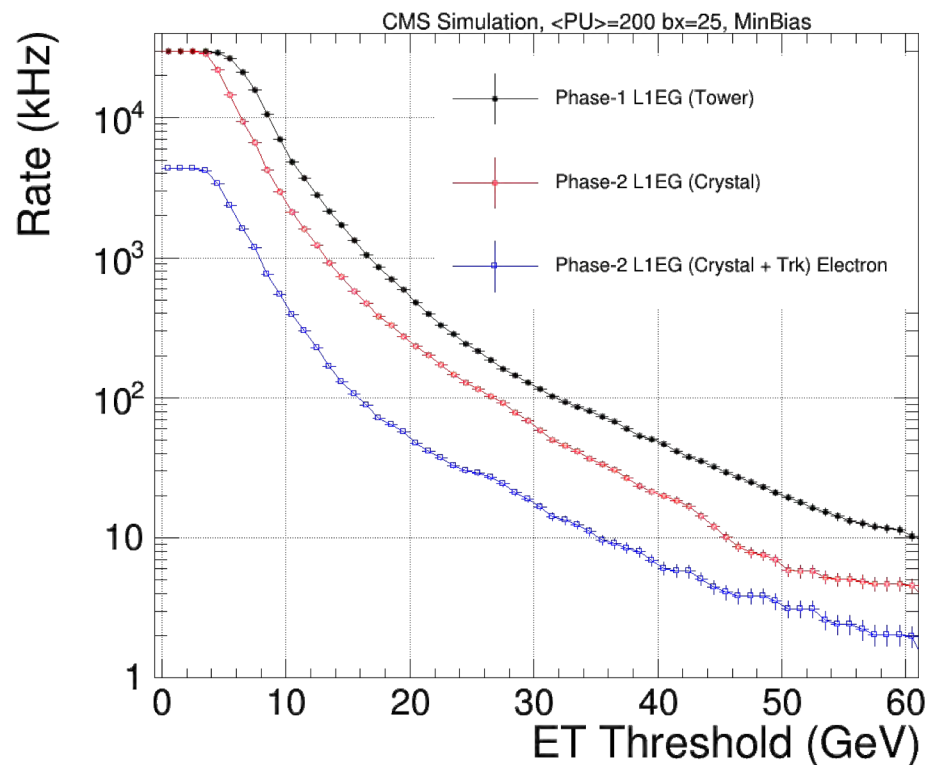
Gen-0 (μTCA) Demonstrator: U. Wisconsin CTP7 Card for Phase 1 Cal. Trig.

- 12 MGT MicroTCA backplane links
- 67 Rx and 48 Tx 10G optical links


Virtex-7 690T FPGA (Data Processor)

ZYNQ `045 System-on-Chip (SoC) Device (embedded Linux control platform)

CTP7 Deployment Phase 1 & HL-LHC

- U. Wisconsin

- **Production:**
  - 50 Boards

- **Phase 1 L1 Trigger Deployment:**
  - Stage 1 and Stage 2 Layer-1 Calorimeter Trigger
  - 22 CTPs including hot spares
  - Stage-1 was main calorimeter trigger for 2015
  - Stage-2 operating in parallel since Sept. 2015 – main cal. Trig. for 2016

- **HL-LHC R&D: Tracklet Trigger Setups**
  - Identical 4-card CTP7 configurations at CERN and Cornell
  - Used for algorithm firmware development and testing

- **HL-LHC Cal, Correlator Trigger prototypes: platforms for FW development and testing**
  - FNAL, CERN, Wisconsin

- **HL-LHC EMU, HB/EB Cal Readout, Trigger prototypes: FW development and testing**
  - CERN, FNAL, Rutgers, Princeton, Texas A&M, UCLA, Virginia
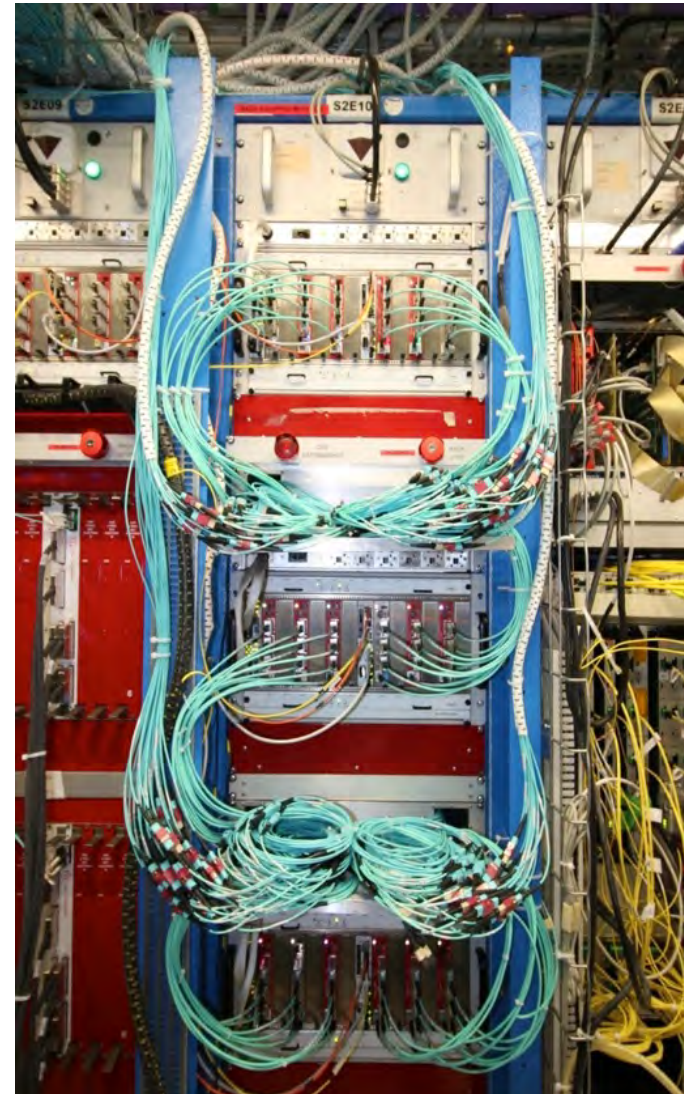
CTP7 introduces HL-LHC technologies

- **Embedded Linux**
  - Functional Linux system (network, file system, shell)
  - Low latency access point tightly integrated with workhorse FPGA
  - Basic card level infrastructure with very little new code—Ethernet, I2C, USART, GPIO drivers, ssh, file system, etc.—all standard
  - Paid for itself in time saved in the first project cycle
    - First CTP7 proto. power-up to integrated operation in CMS pp runs in 21 months

- **AXI Architecture**
  - Open, industry standard on-chip interconnection scheme for SoCs and FPGAs
  - Straightforward to implement AXI interfaces for registers and memory
  - AXI infrastructure bridged into the Virtex-7 ("Chip2Chip" core), a single integrated address space for both devices
  - 95% of CTP7 generic infrastructure from ZYNQ hard cores and Library IP catalog, no custom HDL needed—it's in the tools
  - Improved status and access to advanced applications
    - Real-time link eye-diagrams for all channels while taking data available online!
    - http://www.hep.wisc.edu/wsmith/cms/doc15/UW_Phase2_HWR&D_12Nov2015.pptx

- **XVC – Embedded Linux Xilinx Virtual Cable (e.g. JTAG)**
  - Debug Card at P5 via TCP/IP just as if on the bench in the lab

ATCA Hardware Demonstrator

- U. Wisconsin

- Explore hardware technologies targeted for the Phase 2 upgrade
  - ATCA Form Factor including Rear Transition Module
  - MGT Link design beyond 10G line rates (16G, 25G)
  - Efficient cooling of next-gen FPGAs
  - Next generation IPMI and embedded Linux solutions
  - Advanced RAM/FPGA interconnections (U. Florida)

- General ATCA technology demonstrator, with emphasis on Trigger applications
  - Powerful performance with flexibility
  - Closely related to the ECAL Demonstrator

- Specifications:
  - Single FPGA Design, C2104 Package
  - $\geqq$ 100 Optical Links — Firefly optical modules
    - 14/16G with options to test 25G links as well.
  - Approximately 24 Links to RTM for enhanced versatility
    - RTM includes some of optical links above
  - Embedded Linux and IPMI Controller on Mezzanines
  - Deep Memory Mezzanine

- Test the full chain
  - Calorimeter BE → Calorimeter Trigger → Correlator

APd1 ATCA Card

- U. Wisconsin

- **APd1 (Advanced Processor demonstrator #1):**
  - APx-family card for Phase 2 Trigger: Calorimeter, Correlator, Muon.
  - Demonstrator for a multi-purpose, customizable, common processing platform, suitable for wide-scale use in CMS back end and trigger subsystems
  - Extension of the popular and successful CTP7*-style architecture (Linux & ZYNQ/Virtex)architecture into ATCA on ZYNQ/Virtex Ultrascale/+
  - Customizable via high performance Rear Transition Modules (RTMs) and memory mezzanines (U. Florida)

- **Single Virtex Ultrascale+ VU9P device per board**
  - XCVU9P-compatible, C2104 package
  - Optics: Samtec Firefly Modules with either 12 transmitters or 12 receivers per module (up to 16 Gbps) and 4 transmitter plus 4 receiver modules (up to 28 Gbps) (U. Florida)

- **In design now**

- **Specs written for:**
  - Large LUT Mezzanine Interface and RTM Interface
  - Control Interfaces (ELM, IPMC, 1G/10G Ethernet)
  - Power Distribution and Internal Clock Distribution

- **DTH Interface work in progress**
  - CMS Central DAQ and Trigger/Timing/Control Interface Card
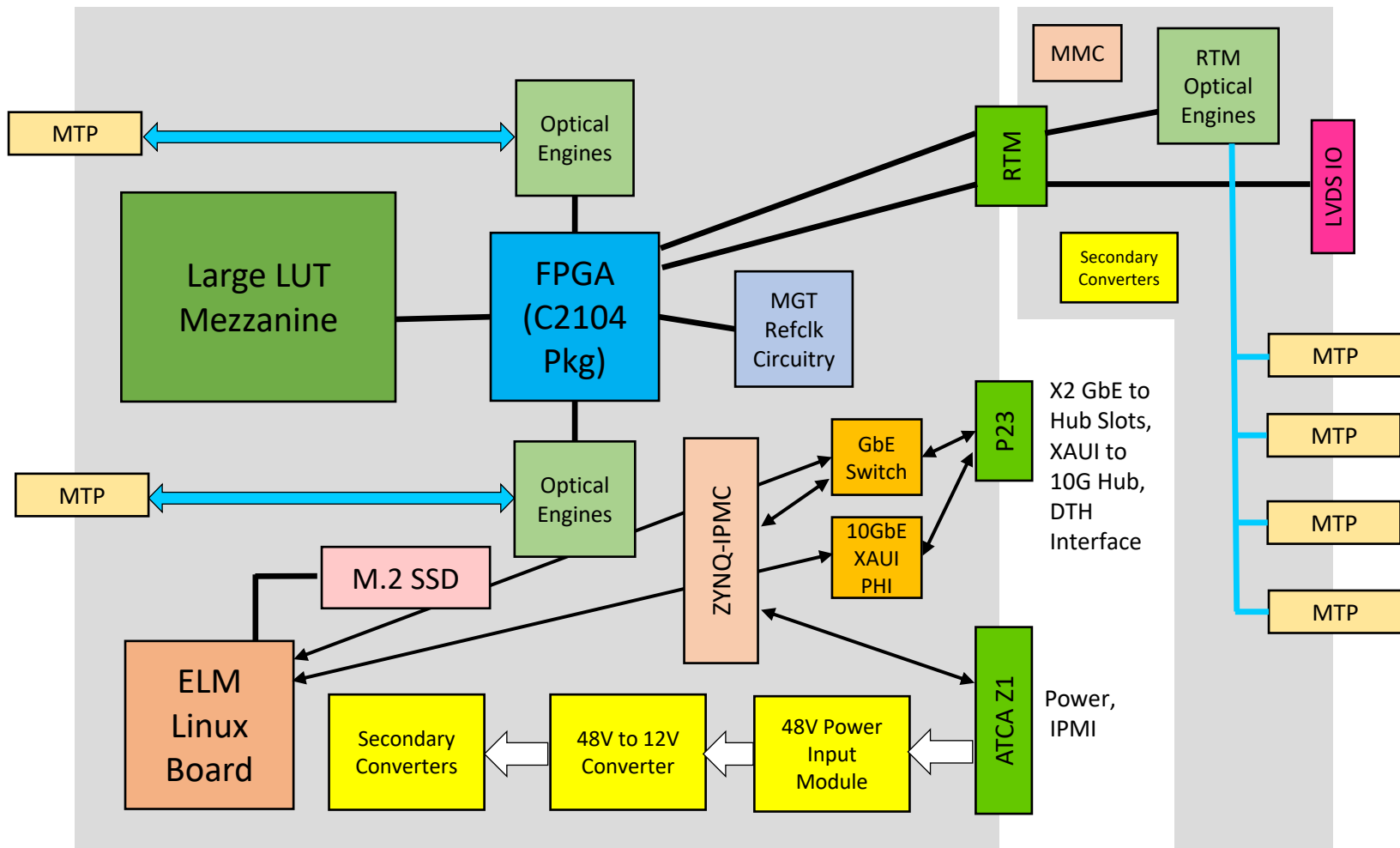
The APx Consortium

- Pooling of efforts in ATCA Processor hardware, firmware and software development

- Multiple ATCA processors and mezzanine board types

- Modular design philosophy, emphasis on platform solutions with flexibility and expandability

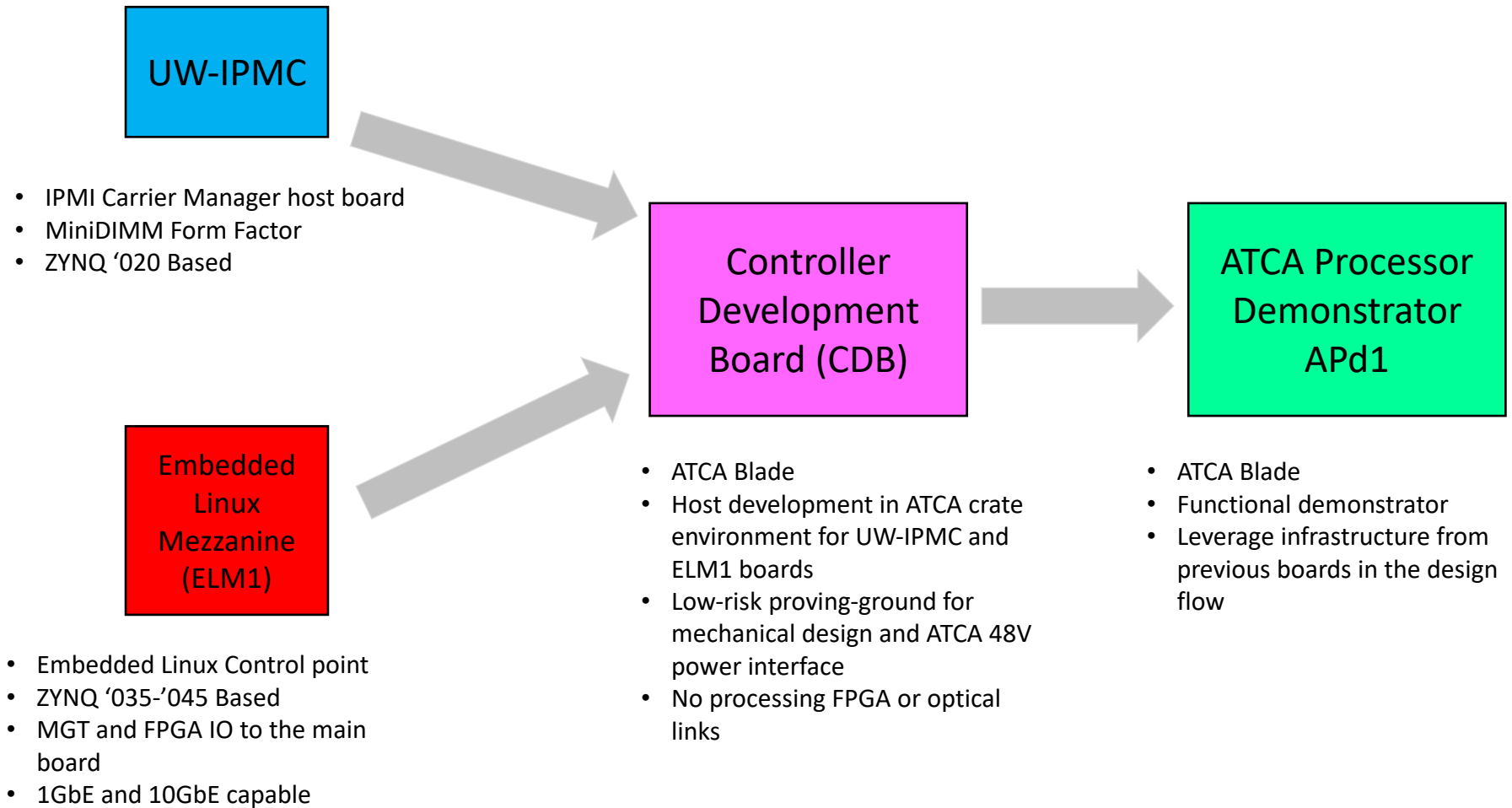- Reusable circuit, firmware and software elements

APd1+LUT+RTM Block Diagram

Control Infrastructure

- **Recurring elements in ATCA boards:**
  - IPMI Endpoint—IPMC
    - Negotiates with crate for power, connectivity
    - Controls power, monitors board conditions via sensors
    - Provides lower level configuration support (e.g., boot control)
  - Embedded Linux Endpoint
    - Provides higher level configuration support (booting FPGAs, configuring memories, clocks, optics, etc.)
    - Acts as primary network-connected TCP endpoint on the board during online operation
  - Ethernet Switch—connects the on-board endpoints such as the Linux & IPMC to the crate switch in an ATCA hub slot via backplane connection (1000BASE-T is standard)

U. Wisconsin

UW-IPMC

- IPMI Carrier Manager host board
- MiniDIMM Form Factor
- ZYNQ '020 Based

Embedded Linux Mezzanine (ELM1)

- Embedded Linux Control point
- ZYNQ '035-'045 Based
- MGT and FPGA IO to the main board
- 1GbE and 10GbE capable

Controller Development Board (CDB)

- ATCA Blade
- Host development in ATCA crate environment for UW-IPMC and ELM1 boards
- Low-risk proving-ground for mechanical design and ATCA 48V power interface
- No processing FPGA or optical links

ATCA Processor Demonstrator APd1

- ATCA Blade
- Functional demonstrator
- Leverage infrastructure from previous boards in the design flow

ZYNQ-IPMC Hardware

- 244-pin MiniDIMM form factor

- Single +3.3V power supply (runs off of ATCA management power)

- Mounts to main board using angled connector

- ZYNQ XC7Z020, with 256 MBytes of DDR3 RAM

- Dedicated 16 ADC channels (16-bit) for fast response signal monitoring

- ~100 3.3V configurable IOs in ZYNQ PL section

- Design to be fully published, schematics, PCB, artwork, BOM, for independent production

ZYNQ-IPMC in Test Fixture

ZYNQ-IPMC Test Fixture Top View

ZYNQ-IPMC Software

- FreeRTOS-based runtime environment

- Cortex-A @ 600+ MHz backed by 256MB of RAM is a radical upgrade in resources compared to typical IPMC hardware platforms

- Can take a true object-oriented approach to the design without performance penalty—simplifies rendering of design blocks into working code

- 60% complete—base drivers, message service, IPMC core framework, console interface & parser, nonvolatile data service all coded, implementing individual commands now

- Code to be released under GPL, <u>no NDA required</u> to use/reference

IPMC Console

```cpp
/**
 * An IPMBSvc driver.
 */
class IPMBSvc {
public:
    const std::string name; ///< The name used for this IPMB in StatCounter or Task names, as well as l
    IPMICommandParser *command_parser; ///< The command parser used for incoming messages.

    IPMBSvc(IPMB *ipmbA, IPMB *ipmbB, uint8_t ipmb_address, IPMICommandParser *command_parser, LogTree
    virtual ~IPMBSvc();

    static uint8_t lookup_ipmb_address(const int gpios[8]);

    /**
     * The supplied function will be called when a response to this outgoing
     * message is received, or when delivery is aborted.
     *
     * \note This will not be called for outgoing response messages except in
     *       the case of inability to transmit.
     *
     * \param original The original IPMI_MSG transmitted.
     * \param response The response IPMI_MSG received, or NULL if delivery aborted.
     */
    typedef std::function<void(std::shared_ptr<IPMI_MSG> original, std::shared_ptr<IPMI_MSG> response)> response_cb_t;

    void send(std::shared_ptr<IPMI_MSG> msg, response_cb_t response_cb = NULL);
```
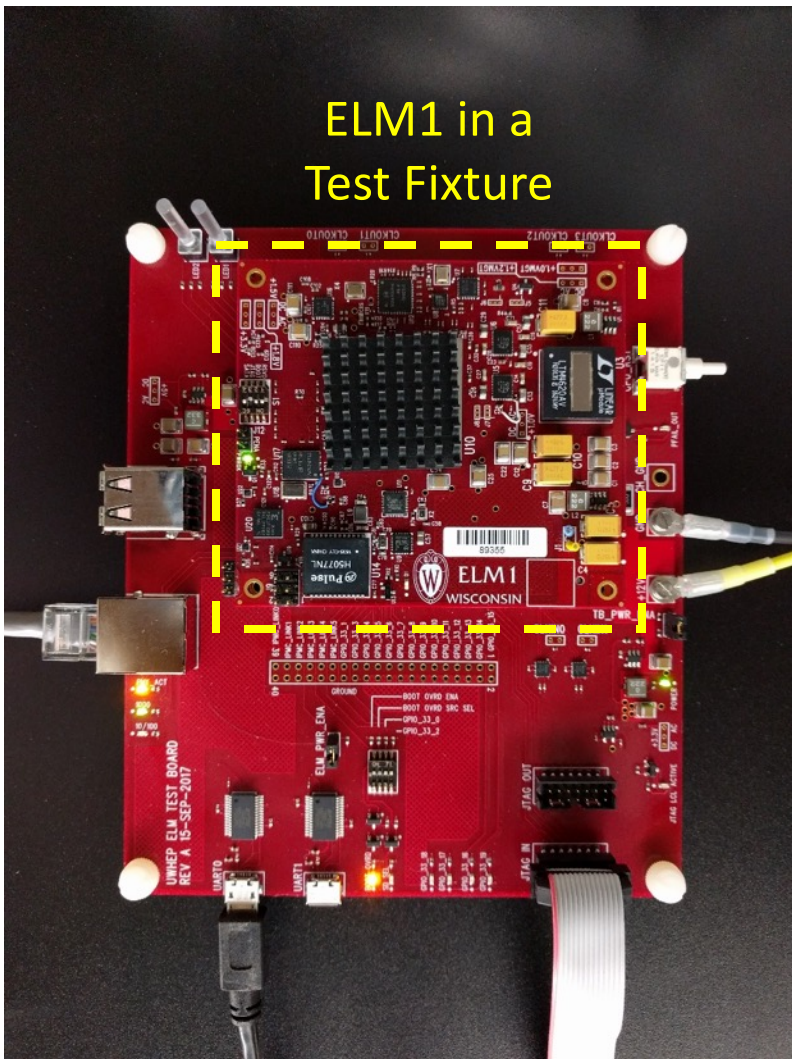
```
[NOTI] Our IPMB0 hardware address is 72h
[NOTI]
*****************************************************
University of Wisconsin IPMC f60c7d1

M Vivado/ipmc_zynq_vivado.sdk/common/uw-ipmc/IPMC.cc

[INFO] Request received on ipmb0:  0.20 -> 0.72: 06.01 (seq 01) []
[NOTI] Request received on ipmb0:  0.20 -> 0.72: 06.01 (seq 01) []  (duplicate)
[NOTI] Request received on ipmb0:  0.20 -> 0.72: 06.01 (seq 01) []  (duplicate)
> ps
PID Name              BasePrio CurPrio StackHW CPU% CPU
  4 IDLE                     0       0     155  99% 2167133
  2 ipmb0                    4       4    1319  <1% 2350
  3 console                  3       3    1479  <1% 295
  1 PersistentFlush          1       1    1783  <1% 92
  5 tmrd                     5       5     401  <1% 55
[NOTI] Request received on ipmb0:  0.20 -> 0.72: 06.01 (seq 01) []  (duplicate)
>
```

ELM1 Board

ELM1 in a
Test Fixture

- "ELM": Embedded Linux Mezzanine

- 84mm x 75mm form factor

- ELM1: 7-Series ZYNQ, XC7Z045-2 (8 GTX MGTs)

- Programmable IO: >24@3.3V, 74@1.8V

- 4 Rev A boards built. Design is fully functional, with some wires

- 9 ZYNQ devices on hand for additional ELM1 builds

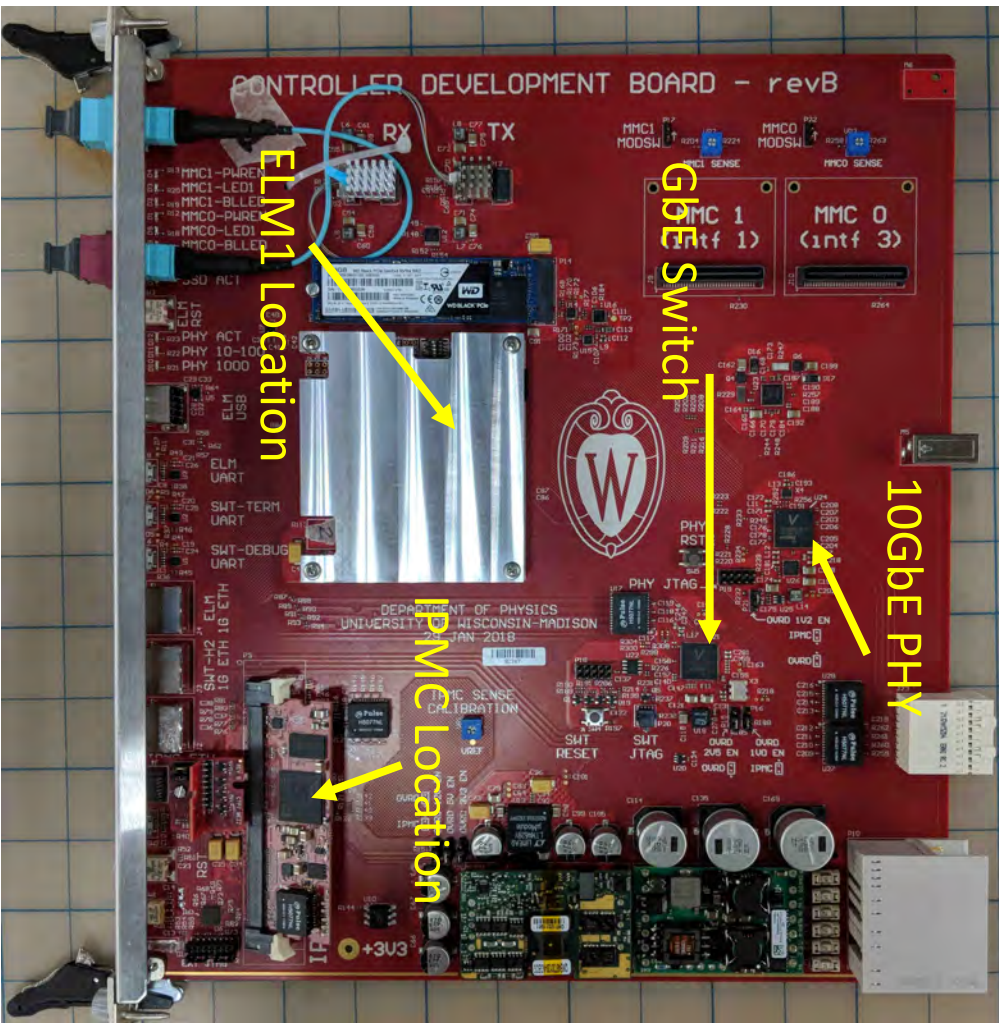- ELM2: ZYNQ Ultrascale+ (2019)

Controller Development Board

- ATCA Development Board for control infrastructure (ELM, IPMC, GbE Switch, 10GbE XAUI/XFI PHY)

- ELM MGT allocation: 6 lanes to Fireflys, 1 lane to SSD, one lane to 10GbE PHY

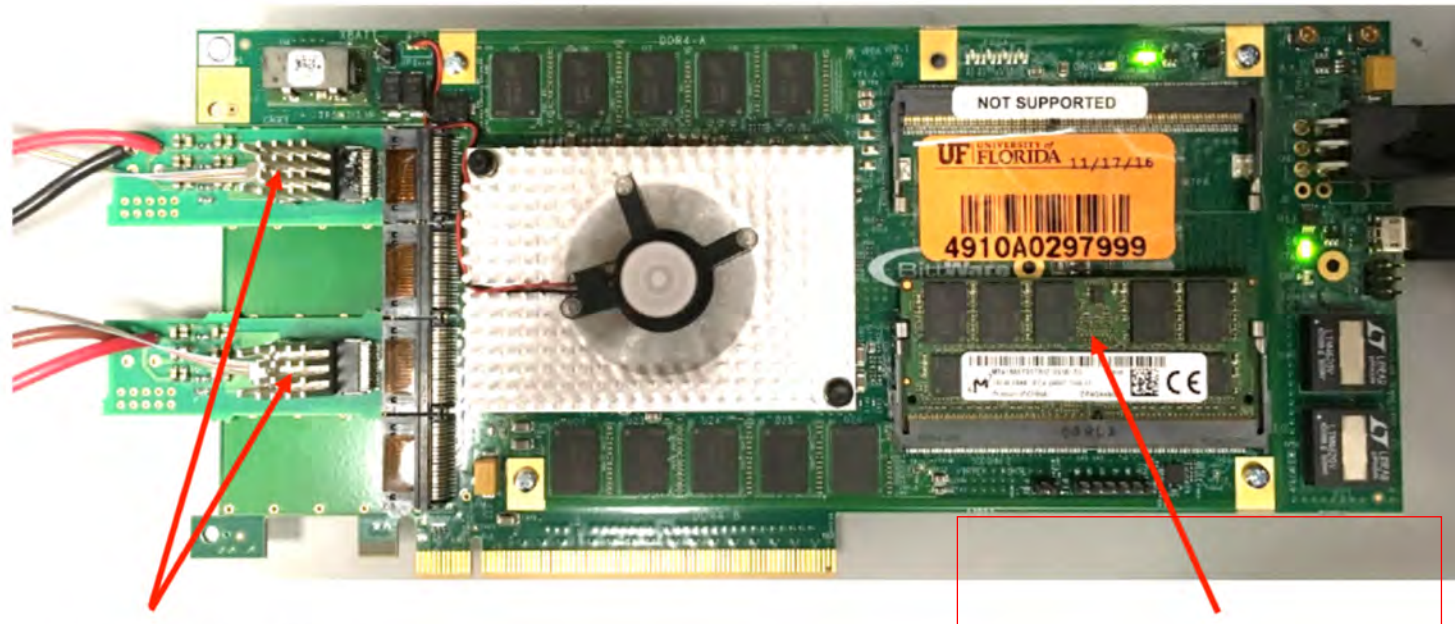- Built and in use for tests (next slides)
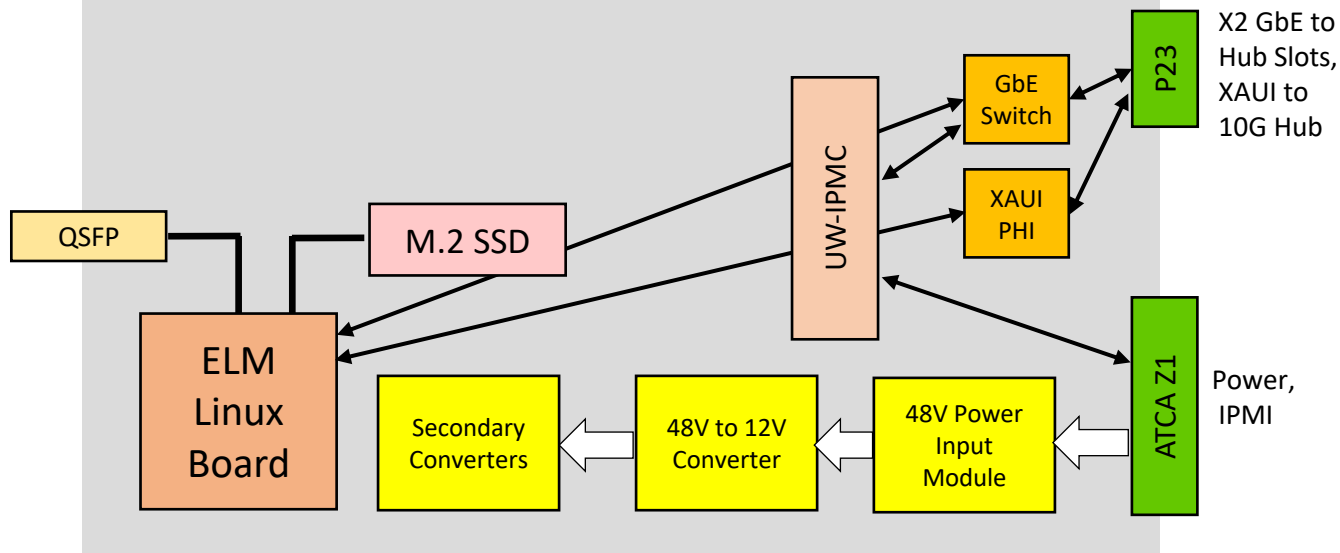
Controller Development Board Status

■ 3 Boards produced, under test

DDR4 Memory R&D

- In baseline design for Correlator and Muon Triggers
- Tested DDR4 memory (16 GB) with a Xilinx Ultrascale+ FPGA evaluation board XUSP3S
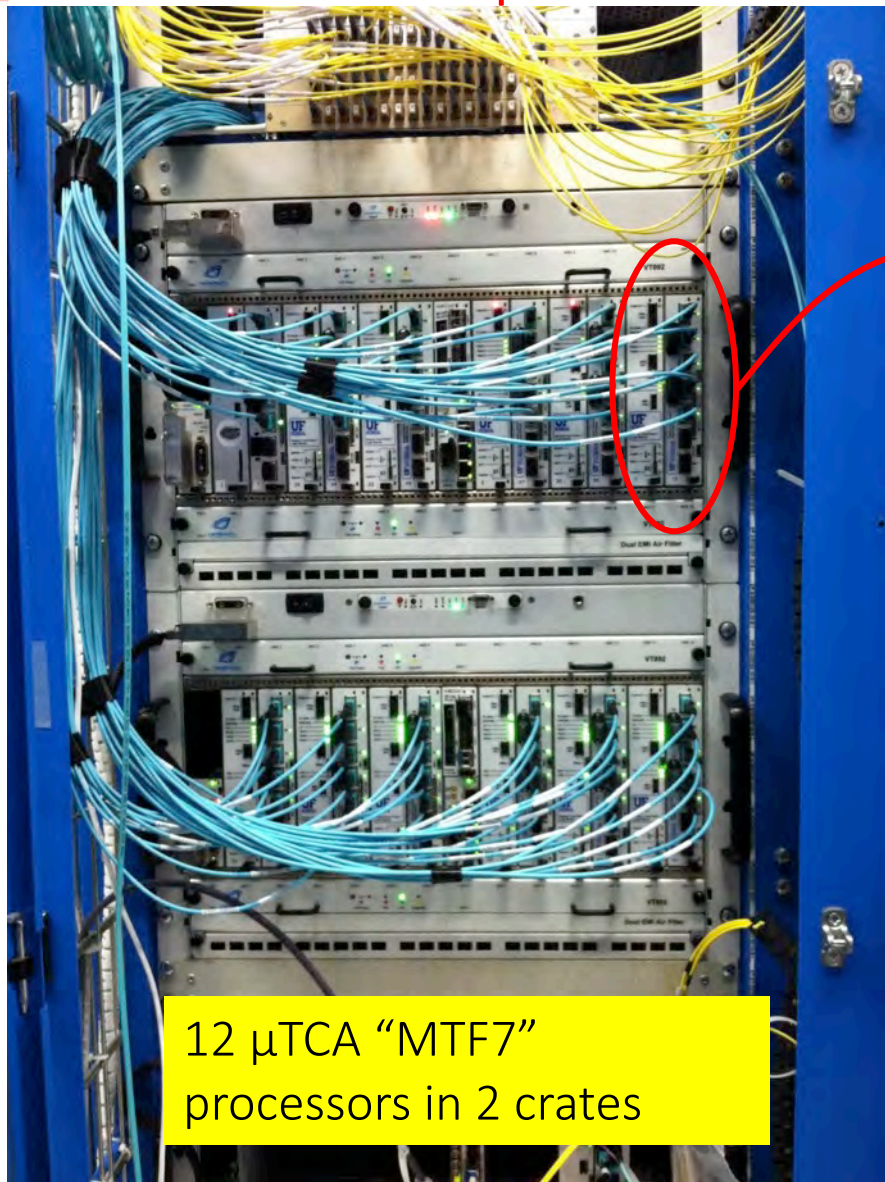

FireFly optical links

DDR4 SODIMM 16GB

FireFly links are inserted instead of QSFP+ modules using adapters
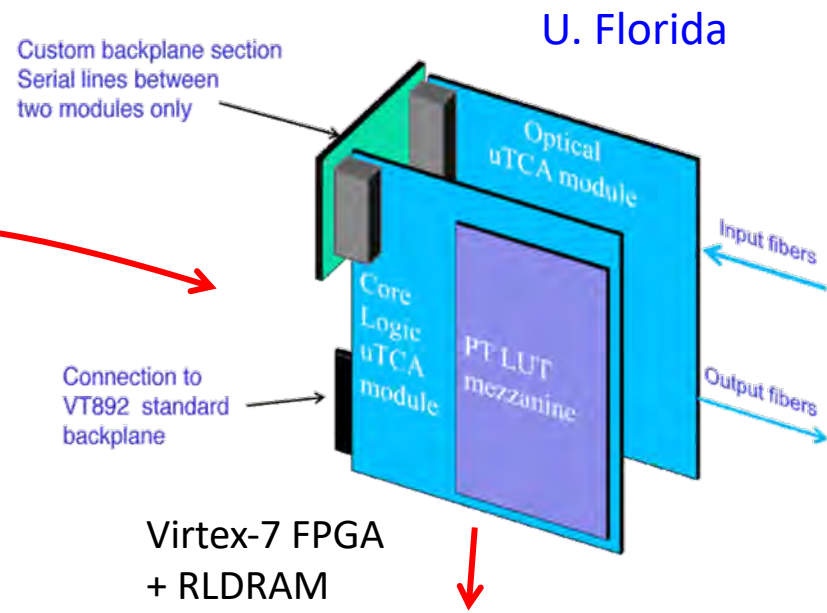
- Conclude that DDR4 memory is suitable for use in the trigger, and allows us to reach very large memory bank sizes (64 GB).

Memory Mezzanine similar to Phase-1 Endcap Muon Track Finder PT LUT Mezz.

U. Florida

Custom backplane section
Serial lines between
two modules only

Optical uTCA module

Input fibers

Core Logic uTCA module

PT LUT mezzanine

Connection to
VT892 standard
backplane

Output fibers

Virtex-7 FPGA
+ RLDRAM

12 µTCA "MTF7"
processors in 2 crates

Optical Link R&D

- Test of Firefly optical links at 14 and 26, 28 Gbps with same Xilinx Ultrascale FPGA evaluation board

- Add transmission through a 15 cm differential line and Impel connectors (to mock-up connection from RTM) and through a 15 cm Firefly optical fiber, with PRBS-31
  - Uses resynchronization circuitry (CDR)

Optical Link R&D
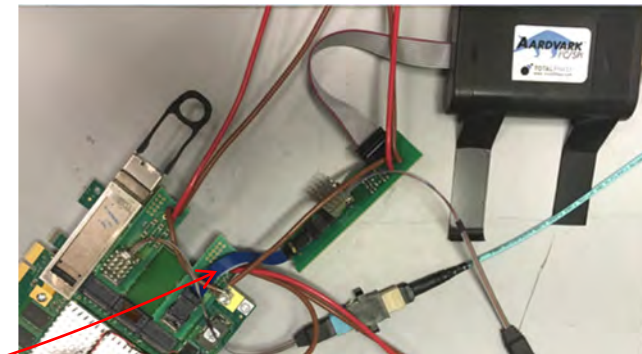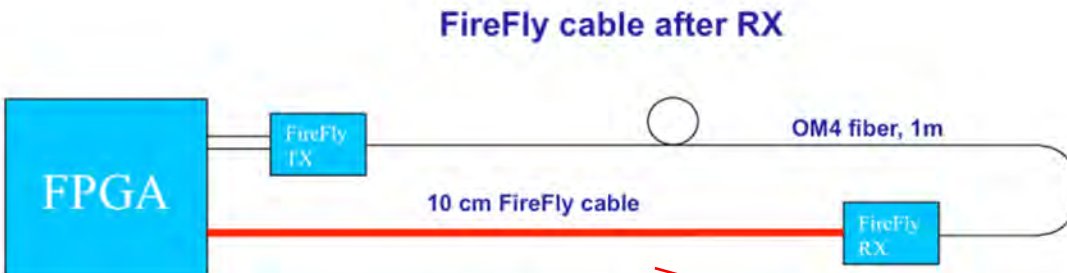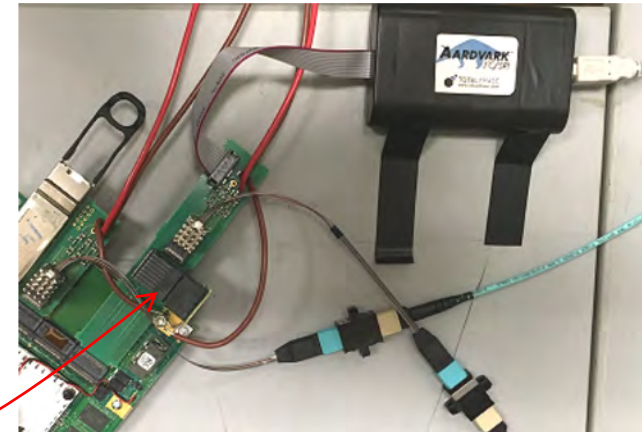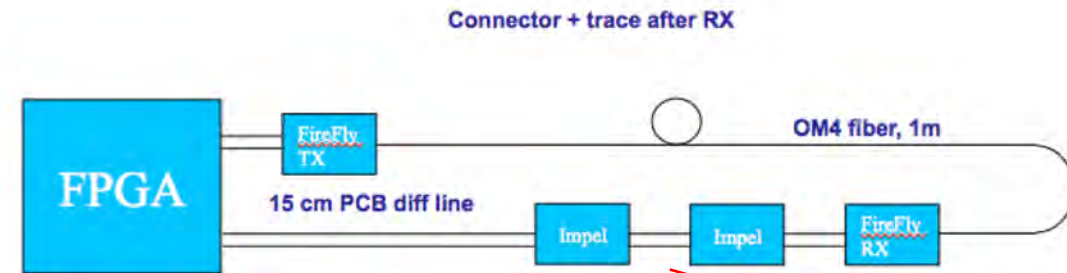
- **Firefly works at 14G or 28G**

  - Endcap Muon, Correlator, Calorimeter Triggers require only up to 16G
    Barrel Muon Trigger up to 25G

  - Can be used on RTM or mezzanines

  - Can be attached to FPGA via high-speed connectors or cables

With
connectors
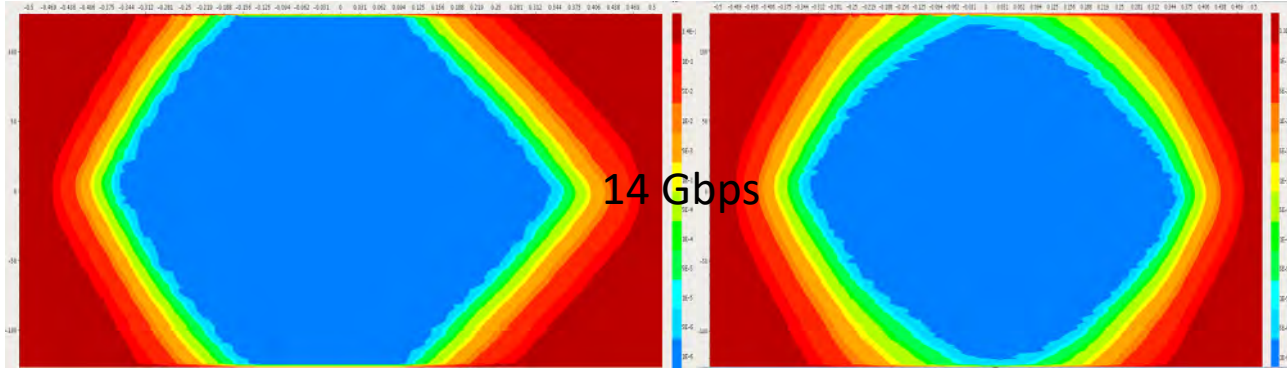
14 Gbps

With Firefly
optical cable

26 Gbps

Firmware R&D

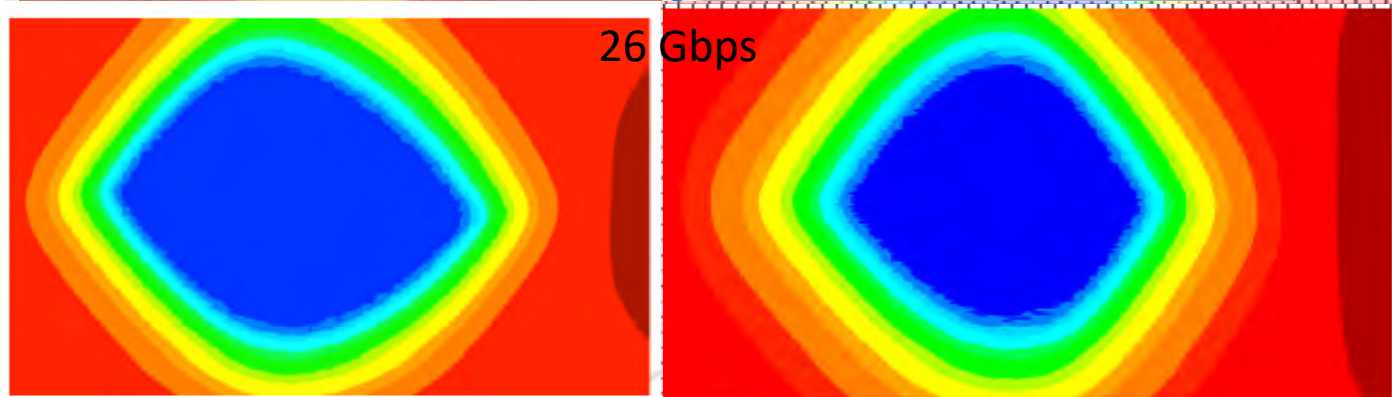- **Makes use of High Level Synthesis (HLS) Tools**
  - HLS is an automated design process that interprets algorithm specification at a high abstraction level and creates digital hardware/RTL code that implements that behavior.
  - HLS significantly accelerates design time while keeping full control over the choice of optimal architecture exploration, proper level of parallelism and implementation constraints.
  - Reduces overall verification effort
  - Using Xilinx Vivado HLS
    - Complete design environment with abundant possibilities in the form of pragma directives to fine-tune hardware generation process from High Level Language (HLL) to Hardware Description Languages (HDL)
    - Packages implementation files as an IP block for use with other tools in the Xilinx design flow.
    - C/C++ libraries contain functions and constructs optimized for implementation in an FPGA.
    - Using these libraries helps to ensure high Quality of Results (QoR)

Firmware Demonstrator

- **Complete and realistic Phase-1 Calo Layer-2 trigger algorithm set:**
  - Pileup subtraction at 4x4 region level lookup using PUM
  - eGamma, separately sorted relaxed and isolated candidates
  - Tau, separately sorted relaxed and isolated candidates
  - 12x12 jets, separately sorted central and forward candidates
  - Energy Sums (Total ET, MET, MHT, HT)

- **Compare with test Calo Stage-1 Layer-2 project (done in VHDL):**
  - Both projects target the single Virtex-7 690T FPGA used in Phase-1.
  - Algorithms/physics performance significantly better with 4x finer resolution
  - Similar FPGA resource utilization
  - Algorithm latency improvement: 11 vs 20 BX
  - Implementation time: 6 weeks vs 1.5 year

- **Very encouraging result → justifies using HLS technology in Phase-2 algorithm development**
  - However, FW development effort estimate remains based on actual Phase 1 effort with no anticipated development time savings from HLS

Vivado HLS Performance and Utilization estimates

- **Example of Firmware usage study in Phase 1 and Phase 2**

Name	Virtex-7 690T				Virtex UltraScale+ VU9P			
	BRAM18K	DSP48E	FF	LUT	BRAM18K	DSP48E	FF	LUT
DSP	-	-	-	-	-	-	-	-
Expression	-	-	0	21934	-	-	0	29153
FIFO	-	-	-	-	-	-	-	-
Instance	-	-	142188	97904	-	-	134985	96976
Memory	-	-	-	-	-	-	-	-
Multiplexer	-	-	-	26229	-	-	-	28677
Register	-	-	53300	9840	-	-	56513	10095
Total	0	0	195488	155907	0	0	191498	164871
Avialable	2940	3600	866400	433200	4320	6840	2364480	1182240
Ulitization(%)	0	0	22	35	0	0	8	13

- **Calculation of clusters included above**

Device	Latency		Interval		Pipeline Type	Clock
	min	max	min	max		
Virtex-7 690T	53	53	6	6	Function	240 MHz
Virtex UltraScale+ VU9P	72	72	8	8	Function	320 MHz

- **For both devices, absolute latency of 8.8 BX is obtained**

R&D Milestones

- 2018 Q2 (30-June-2018): ATCA Control Infrastructure Mezzanine First SW/FW release

- 2018 Q3 (30-September-2018): APd1 Produced

- 2018 Q4 (31-December-2018): APd1 Data connectivity test

- 2019 Q1 (31-March-2019): APd1 first FPGA firmware infrastructure release

- 2019 Q2 (30-June-2019): UW-IPMC rev.2 design complete

- 2019 Q3 (30-September-2019): ELM2 design complete

- 2019 Q4 (31-December-2019): Subsystem Interconnect test
  - Calorimeter BE → Calorimeter Trigger → Correlator

- 2020 Q1 (31-March-2020): APd2 design complete

- 2020 Q2 (30-June-2020): ATCA Control Infrastructure Mezzanine Second SW/FW release

- 2020 Q3 (30-September-2020): APdx second FPGA firmware infrastructure release

- 2020 Q4 (31-December-2020): Pre-production Complete

Calo. Trigger Technical Summary

- **Barrel Calorimeter Trigger Upgrade meets technical performance requirements**

- **Designs are based on similar technologies to Phase-1**

- **Upgrade uses common ATCA hardware platform and components also used by other CMS systems**

- **Firmware + software development evolves from Phase-1**
  - Uses High Level Synthesis (HLS) tools creates efficient FW designs linked closely to algorithm simulation.

- **Initial R&D program prototyping demonstrates interfaces and controls**

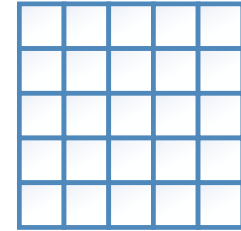# Backup

ECAL Input Information

- **ECAL crystal level information:**
  - 10 bits for energy (Et),
  - 1 bit for the spike flag,
  - 5 bits for timing.
- **Total of 16 bits/BX per crystal.**

1x1 ECAL region

at the trigger

- **An ECAL tower is defined as a 5x5 crystal matrix:**
  - Totalling in **400 bits/BX per tower** (25x 16 bits/BX).

- **Each ECAL BE processor FPGA will process 3η x 4φ or 2η x 4φ towers, or regions.**
  - Totalling in **4800 bits/BX for each 3x4 region** (3x4 x 400 bits/BX).
 - Or, **3200 bits/BX for each 2x4 region** (2x4 x 400 bits/BX).

ECAL-Trigger Fiber Count

- **Fiber requirement per region type:**
  - 3x4 region: 4800 bits/BX/region / 352 bits/BX/packet
    - = 13.6 fibers -> Reserve **15 fibers**.
  - 2x4 region: 3200 bits/BX/region / 352 bits/BX/packet
    - = 9.1 fibers -> Reserve **10 fibers**.

- **Each Layer-1 card will process the data from a super-module (17x4 region):**
  - 85 fibers from ECAL (five 3x4 and one 2x4 region).
  - 4 fibers from HCAL (one 16x4 region).

- **Data packaging optimization under study**
  - Baseline: each group of 5 fibers carries the data of 1x4 strips, or 20 crystals per fiber, easy payload mapping.

ETA (η)
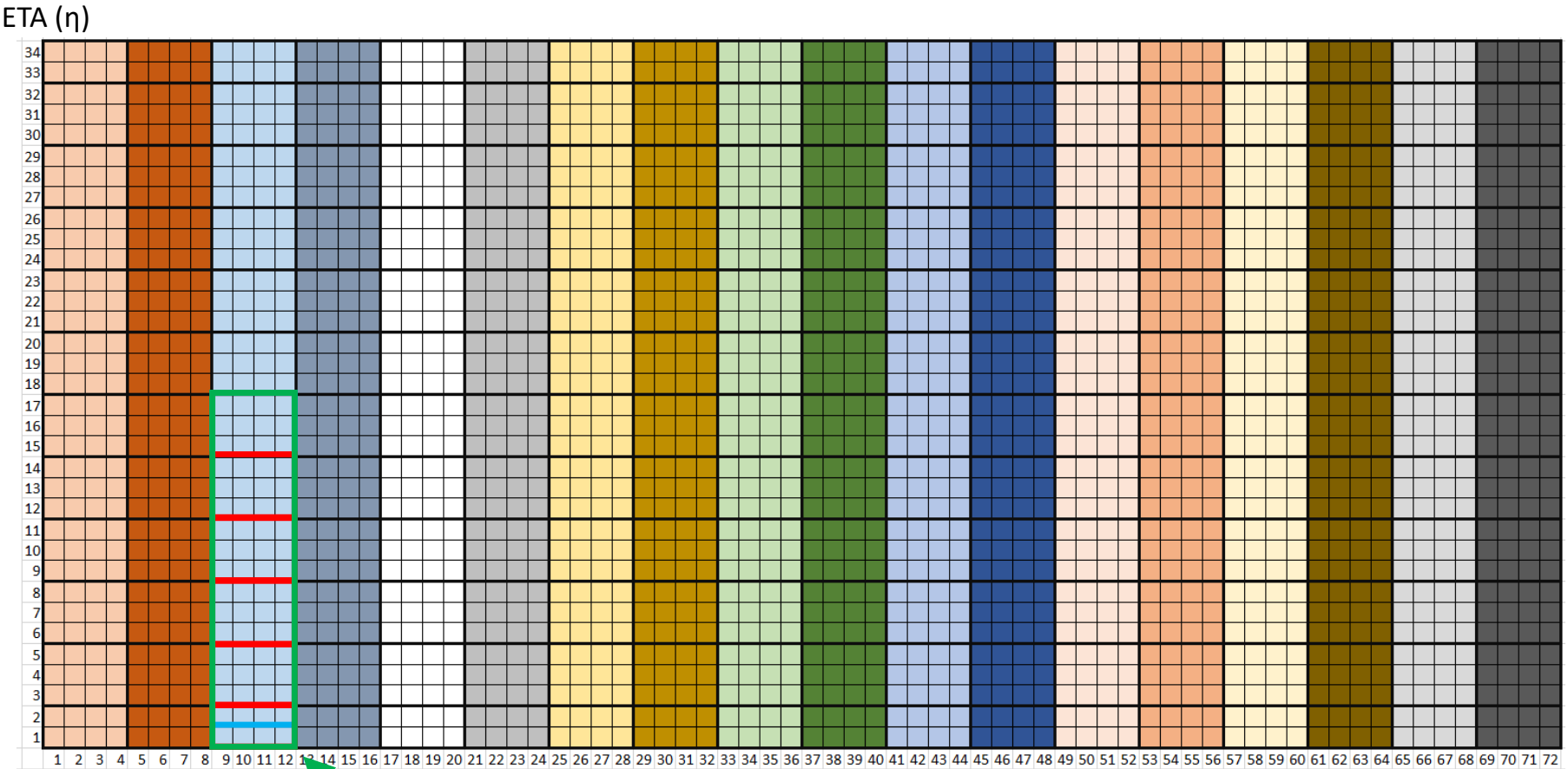
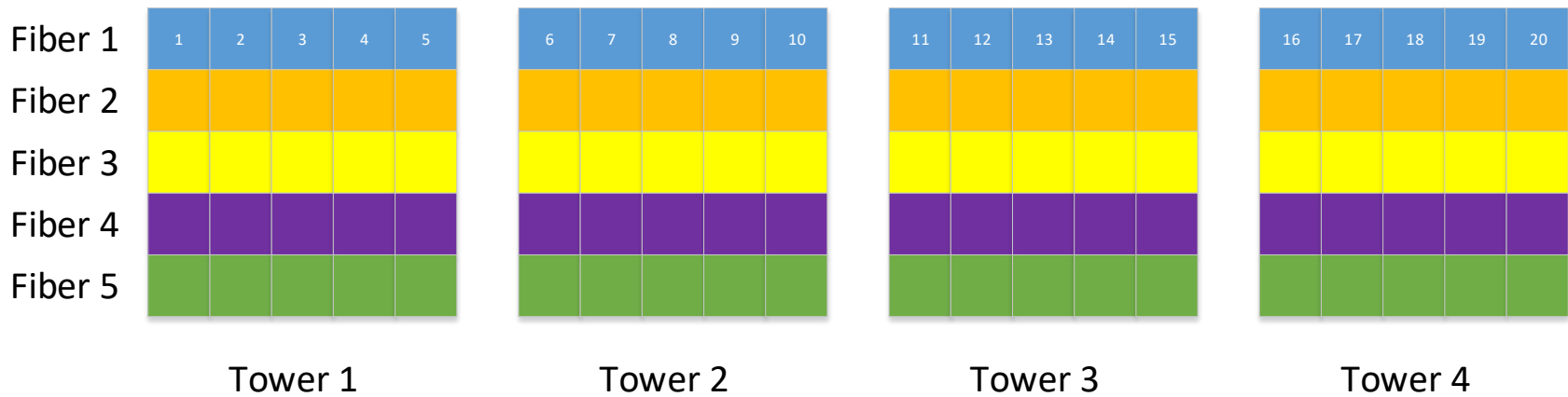17x4 layer-1 region – total of 36 regions

PHI (φ)

Studied payload mapping

Stream in this direction →


Tower 1 Tower 2 Tower 3 Tower 4

	Byte							
	1	2	3	4	5	6	7	8
Word 1	Header		Crystal 1		Crystal 2		Crystal 3	
Word 2	Crystal 4		Crystal 5		Crystal 6		Crystal 7	
Word 3	Crystal 8		Crystal 9		Crystal 10		Crystal 11	
Word 4	Crystal 12		Crystal 13		Crystal 14		Crystal 15	
Word 5	Crystal 16		Crystal 17		Crystal 18		Crystal 19	
Word 6	Crystal 20		Unassigned				CRC	

Layer-1 to Layer-2 Mapping

3 Layer 2 cards receive information from 36 Layer1 cards
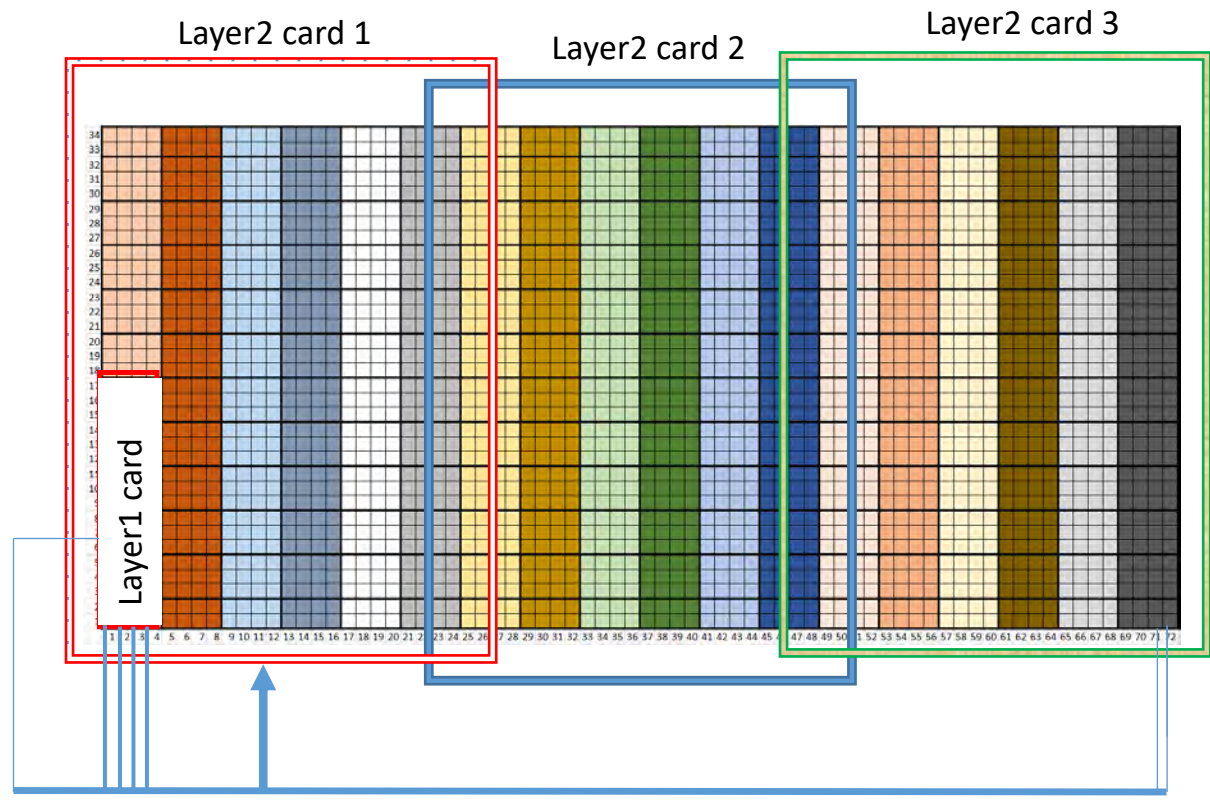
Each Layer 1 card sends out 4x1 "phi" links, each contains 17 towers x 16 bits + 2 clusters x 40 bits, and has 1-4 links to Layer 2 for additional information, each Layer 2 card receives 28 "phi" links x 2 in eta = 56 + has capacity to receive up to additional 40 links, each link can transmit up to 352 bits/BX

Output to Correlator, Global Trig.

- ## Correlator:
  - ### 2x2 Tower-Cluster Data format with 96-bit width:
    - 10-bit ET of the full 2x2 region
    - 7-bit Energy-weighted Position identifying the centered crystal
    - 15-bit Cluster summary, E/H, time
  - ### 4 clusters, each containing:
    - 9-bit ET of the highest cluster in 2x2 region
    - 7-bit Energy-weighted Position identifying the centered crystal

- ## Global Trigger:
  - ### Leading isolated electrons/photons
  - ### Leading jets
  - ### Leading taus
  - ### Sums: E_T, H_T, E_{TMIss}, H_{TMIss}

Key Performance Parameters

- **Threshold:**
  - The project shall design, produce, and test the electronics required for receiving data from the barrel calorimeter, processing them for L1 trigger reconstruction, and transmitting output to the Correlator Trigger and DAQ. The trigger shall be validated, based on simulated test data patterns from MC verified against detector readout data, to give an average factor of four reduction of electron, photon and tau trigger object rates, after combination with track trigger simulated data, with respect to the Run-2 system with less than 20% efficiency loss.

- **Objective**
  - The trigger shall be validated, based on simulated test data patterns from MC verified against detector readout data, to give an average factor of four reduction of electron, photon and tau trigger object rates, after combination with track trigger simulated data, with respect to the Run-2 system with less than 15% efficiency loss. The trigger will be installed, commissioned, and calibrated, with the overall CMS upgraded trigger

Major System Tests

- **Subsystem interconnect test at the end of CY19:**
  - Prototypes used
  - Calorimeter BE → Calorimeter Trigger → Correlator
    - AP Consortium boards have same link technologies so Calorimeter trigger cards can temporarily serve as substitutes for Calorimeter BE to decouple schedules.
    - Correlator is identical board to Calorimeter Trigger.
  - Test provides input for Trigger TDR

- **System integration test Mid-CY22**
  - Production Pilot Boards used
  - Calorimeter BE → Calorimeter Trigger → Correlator
  - Final Test before production starts
  - Final Major System test before shipment to CERN.