

# **CMS EMU TRIGGER ELECTRONICS**

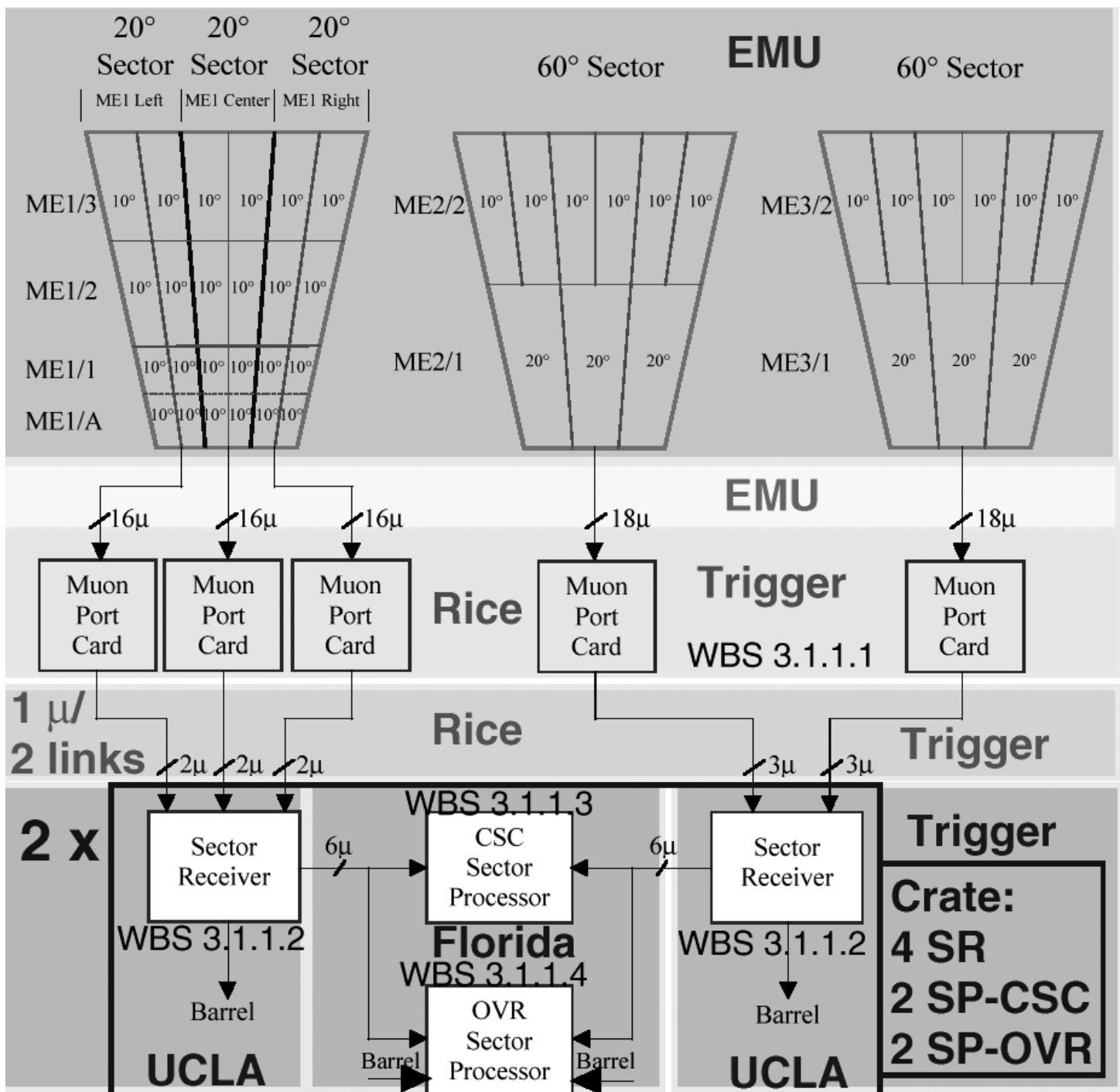


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**Rice University**

**February 1999**

# Trigger Layout and Responsibilities



# Basic Requirements



- Latency:  $< 3.2 \text{ us}$
- Fully pipelined synchronous architecture, dead time = 0
- Maximum output rate:  $< 15 \text{ kHz}$
- Output to the Global Trigger: up to 4 highest Pt muons in each event

# Initial Design



- Put all front end, LCT generation and processing electronics on chambers
- Issues:
  - Poor accessibility
  - Power dissipation
  - Radiation hardness

# **New Design**

## **(Summer '98 UCLA)**



- Simple front end boards on chambers
- All digital LCT generation and processing logic into 9U crates on periphery

# **MUON TRIGGER SYSTEM MODULE COUNT (UCLA, OSU, RICE, UF)**

✓ Anode LCT Module	- 504
✓ Cathode LCT Module	- 504
✓ Trigger Motherboard	- 264
✓ DAQ Motherboard	- 264
✓ Port Card	- 60
✓ Clock and Control Board	- 126
✓ Sector Receiver	- 24
✓ Sector Processor	- 24
✓ Sorter	- 1
✓	<b>Total - 1771</b>

# **EMU Trigger Motherboard**

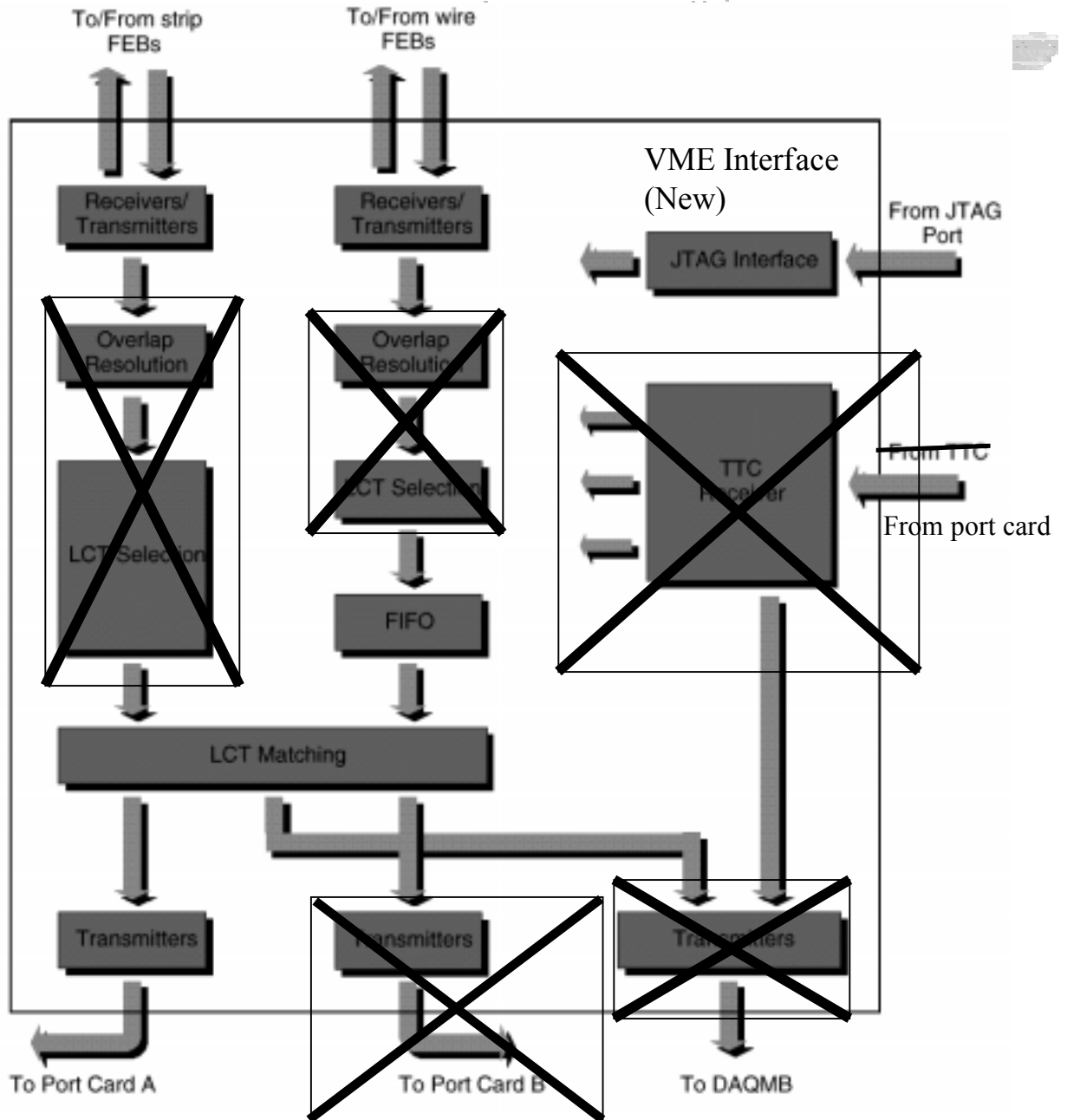


- One board for two chambers
  - Receives up to two anode and two cathode LCT's
  - Matches them in time
  - Passes them on to Port Card
  - 9U VME board with interface
- 
- We have proposal to allow the use of RPC information to resolve ghosts if needed

# MB

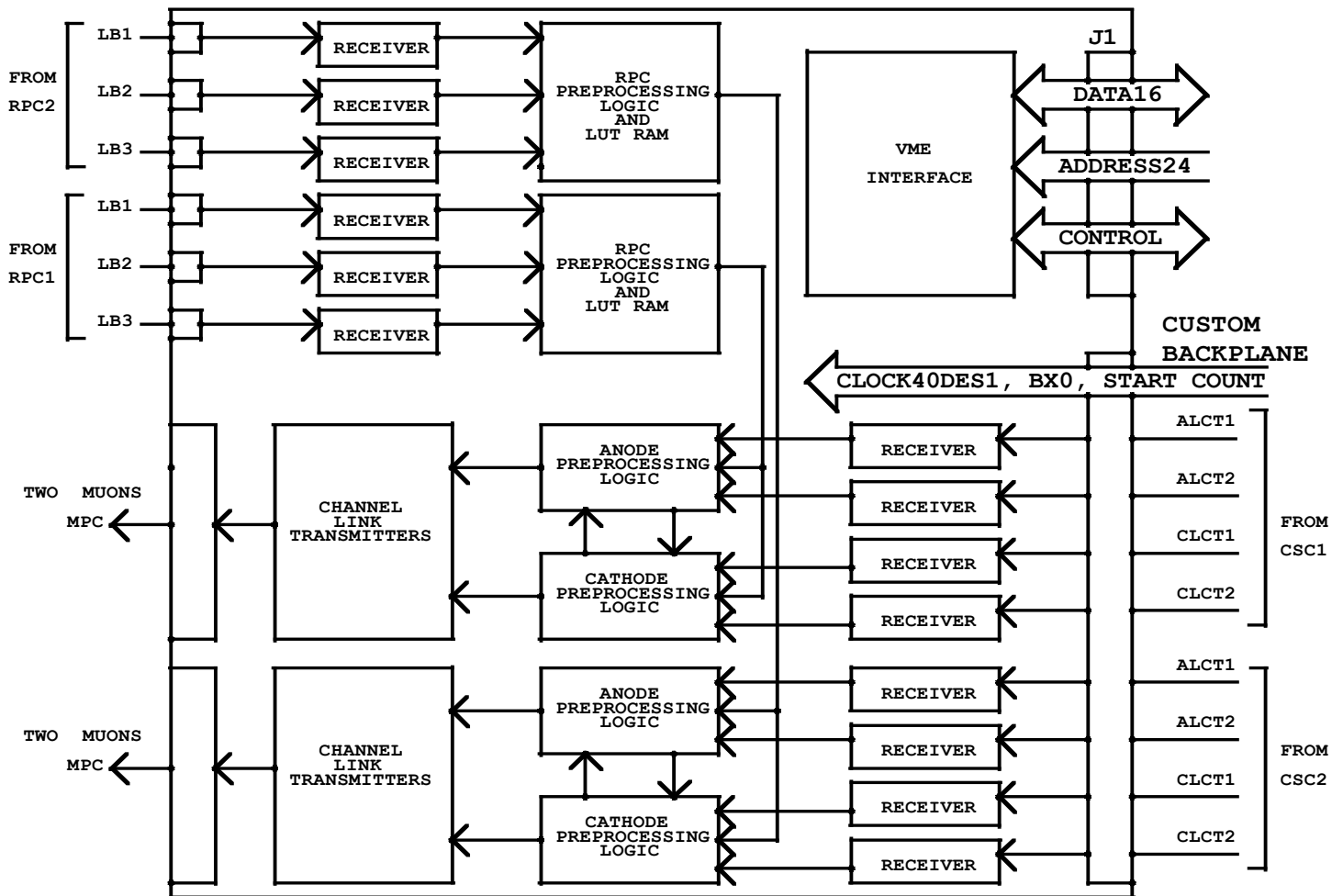
## Schematic

(and changes)



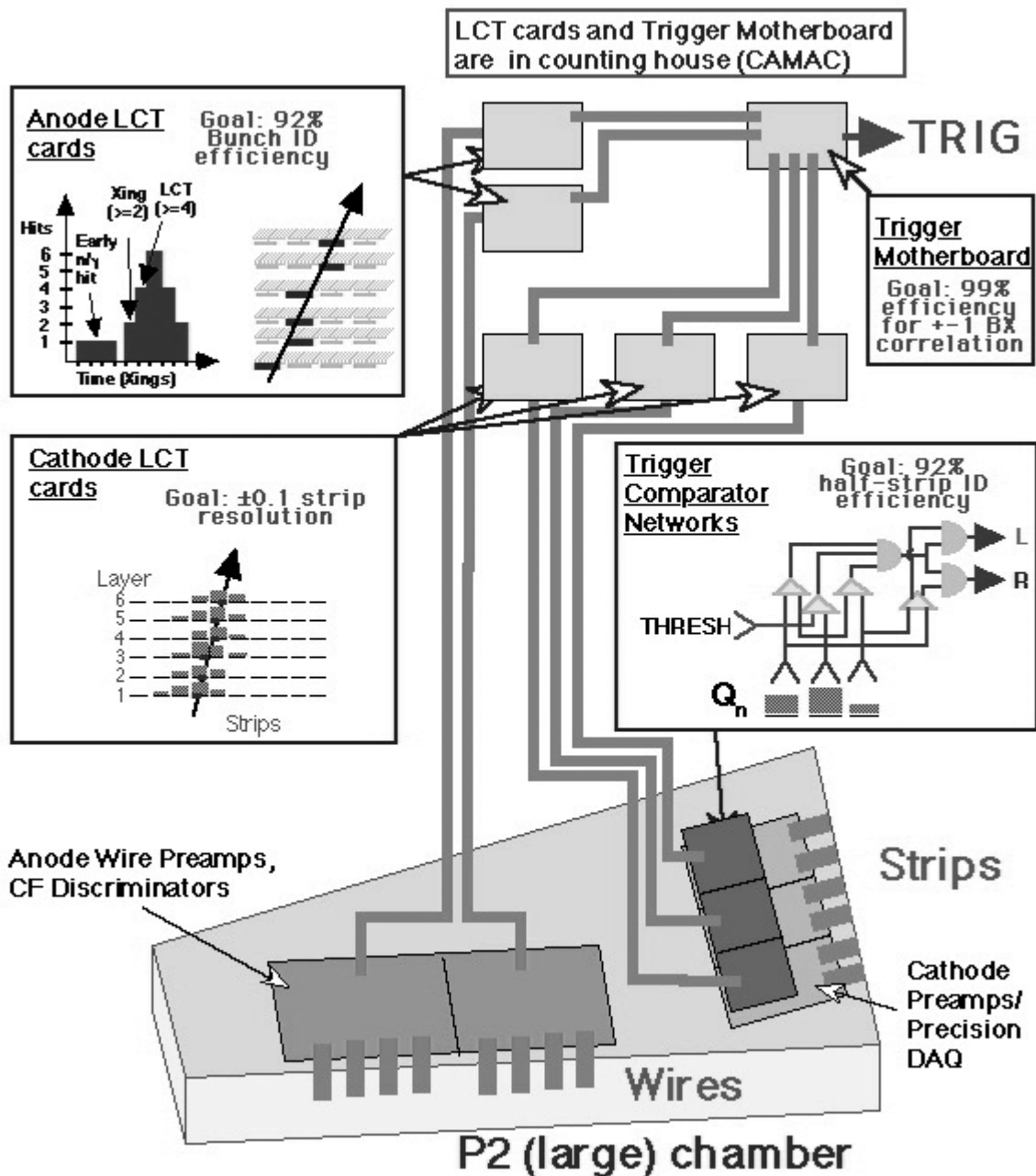


# TRIGGER MOTHERBOARD




MUON TRIGGER MOTHERBOARD BLOCK DIAGRAM

# Summer 98 Test Beam Prototypes



# **Engineering "proofs-of-principle"**



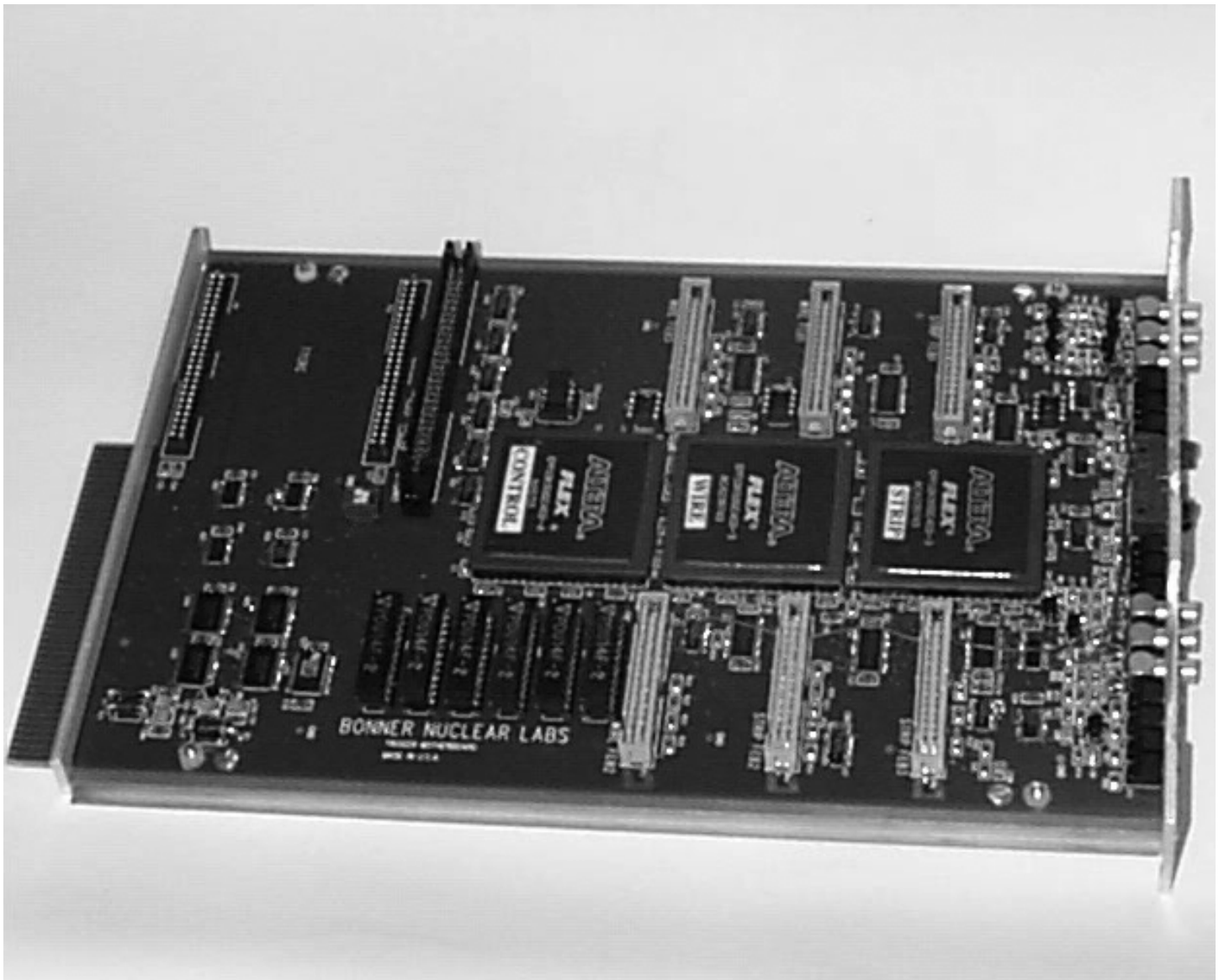
- **Custom analog ASICs (preamps, disc's, comparators)**
- **Wide use of FPGAs at 40 MHz**
- **High-speed LVDS channel links**
- **Clock distribution from motherboard**
- **Trigger drives DAQ system readout**

# Motherboard Prototype



- CAMAC board
- Communicate with FE via LVDS
- Send Clock to FE from quartz or external generator
- Selected LCT's stored in FIFO for reading by CAMAC
- Board is tested and working at 40 MHz.

**It was built,  
and worked!**

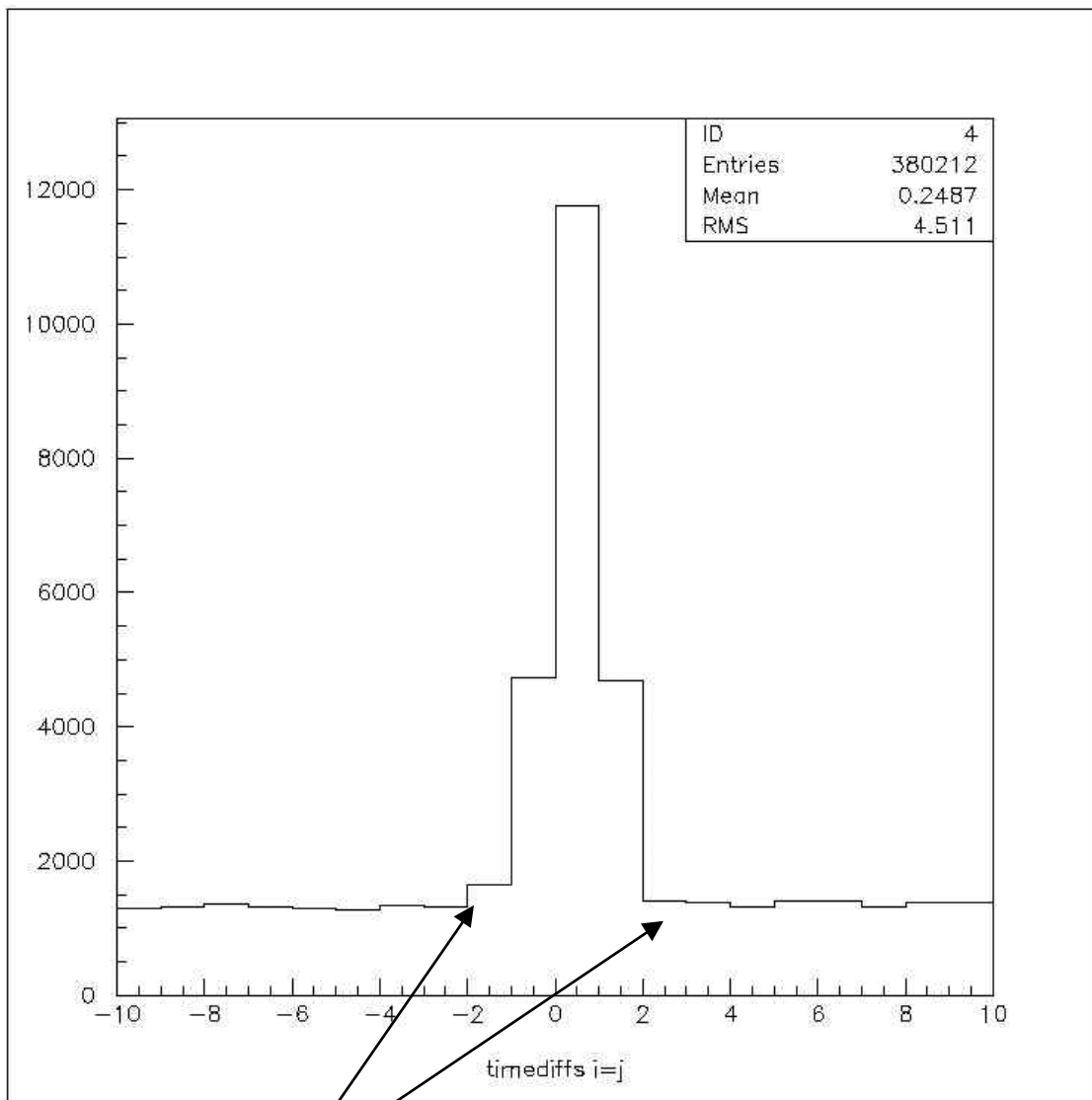


# By that I mean



- Communicated with LCT card via National channel link LVDS
- Distributed clock
- Correctly selected “best” LCT’s
- We could study BXN matching
  - but we could not test the BXN PLD code
    - Its tough testing this in an asynchronous beam.

# BXN Matching Study



GIF  
Turned  
OFF

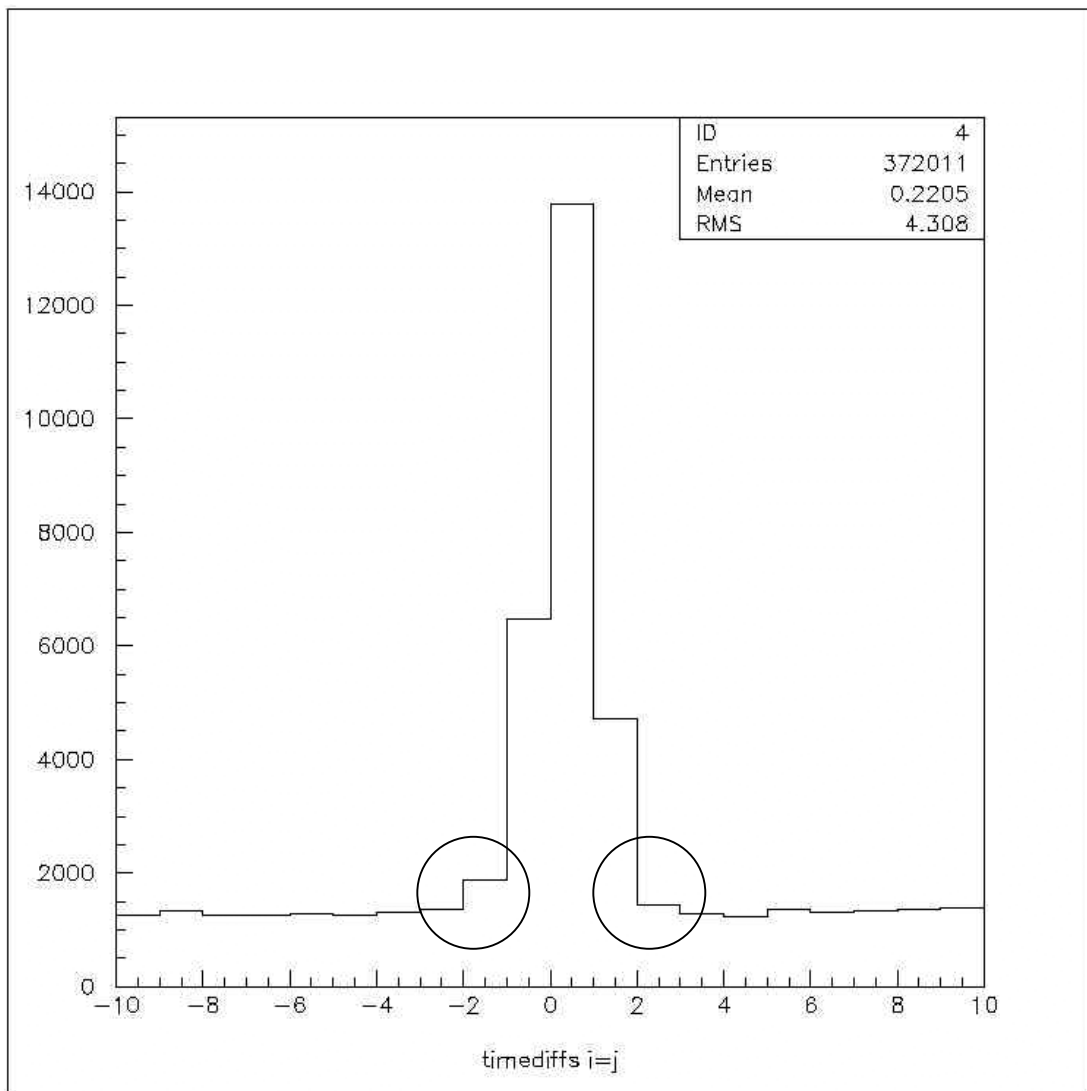
Excess

$|\text{BXN mismatch}| > 1$

2% of the time

# BXN Matching Study

GIF  
Turned  
On



In this case 3.2% excess



# Caveat Emptor



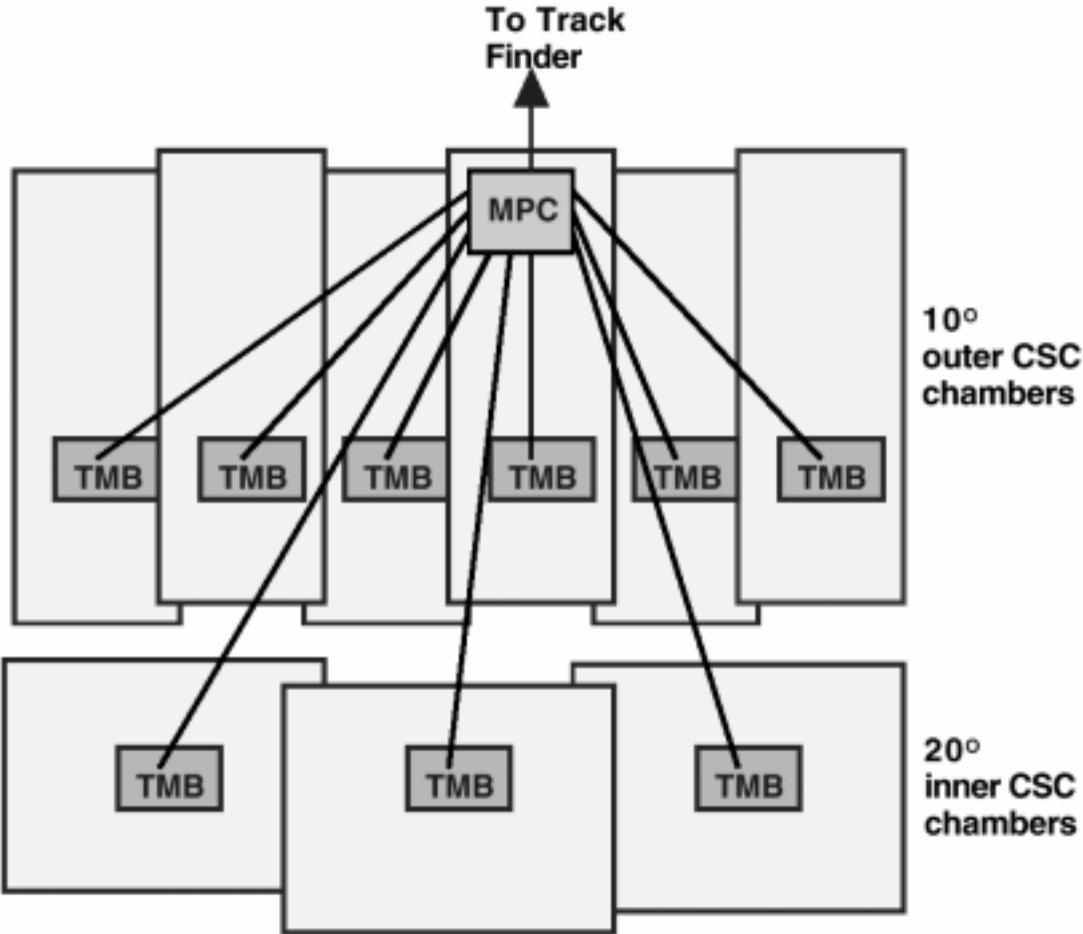
- It must be noted that those BXN matching results are using the worst possible timing you could get from the Anodes
- There is no way in this test data to correct the BXN from the anode as will be done in reality.
- Thus the results represent upper limits.

# **Trigger Motherboard New Prototype Design Status**



- Inputs from LCT modules and outputs to Port Card are specified
- PLD design 60% completed
- Schematic design in progress

# The Port Card

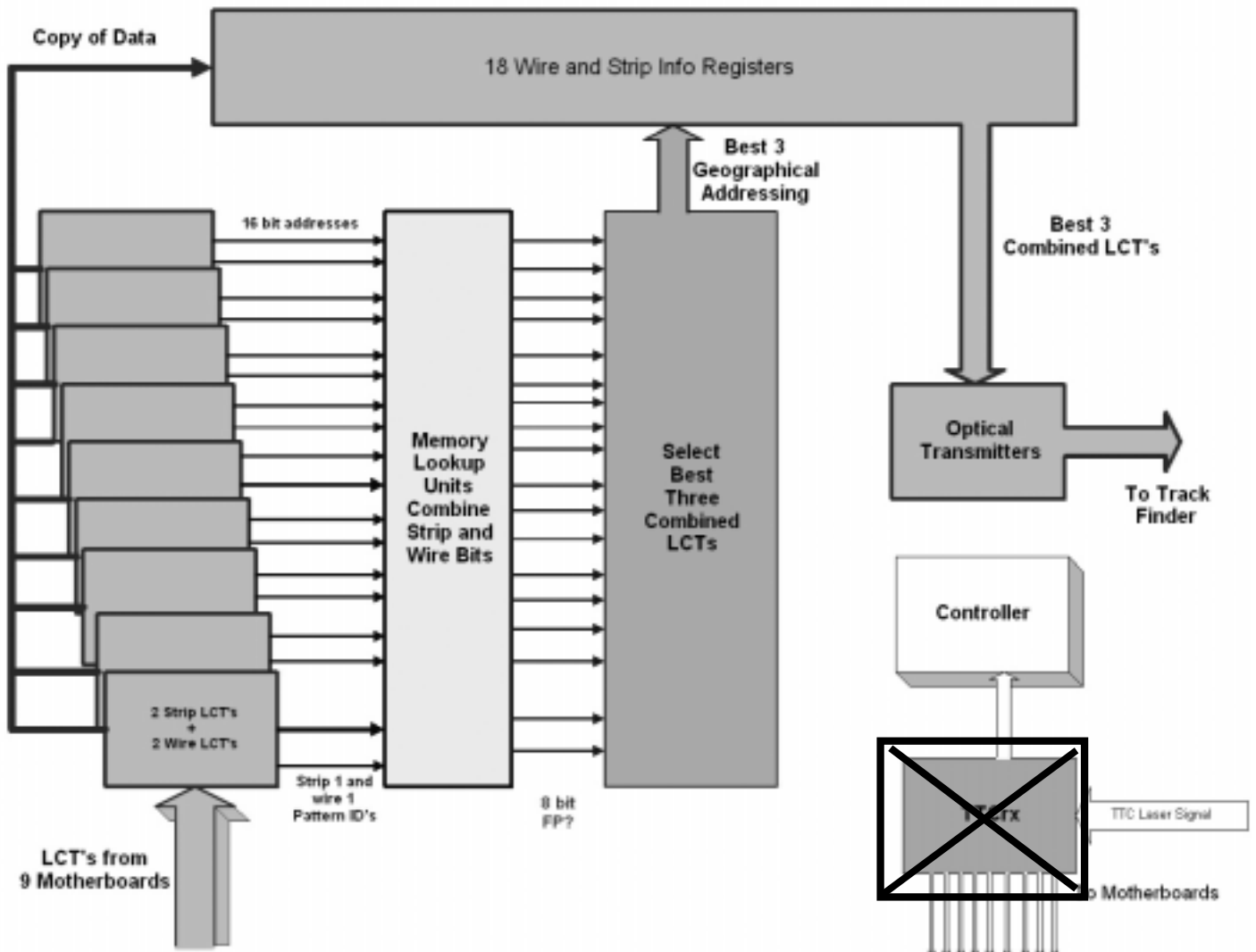


# The Port Card

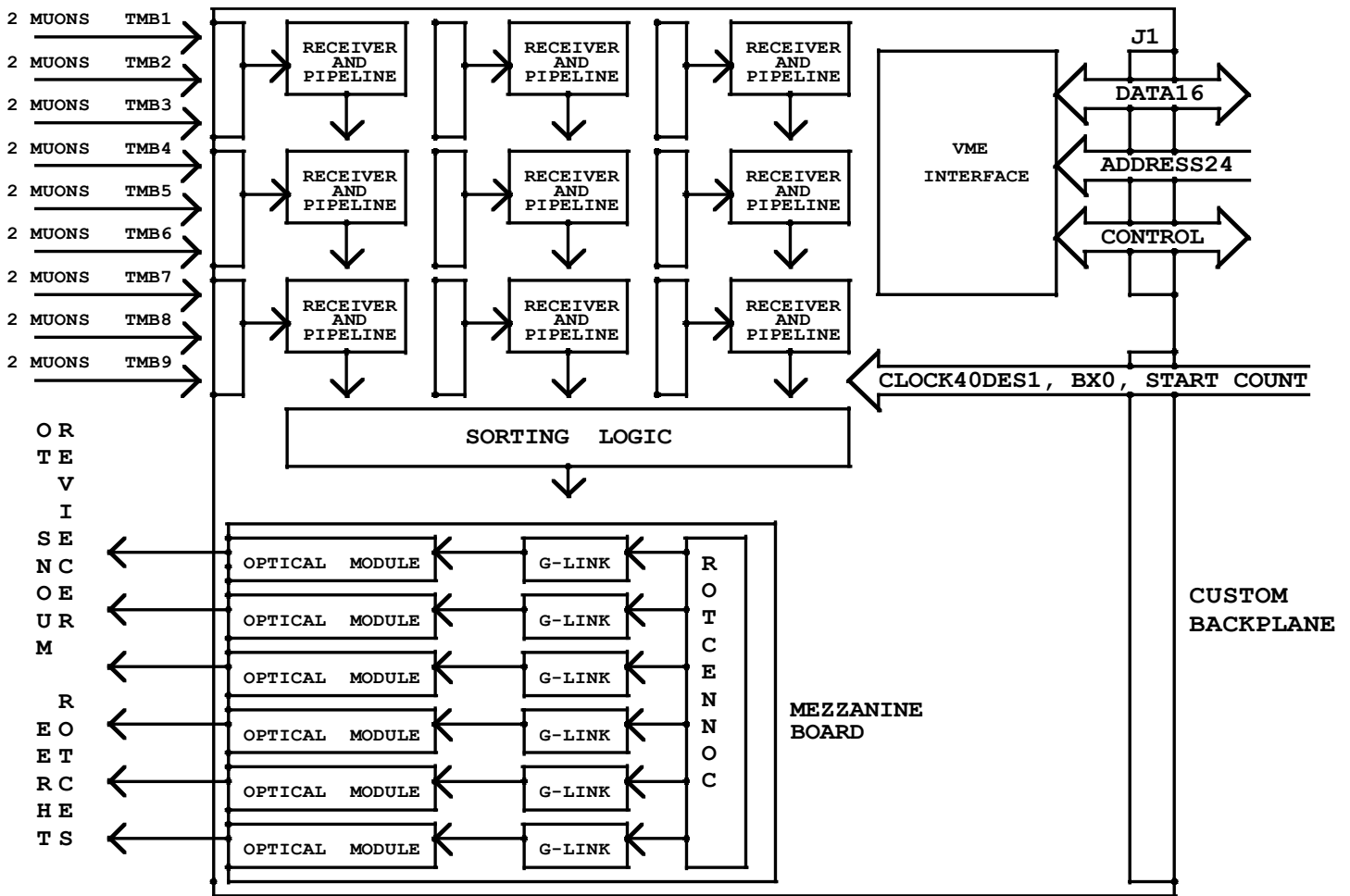


- Serves one sector of 8 or 9 chambers
- Receives up to 18 LCT's from motherboards
- Selects the best 3 and sends to sector receivers on optical cable
- VME 9U board

# Port Card



# MUON PORT CARD



MUON PORT CARD BLOCK DIAGRAM

# **PORT CARD DESIGN STATUS**



- Inputs from Trigger Motherboard and outputs to Sector Receiver are specified
- Chipset and Optical Modules for communication with Sector Receiver are defined
- Sorting Logic designed and under optimization now
- Schematic design will start soon

# Hardwired Limitations



- Note restrictions of the scheme
- 1 stub per FE card
- 2 stubs per chamber
- 3 stubs per 20 or 60 degree sector

In station 1 use 20 degree sectors to limit number of Mboards to 9

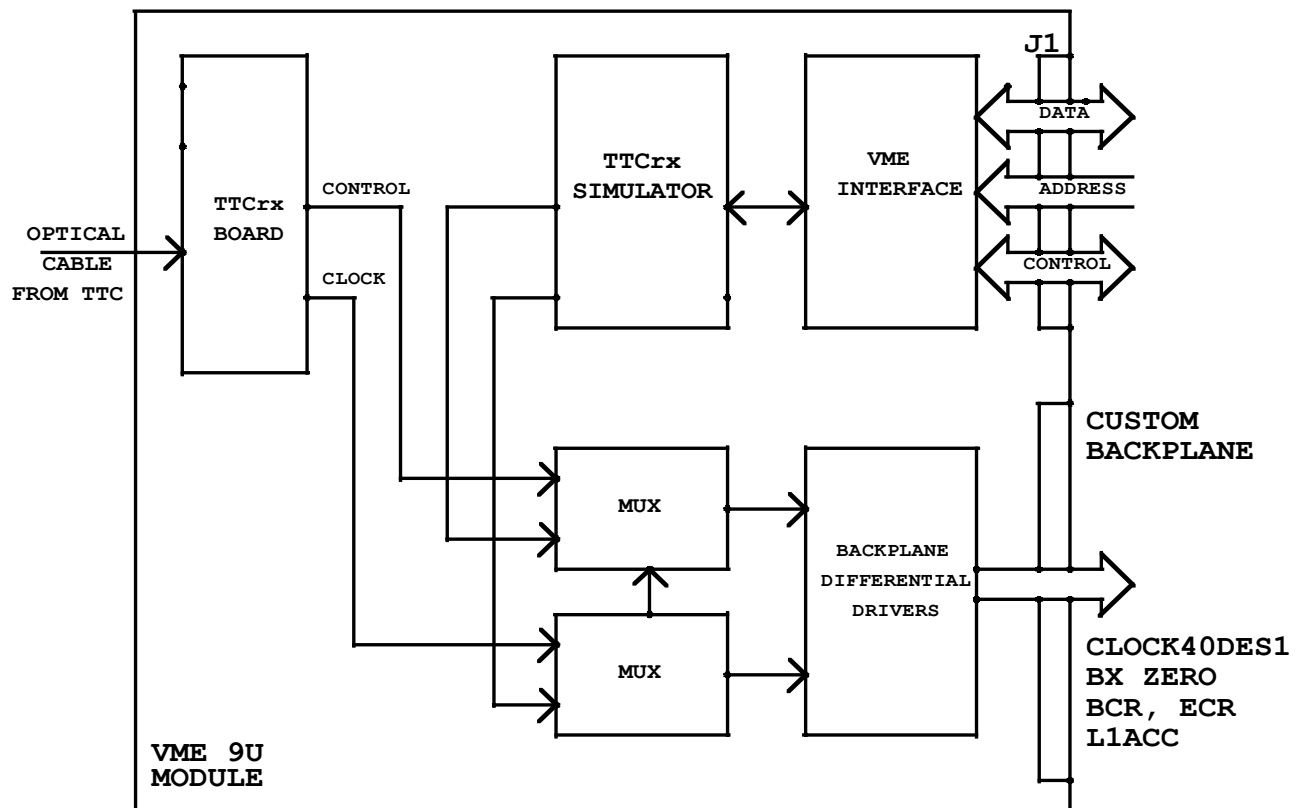
This used to be 30 degrees

Consequence of descope, must use 60 degree sectors in stations > 1



# CLOCK AND CONTROL BOARD

- DISTRIBUTES TTC SIGNALS TO ALL TRIGGER 9U VME MODULES
- UNIFIED DESIGN FOR TRIGGER AND SECTOR PROCESSOR CRATES
- ABLE TO GENERATE TTC SIGNALS FROM BUILD-IN SIMULATOR
- VME 9U MODULE



MUON CLOCK AND CONTROL BOARD

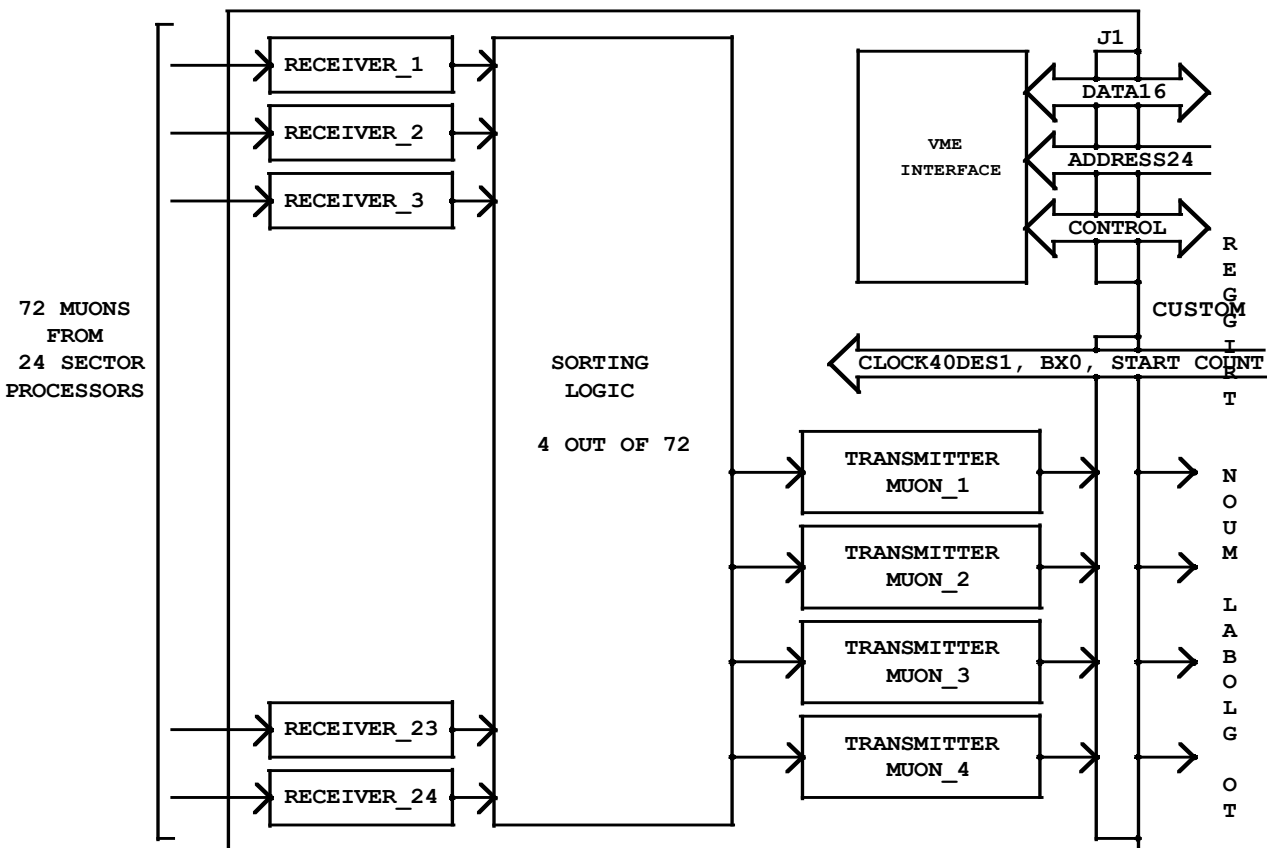
# **Clock and Control Board Design Status**



- Number and list of signals which should be distributed from TTC to trigger modules will be finalized soon
- Initial proposal on custom backplane is ready
- Schematic design will start soon

# MUON SORTER

- RECEIVES 72 MUONS FROM 24 SECTOR PROCESSORS (3 MUONS PER SECTOR PROCESSOR)
- SELECTS FOUR BEST MUONS AND SENDS THEM TO GLOBAL MUON TRIGGER
- VME 9U MODULE



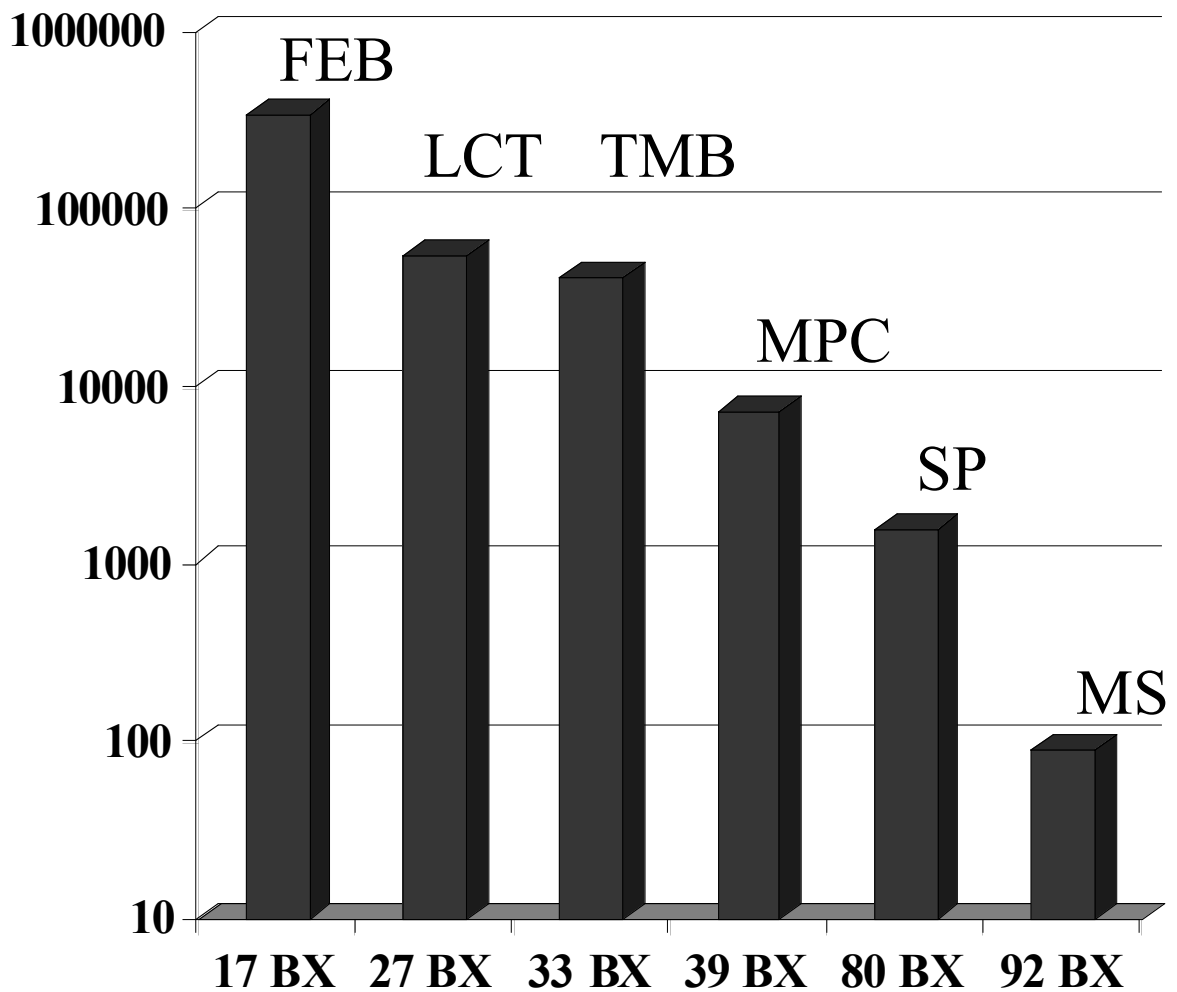
MUON SORTER BLOCK DIAGRAM

# **MUON SORTER DESIGN STATUS**



- **General requirements (inputs from Sector Processors and outputs to Global Trigger) are specified**
- **Basic sorting unit (4 best patterns out of 8) initial design is completed**
- **Optimization and timing analysis in progress**
- **Initial specification will be prepared this year**

# EMU TRIGGER BITS REDUCTION FACTOR vs TRIGGER LATENCY



1 BX = 25 ns