CMS Upgrade MB Response to SLHC Document:

10.01: Development of Radiation Hard Pixel Detectors for the CMS Tracker Upgrade for the SLHC

(Contact Person: Simon Kwan, Fermilab)

It is our intent to recommend this proposal for approval with some requested revisions, which could be provided in an addendum. These revisions and plans for reviews, *etc*. should be made with agreement of Tracking Project Management. Please see the comments from the referees.

Specific requests for the revised proposal or addendum are:

1. Provide more information on the *prioritization* of the effort on the various types of sensors and technologies as well as the process of narrowing down and selecting a particular sensor (e.g. polycrystalline diamond, single crystal diamond, SoD) and technology (e.g. readout chip ASIC process, feature size, etc.) .

2. Provide more details on collaboration with or incorporation of information from other diamond R&D work such as RD42, ATLAS R&D, the CMS BRM group, other CMS R&D efforts and also other groups that have designed pixel readout chips and infrastructure.

3. Provide a plan for project reviews at appropriate points in the schedule when major design, sensor and technology choices will be made, before starting the design of the prototype FE chip and at regular intervals to track general progress. For the development of the sensors, example milestones with reviews would be delivery of wafers/substrates, characterization of wafers/substrates, metallization of sensors and bump bonding of modules.

4. Provide more details with comparisons to previous pixel detector projects, as to how the various components of this program can be completed in the times estimated.

5. Provide more details on the diamond radiation hardness expected and needed within the CMS environment, including the particle energy spectrum.

6. Explain how the integration of the various technologies will be done, e.g. diamond pixels and 3D pixels with very different input capacitances.

7. Provide more details on the SOD and SOI R&D and the relative emphasis vs. other parts of the proposal.

8. Provide more details on the integration of this R&D program with the overall CMS planning for the inner pixel detector.

In addition, we request you to address the detailed comments on the proposal from the referees below.

Referee #1:

The proposal addresses important subjects with many unsolved problems for a future tracker upgrade. It deals with new sensor technologies which are supposed to withstand much higher integrated doses than the present technology. Also the readout of the enormous data rates at higher peak luminosities with low data losses and the low signal amplitudes of the proposed sensor technologies need considerable R&D. Let me first answer your specific questions:

1 Is the R&D appropriate for the needs of CMS at SLHC (ie focused)? -Yes. I think most of the topics need to be addressed. Diamond and 3D Si must be considered as alternatives to planar Si for the future and it still needs substantial R&D to make the technology mature and fit the needs of CMS. No doubt, a new architecture for a readout chip is needed at very high luminosities, likely with smaller pixel size and in a technology with smaller feature size.

2 Is the R&D not excessively duplicated ? -There will be some duplication. Within the EU FP7 program, PSI has been granted a 2 years position which we are just about to fill. The goal is to work on a new chip architecture and design analog front ends. At this early stage I would not asses this duplication as problematic. The past has shown us that new architectures can only be properly evaluated after it has been worked out in quite some detail. This can naturally been parallelized through different teams. However at some point CMS should choose the (hopefully) best solution. Here I see more of a problem. To me the proposal goes way too far for the proposed timescale. As I will explain below I don't think this is realistic. It will take considerably more time and in the mean time other projects should not be rejected with the argument of duplication.

Since I am not an expert in the field of sensor development I will mainly concentrate on the readout part.

According to the schedule (table 6), it is planed to have the first full scale prototype readout chip in hand 2.25 years after project start. This timescale seems to me far too aggressive. In order to support this, table 1 summarizes milestones of selected pixel chip projects of similar or lower complexity. The most relevant project is the ATLAS chip, which has to fullfill more or less the same specifications. They will have their first prototype chip (with non-final interface) in hand 3.5 years after project start. Several labs and designers with excellent qualifications are involved.

It is obvious that one cannot draw solid conclusions for future projects from this table. But a few points are worth to be mentioned:

1 So far there was no new development of a pixel chip of comparable complexity with a full prototype ready in less than 3.5 years.

2 Even upgrade projects in the sense of change in technology (which is always accompanied by functional improvements) had no prototype ready in less than 1.5-2 years

3 In all cases it took more than 2 years after the first prototype to have the production version ready.

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Table 1: Time scales of other pixel chip design projects with comparable or lower complexity. The first 3 projects are new developments, while the lower 3 are migrations (and improvements) of an existing architecture to a new technology.

Project	Project start	First full scale chip submission	final submission	Number of labs/designers
ATLAS B-layer CMS DMILL Eiger[2] 250nm	end 2006 1996 1/2005	4/2010[1] 12/2001 2/2009	not yet stopped not yet	5 / > 10 1 / < 10 1 / 1.5
BTeV FPIX 250 nm CMS pixel 250 nm Pilatus[2] 250 nm	1/1999 2/2002 11/2002	10/2002 9/2003 9/2004	5/2005 (not final) 11/2005 3/2007	1 / O(10) 1 / 6 1 / 3

[1]Complete core, but non-final interface. [2]Photon counting chip for synchrotron applications developed at PSI

1 There is no indication that parallelization (more labs and designers involved) can drastically reduce the development time. This should not be too surprising. Interfaces between different functional blocks are not so clearly defined as in a typical commercial logic chip. This gives rise to organizational overhead which grows far more than linearly with the number of people involved.

2 Having a chip is not the same as having a module operating under realistic circumstances. Module development cannot proceed completely in parallel. Many problems only show up with the final chip in hand.

Although there are 9 institutes and > 40 people on the proposal, most of the work is done by the FNAL group. The chip design group at FNAL certainly has a lot of experience in the field and a high reputation. Nonetheless, it needs explanation why they think they can develop such a complex ASIC in so much less time than in any previous project. I would recommend to ask for a more realistic R&D plan, especially in the readout part. The large coverage of this proposal might impede other useful R&D projects, while the chance of success within the proposed time .

Referee #2:

The document is well written, by a collaboration of labs and researchers with relevant experience in the field. The proposal to look globally at sensor plus readout chip is attractive, even though the different types of sensors mentioned (diamond, 3D, Si, SoD, etc.) and the many technologies mentioned (3 types of CMOS, 3D) make the project very challenging, running the risk of effort dispersion if not well coordinated. The timescales for both sensor and readout workpackages are very tight, but this is probably not a show stopping issue given the current development schedule uncertainty.

Sensor Work package:

The proposal focuses on Diamond sensors. How do the authors intend to build on and significantly surpass previous Diamond R&D work (RD42 in particular)? How do they intend to collaborate with the ongoing ATLAS project? The difficulty to find industrial grade producers of detector-quality material is mentioned, but only small size prototypes are described in the proposal details.

Given the size of the CMS pixel tracker and the already long and difficult history of diamond detector R&D, it seems essential that the long term objective to build a full detector is not forgotten. The authors must pay close attention to the breakthroughs that will be required to succeed. If the historical, collaborative and industrial issues are not recognized and carefully addressed, this proposal will be limitted to qualifying concepts which cannot scale up to full detectors, and will thus be a waste of effort from the CMS point of view.

Given this challenge at hand, it might be advisable to concentrate on only a subset of sensor technologies to maximize the likelyhood of success. Also, Table 3 highlights an obvious need for tighter coordination

and collaboration, as only two out of eight institutes sign up for coordination with the other WGs and R&D projects.

Readout work package:

The proposal to make an optimal front-end choice after comparing different sensor scenarios is logical, but the number of ASIC processes considered is overwhelming: 130nm, 90nm, 60nm, 3D. Given the very different maturity levels and costs of these technologies, how do the authors propose to select in an informed way the most appropriate one? Is experience available in each one of them? How is a carefull technology selection process compatible with the design of test blocks starting in the second half of 2010 already? Is money available to test many technologies in parallel? If not, the authors should clarify at the proposal level which technology choices have been made.

To design a pixel front-end chip is a difficult and long process. How do the authors intend to collaborate with the teams that have designed similar chips in the past (in CMS and other detectors)? How do they intend to coordinate their designs with other groups involved in the readout chain at the system level (powering, links, backend)?

The schedule in table 6 indicates that the design of a proto chip could start in the second half of 2011 and will last one year only, while the design of the test blocks will be completed as late as end of 2011. This is very agressive and does not match previously observed timescales. It also seems premature to rush designing a chip while not all test structures and technologies have been evaluated.

A safer plan might be to introduce a project breakpoint before starting the design of a prototype chip, to evaluate the different scenarios envisaged without pressure and only then take a decision on the best path forward.

Conclusion:

This R&D is appropriate for CMS in a context of relaxed upgrade timescales. However, given the risks associated with both sensor and readout work packages, and given the uncertainty of the upgrade schedule, it might be advisable to thoroughly review the project progress in 2012, before the design of a prototype FE chip is launched.

Referee #3:

Common Comments:

The topic is very broad and we all feel the need to develop radiation hard pixel sensors. The R&D proposal is focused mainly on diamond pixels but also wants to exploit ALL other new sensor technologies, e.g. planar and 3D sensors. This needs strong planning and interaction with other groups to ensure the development of all sensors with the correct new chip footprint.

The development of a full electronics pixel chip on the other hand is a more common development. The development of a next generation of a pixel chip with the current architecture is ongoing at the PSI and a plan to development a new architecture is certainly under discussion in the Collaboration. It should be avoided that two groups independently develop two chips, when there is a future need of only one. I'm talking about full developments and submissions not touching the need of brainstorming of ideas of architectures and simulation.

Requirements:

The proposal clearly states the need to know the required pixel size. Is the group going to answer that questions with physics simulations or is the plan to point out and simulate the resulting requirements for the system given a defined pixel size? In the proposal both aspects are mentioned but it was not clear if both will be in the scope of the proposal.

Both items are very common topics and need attention.

Comments and questions to the sensor part:

Throughout the R&D proposal, the radiation hardness of diamond is not questioned. While for silicon always 1MeVn_eq (NIEL) values are quoted, the diamond fluencies are quoted in number of protons, I assume 24GeV protons. What about the following results, which hint to a much reduced radiation hardness to low energetic charged particles and neutrons.

- W. de Boer et al. Phys.Status Solidi 204:3009, 2007
- http://indico.cern.ch/conferenceDisplay.py?confId=69661 page 12
- http://indico.cern.ch/getFile.py/access?contribId=13&sessionId=3&resId=0&materialId=slides&confId=67411 page 4

Has that been taken into account, are studies with this respect planned? Is a simulation of the charged particle energy spectrum in the inner pixel radius planned – taking loopers into account?
How is the "Study of various sensor technologies" planned? Is it in the scope of the R&D group to design and procure also these sensors? This would definitively be redundant. Otherwise, how is the coordination with the sensor WG and other R&D groups planned?
With the current interpolation single crystal diamonds will not be available in the sizes needed for inner pixels detectors. Why is this topic followed?

The proposal states to work with R&D proposals 08-03, 08-01 and 07-13. How is this planned? These proposals contain some of the mentioned new sensor concepts (planar, 3D) but none will come matching any new chip. Is there an intention to characterize some of the sensors or compare results from these R&D groups?

The topic SoD is mentioned, how is this planned, should the same chip be developed in a bump bonding package and also in a SoD monolithic form? Will you actively participate in SoD development or will this be a more a side observational topic.

Although I have personal doubts about diamond as inner pixel detectors, this option should not be forgotten and I support a focused R&D. The low current, low noise, high thermal conductivity is clearly a plus and especially the possibility to operate them at room temperature. Early feasibility studies can be quite separated from other efforts, as long as all information from other collaborations, e.g. RD42, is taken into account and regular reporting is granted, e.g. in the Upgrade Sensor WG.

Comments and questions to the electronics part:

How do you intend to coordinate with other ongoing chip developments, e.g. at PSI and CERN?

How do you plan to handle the very much different input capacitances of diamond pixels and 3D pixels in a single chip? Or do you plan to have several chips with adapted analog circuits?

How do you intend to decide on the chip feature size?

Is it wise to mix the question of 3D chip integration with the question of a diamond pixel detector?

Concluding subjective comments:

The R&D proposal is nicely planned and the group is obviously well equipped and experienced but the scope is enormous it encompasses almost all ingredients to design and build an inner pixel detector: all sensor types plus chips. How it is intended to integrate these common items in the overall planning of the Collaboration?

The proposal contains two very separate efforts: development of diamond sensor and a multi-purpose electronic pixel chip.

- Polycrystalline diamond sensor development should be followed
    - Single crystal probably not
    - SoD probably not, at least not in the same effort
- The development and production of a chip is an extremely demanding task in terms of human and financial resources, and should not be planned as a standalone activity, but evaluated in the context of the already commonly planned ASICs development. It is a more common effort with many common constraints.

The RD is appropriate for the needs of CMS at SLHC (ie focussed)

The RD is not excessively duplicated (ie we don't have too many people have working on the same topics)

This would be the only study on diamond sensor, although I'm personally not very enthusiastic about diamond sensor for an inner pixel volume, the topic should not neglected and has its value.
The development of full grown chip is another topic and here, I believe, a more common effort than an R&D proposal would be more adequate, of course exploiting the full expertise of this group.

The evaluation of all other sensor types is of course redundant and the plan how to do this should be much better specified. Does it mean that other WG groups can freely use the new chip or that other sensors should be delivered to the R&D proposal group? In the second case, the proposal may replace the Upgrade Sensor WG.

Referee #4:

In the following I restrict my review of the Proposal to the sensor part of the proposal, as I am not an expert in readout electronics.

1 General remark

It is not obvious to me why the development of a ROC and the construction of diamond modules need to be combined to the same R&D proposal.

2 Development of diamond sensors

I have the impression that there is some lack of activity within CMS concerning diamond sensors and therefore strongly support any effort in this field. It does not lead to a duplication of efforts, especially as most institution are member of RD42 and are working in this field anyway. Diamond has attractive characteristics, especially the absence of leakage current, which allows for an operation above the dew point of the cavern, even after very high fluences of radiation. Therefore I consider them as an interesting option in addition to planar and 3D-silicon detectors. In this sense the proposal focused on CMS-needs for SLHC (inner pixel layer only, $L > 2´10^{13} cm^{-2} s^{-1}$)

The main problems with diamond detectors are:

- Availability of (high quality) substrates
- Low signal (charge collection distance)

In both points there seems substantial progress in the recent time justifying or even nesseciating a relaunch of the R&D efforts. Especially the emergence of a possible new vendor in the US for DVD-diamond gives hope for a reduction of prices in future.

In this view the evaluation of vendors and the characterization of the ground material which is addressed in activity 2 (page 17/18) seems to me the key point of the proposal. However this point is not well represented in the schedule given in tab. 5.

I would propose some more milestones and ask for a (realistic) time estimation:

a) Delivery of wafers/substrates b) Characterization of substrates c) Metalization of sensors d) Bump bonding of (bare) modules (single chip or larger)

It might be that c) and d) could be done by the same company (e.g. IZM). The rest (source/laster tests, irradiation, testbeam, analysis) is more or less standard and takes in my experience about 2 years.

3 Interconnection techniques

One page 16 there is a short statement that SOI and SOD will also be evaluated. In my opinion this is an R&D project on its own which requires a lot of (financial) resources. I suspect that those technologies might not be available within a mid-term future.