CMS Level-1 Trigger Review

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CMS Comprehensive Review
September 27, 2004

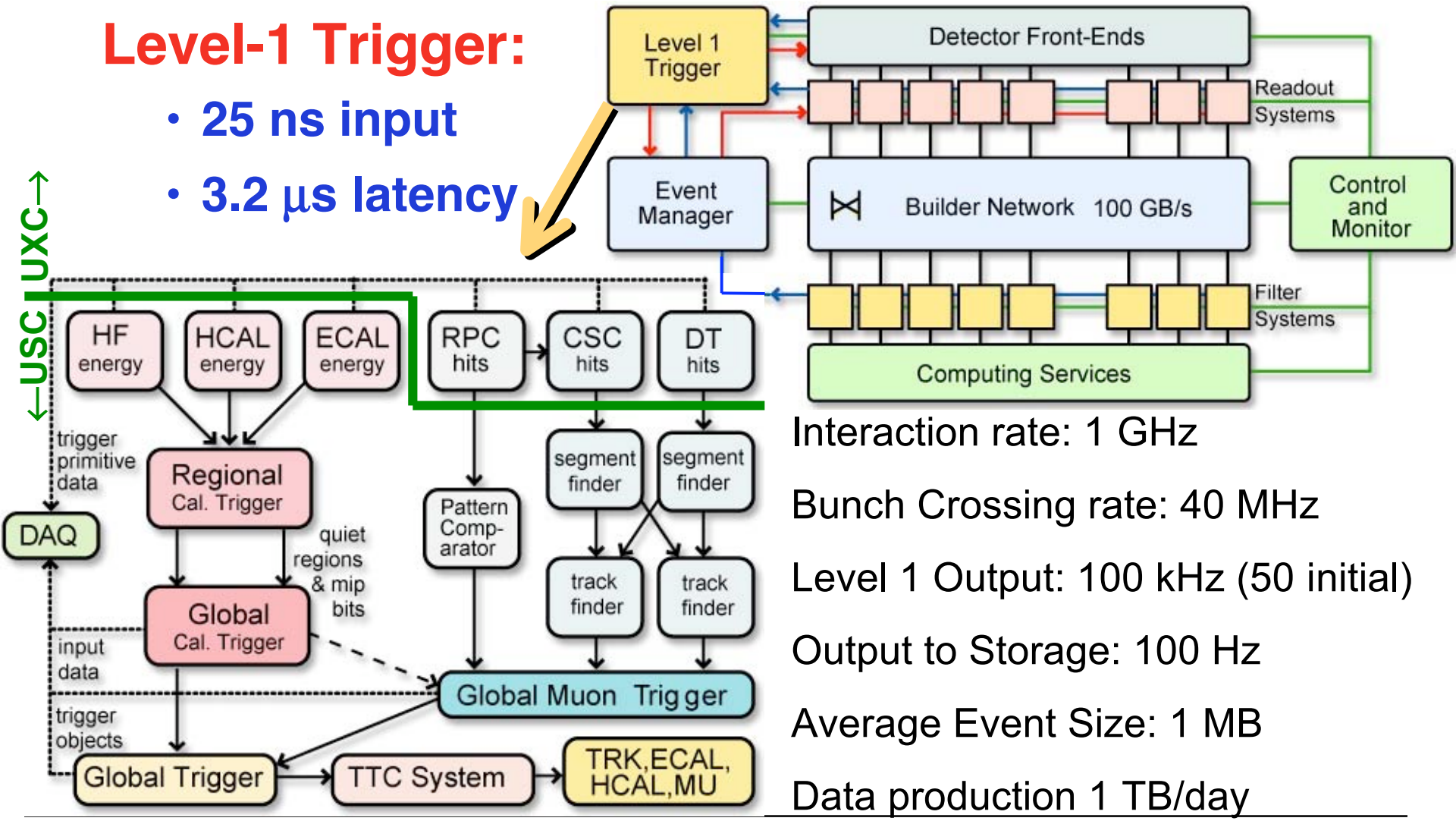
The pdf file of this talk is available at:
http://cmsdoc.cern.ch/cms/TRIDAS/tr/0409/smith_CR_sep04.pdf
See also CMS Level 1 Trigger Home page at
http://cmsdoc.cern.ch/cms/TRIDAS/html/level1.html

CMS Level-1 Trigger & DAQ

Overall Trigger & DAQ Architecture: 2 Levels:

Level-1 Trigger:

- 25 ns input
- 3.2 μs latency



Interaction rate: 1 GHz

Bunch Crossing rate: 40 MHz

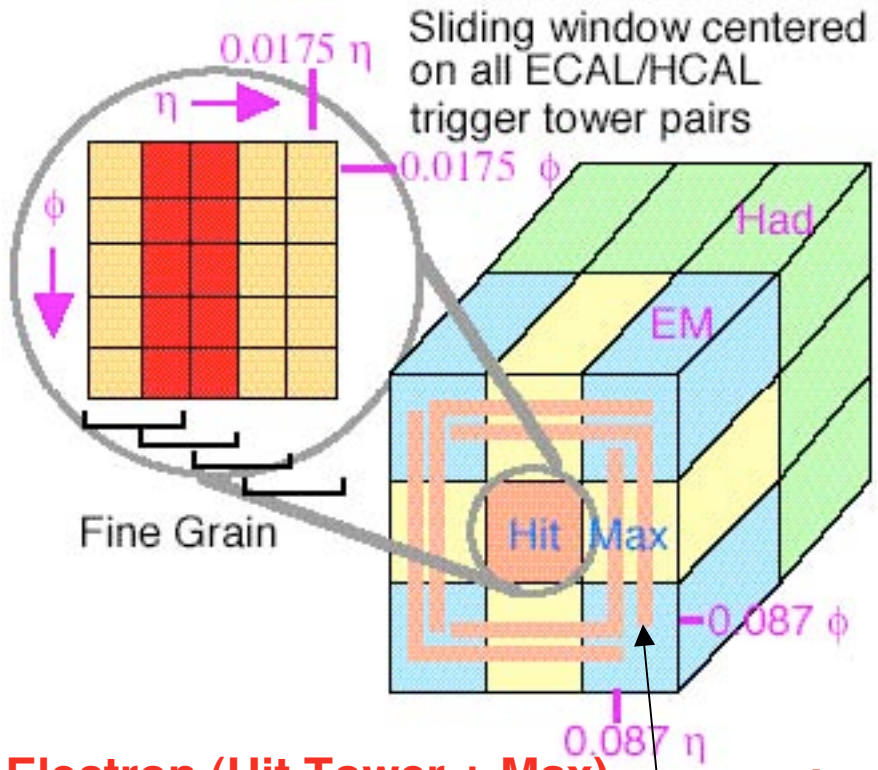
Level 1 Output: 100 kHz (50 initial)

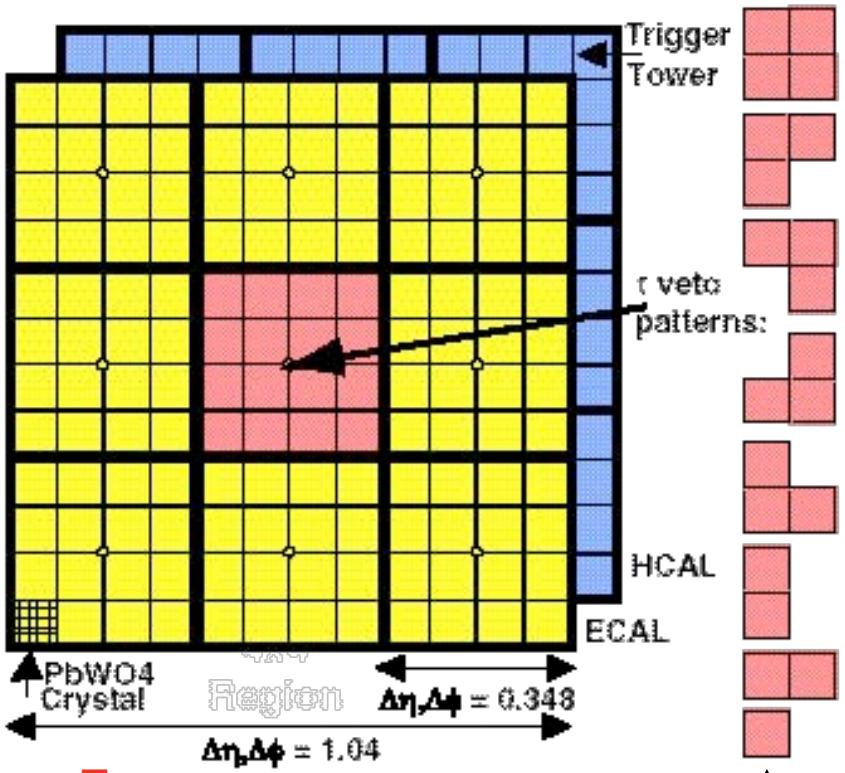
Output to Storage: 100 Hz

Average Event Size: 1 MB

Data production 1 TB/day

Calorimeter Trig. Algorithms





Electron (Hit Tower + Max)

- 2-tower ΣE_T + Hit tower H/E
- Hit tower 2x5-crystal strips >90% E_T in 5x5 (Fine Grain)

Isolated Electron (3x3 Tower)

- Quiet neighbors: all towers pass Fine Grain & H/E
- One group of 5 EM E_T < Thr.

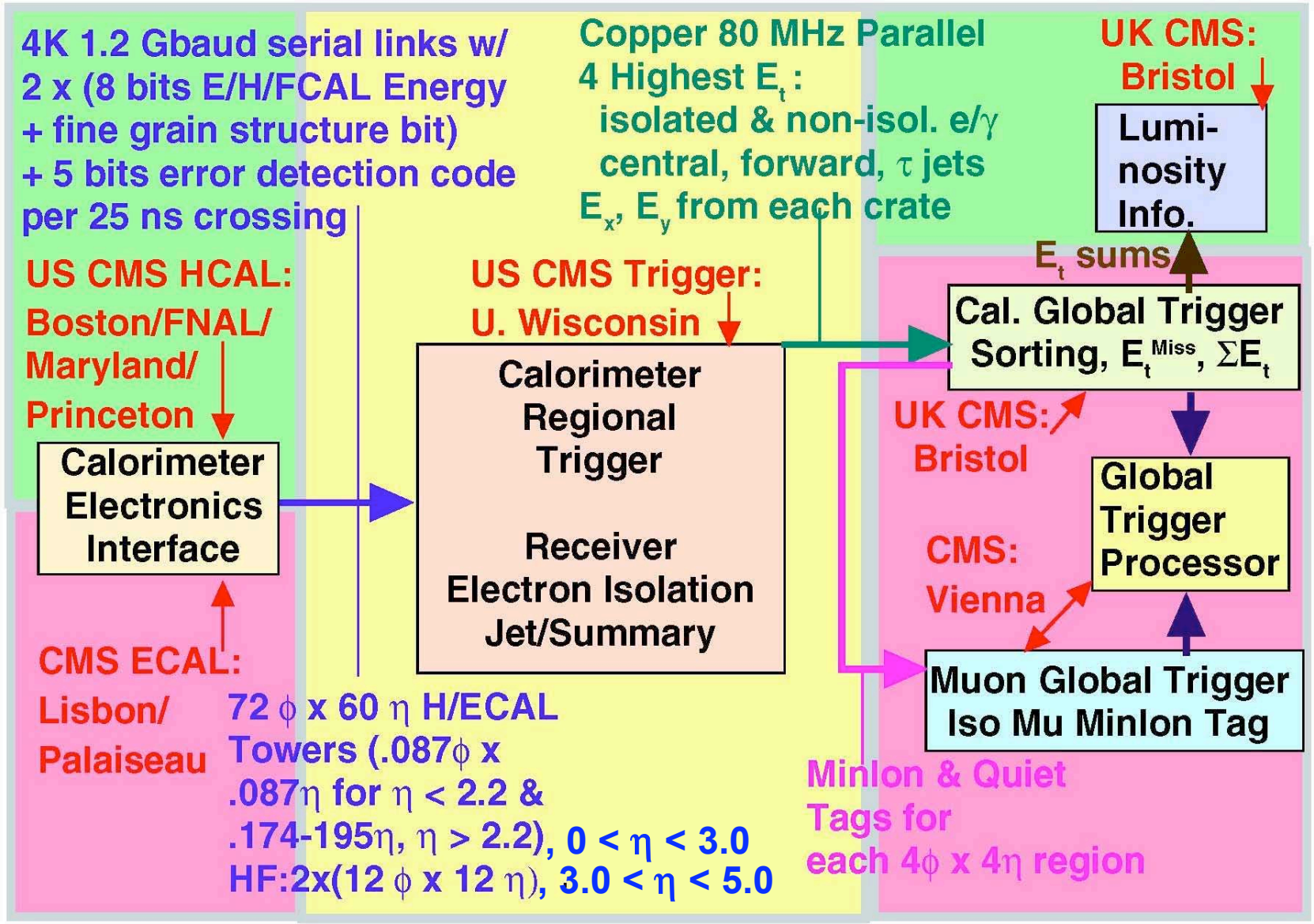
Jet or τ E_T

- 12x12 trig. tower ΣE_T sliding in 4x4 steps w/central 4x4 E_T > others

τ: isolated narrow energy deposits

- Energy outside τ veto pattern sets veto
- Jet ≡ τ if all 9 4x4 region τ vetoes off

Calorimeter Trigger Overview
(in underground counting room — USC55)

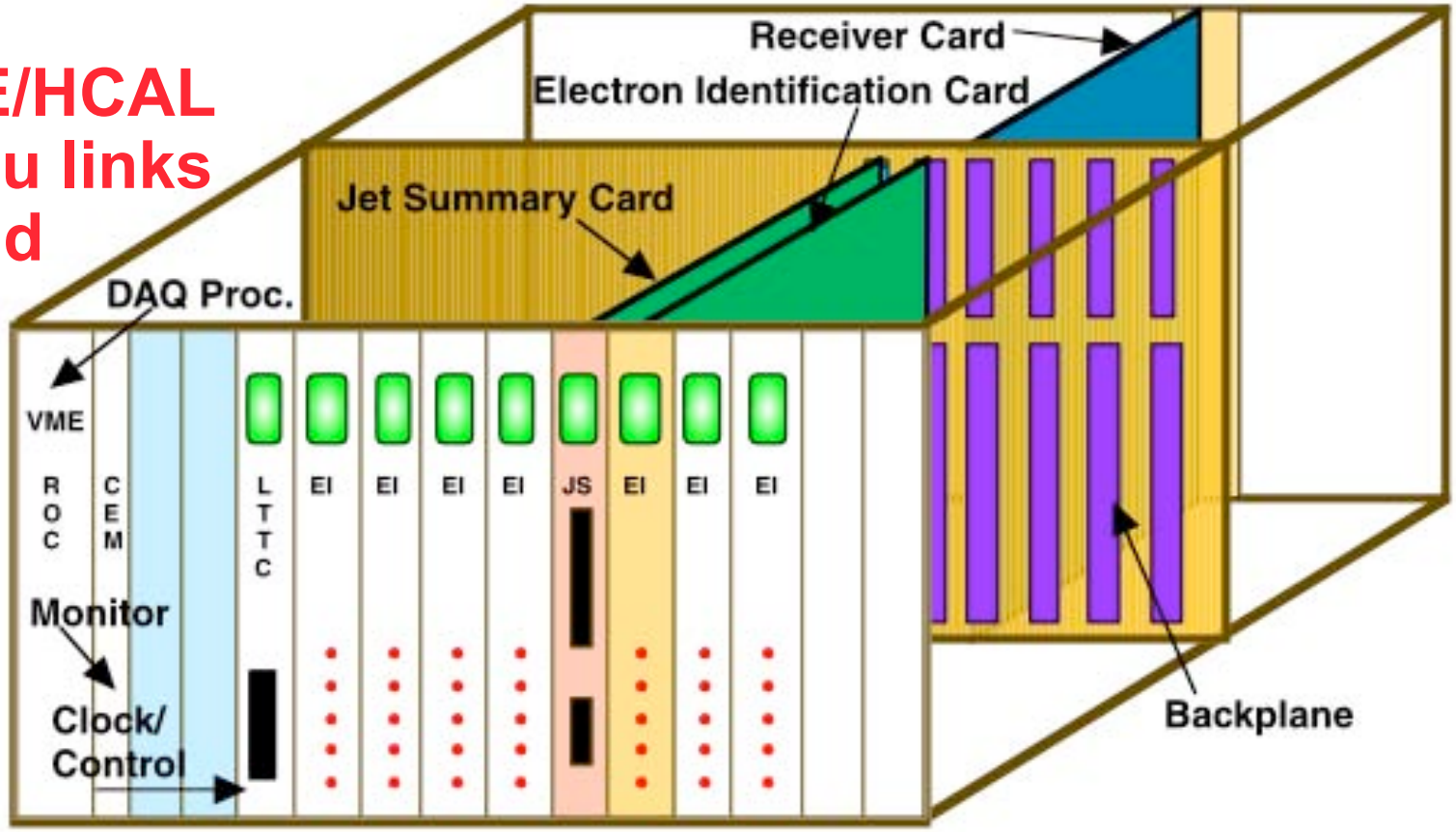


Regional Calorimeter Trigger
- U. Wisconsin

18 Crates:

Data from E/HCAL crates on Cu links @ 1.2 Gbaud

- *Into 126 rear Receiver Cards*
- *Each with 8 Receiver Mezzanine Cards (1026 total)*

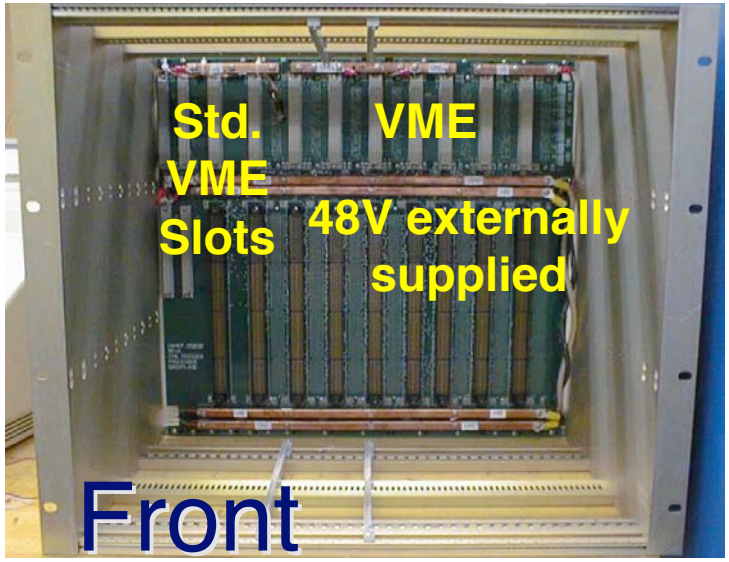


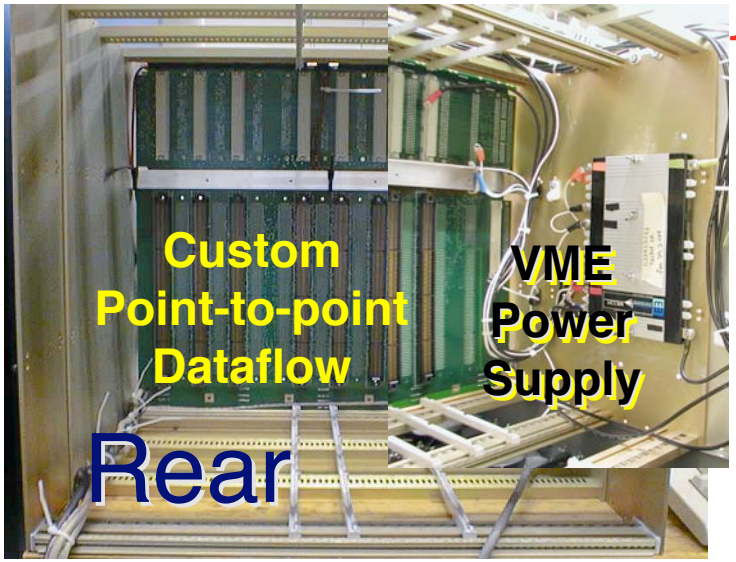
160 MHz point to point Backplane & Cards

- **18 Clock&Control ,126 Electron ID & Receiver Cards**
  18 Jet/Summary Cards
- **Use 5 Custom Gate-Array 160 MHz GaAs Vitesse Digital ASICs**
  - Phase, Adder, Boundary Scan, Electron Isolation, Sort

*Spares not included**

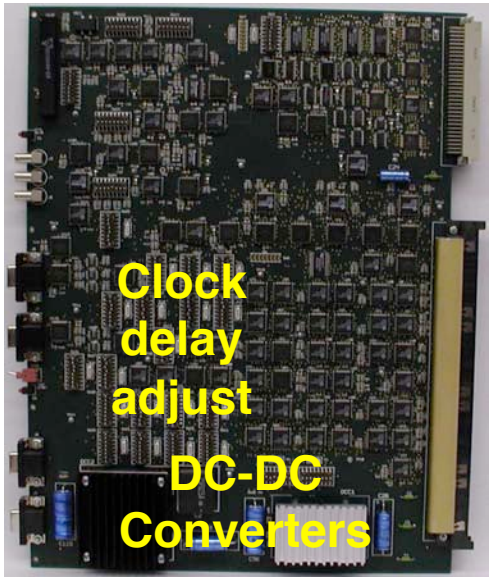
Regional Calorimeter Trigger Production: Crate, Backplane, Clock Cards - U. Wisconsin





160 MHz Backplane w/0.4 Tbit/sec dataflow:

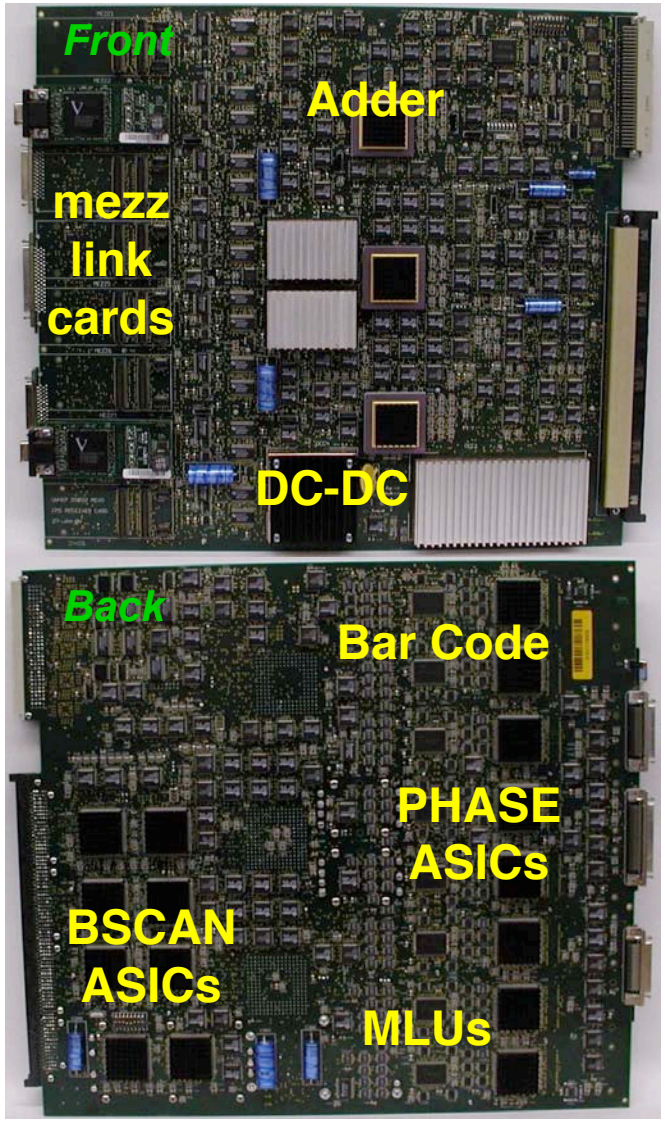
- All data paths checked
- Production version validated
- all backplanes manufactured
- 3/18+7sp tested



Clock Card:

- Receives 160 MHz and 120 MHz clocks and resets from Master Clock Card or generates clocks using an oscillator for standalone testing.
- Fans out and adjusts phase to all boards via backplane.
- All 18/25 for operation/+ spares manufactured
- 6 validated through full testing procedure
- Integrated with full crate of RCT boards. Run with clock arriving via cable (from another CCC).

RCT Production: Receiver Card (RC) & Receiver Mezzanine Card (RMC) – U. Wisconsin



Receives 64 ECAL/HCAL trigger primitives and fine grain bits via Cu cable using 8 Vitesse 1.2 Gbaud links on RMCs.

2 4x4 Tower sums are created and sent to Jet/Summary Card with 2 MIP (OR of 4x4 HCAL FG) and 2 τ-veto bits (patterns).

16 towers of E_T sent directly to an Electron Identification Card and duplicated for edge information for other cards.

Crate-to-Crate sharing on cables of edge and corner towers for e/γ algorithm.

126/154 RCs necessary to operate/including spares

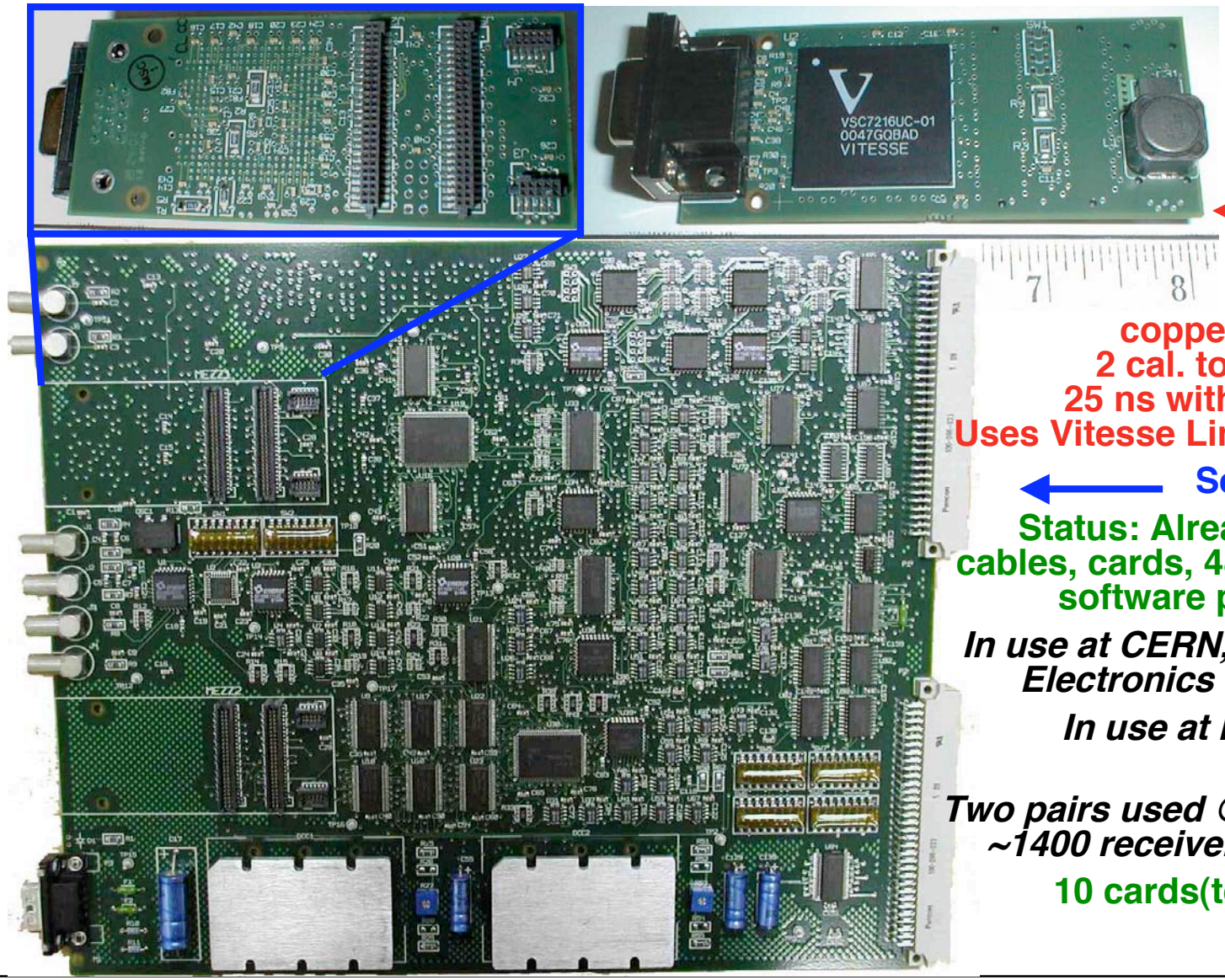
All 154 manufactured and delivered, 5 validated

All 1026/1420 RMCs delivered and tested

Full crate tests performed

Initial Integration with HCAL HTR & SLB performed, more tests planned with HCAL & ECAL

RCT 4 Gbaud Copper Link Cards & Serial Test Card – U. Wisconsin



Compact Mezzanine Cards for each Receiver Card accept 4 x 20 m 1.2-Gbaud copper pairs transmitting 2 cal. tower energies every 25 ns with low cost & power. Uses Vitesse Link Chips (7216–01).

Serial Link Test Card

Status: Already commissioned, cables, cards, 48V PS, and support software provided to groups.

In use at CERN, operating in ECAL Electronics lab for testing SLB.

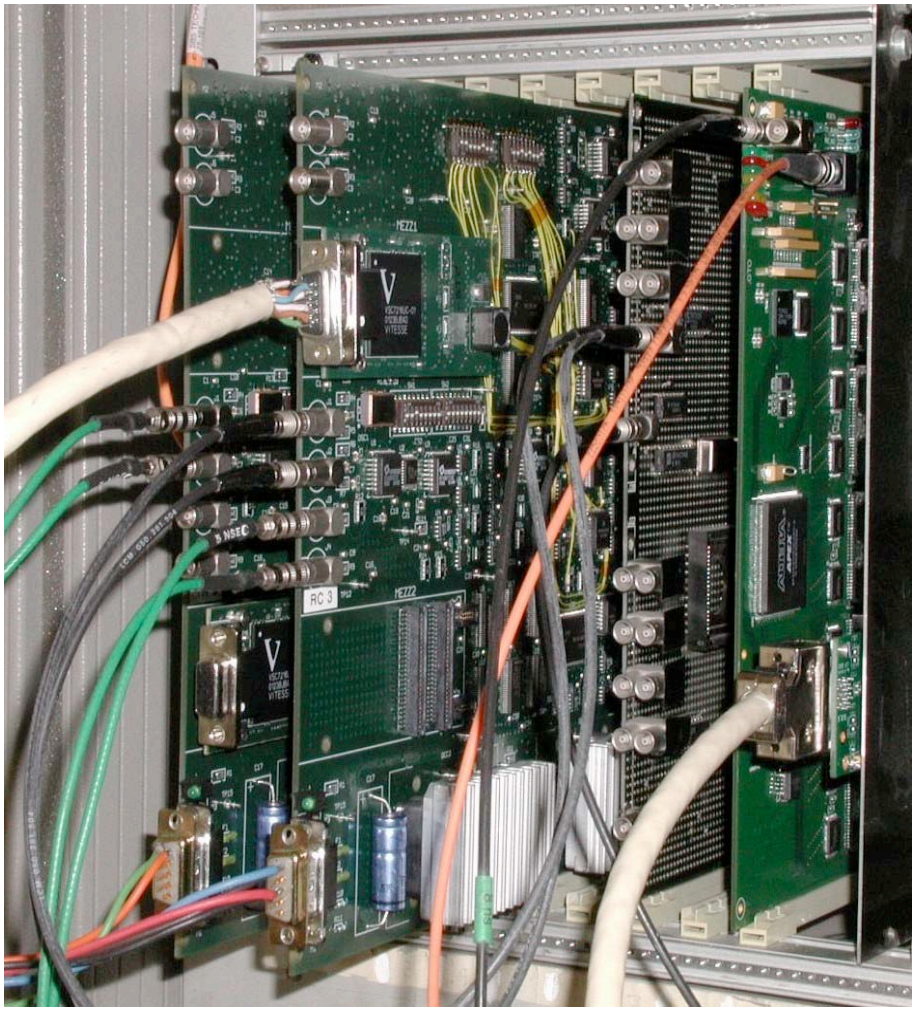
In use at Maryland for HCAL HTR/SLB tests.

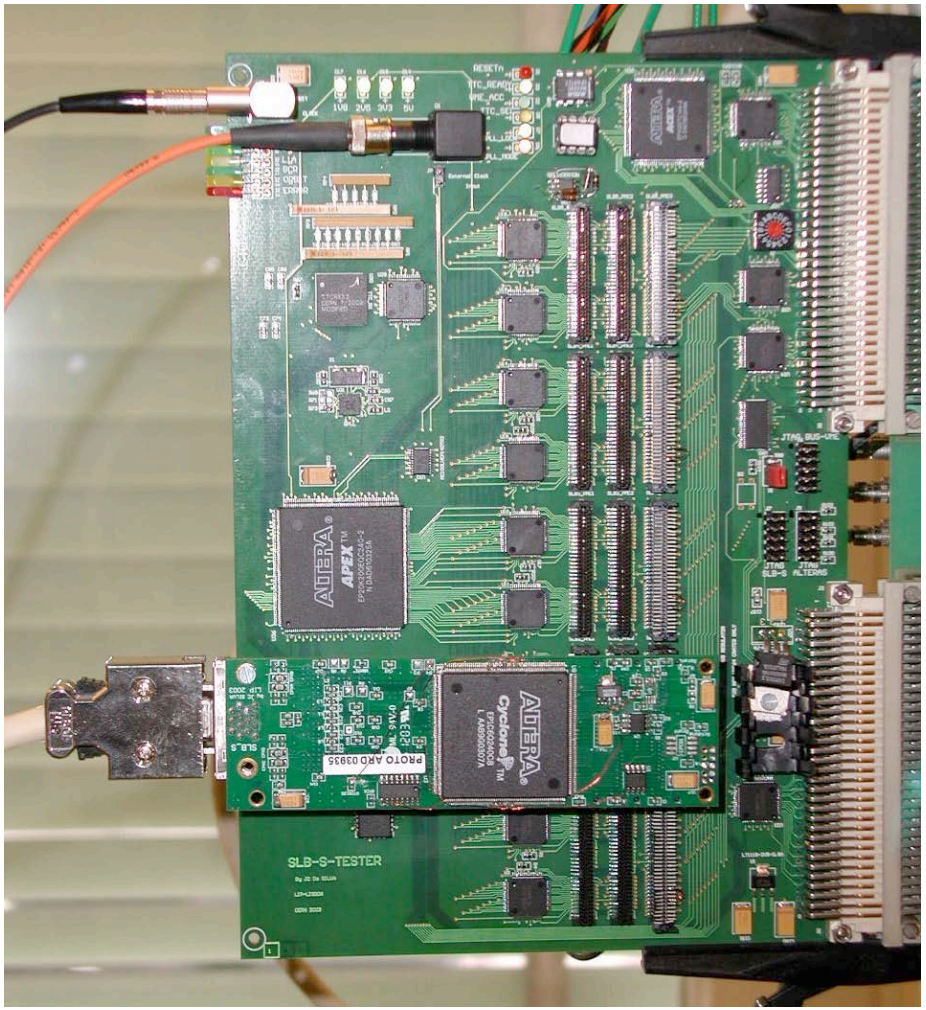
Two pairs used @ UW for testing all ~1400 receiver mezzanine cards..

10 cards(test only-not in final system).

SLB-STC link test setup

Lisbon-Wisconsin

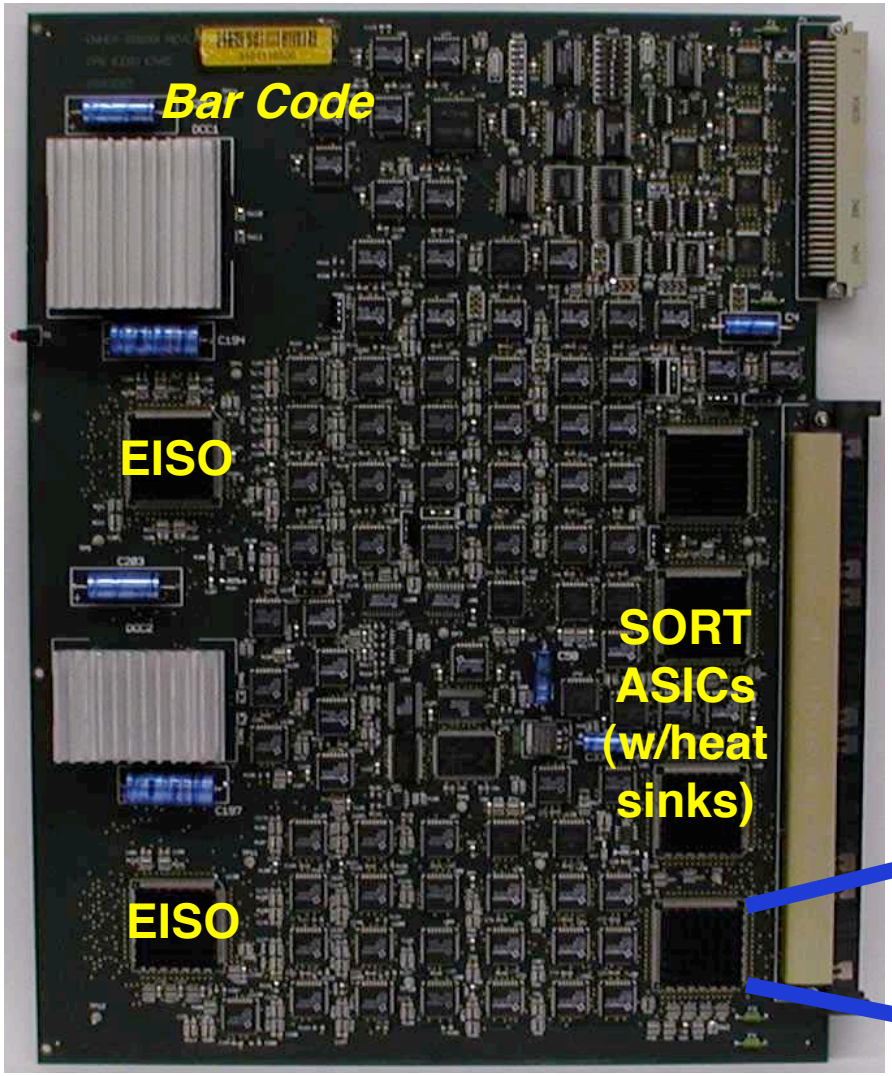


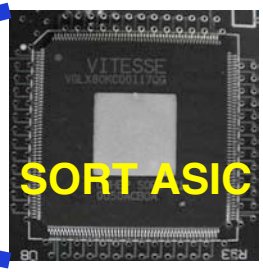


Test of link from Calorimeter to Regional Trigger

Electron Isolation Card (EIC)

— U. Wisconsin





Receives 16 central towers directly from adjoining RC and 32 edge and corner towers from adjacent RC's or via cables into adjoining RC.

EISO ASIC uses this information to produce one isolated and one non-isolated e/γ candidate for each 4x4 trigger tower region which are sent via backplane to Jet/Summary Card for sorting.

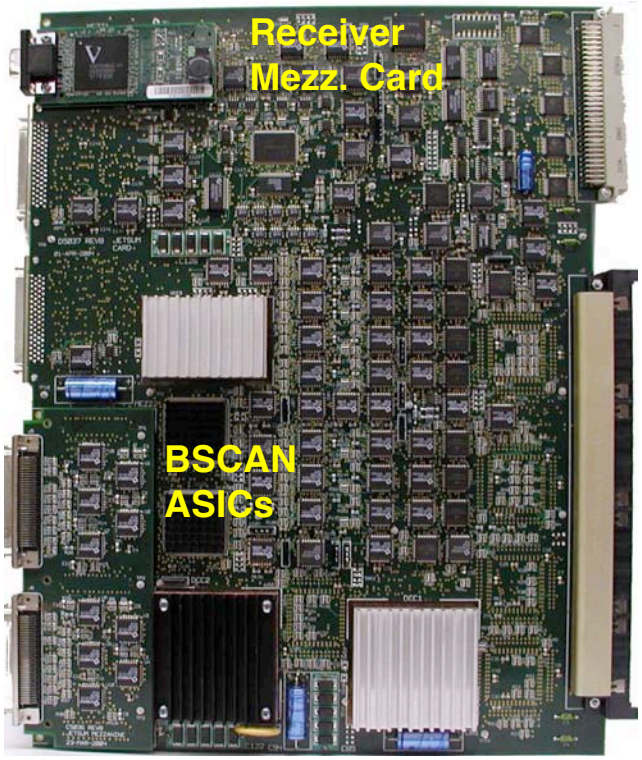
126/154 for operation/total produced

153 of 154 tested and working

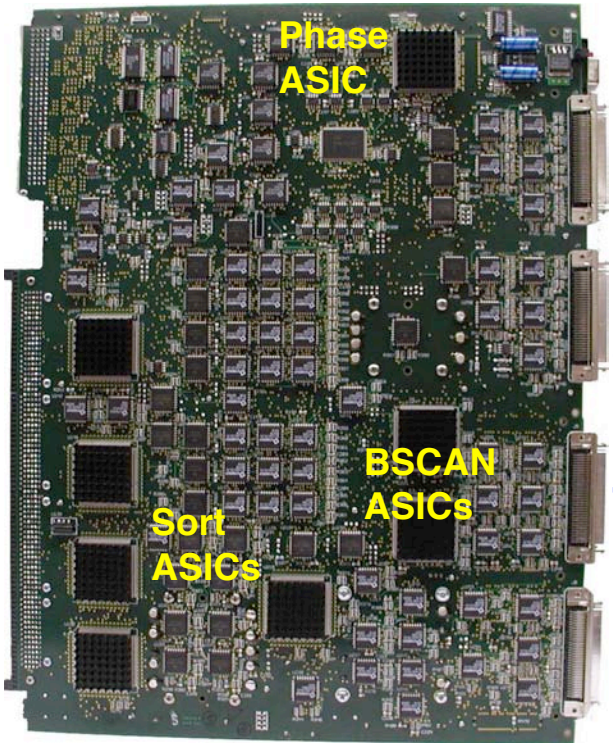
1 back to vendor for part replacement

Completely validated in full crate tests

Jet/Summary Card (JSC)
— U. Wisconsin



Input via Backplane:
28 e/γ per
14 Region E_T Sums,
MIP, t bits



Output:
14 Region E_T Sums, 14 each MIP,t,Quiet bits
8 e/γ – 4 each Iso. and non-iso.
On 6 Cables To GCT
(2 on Mezz. Card)

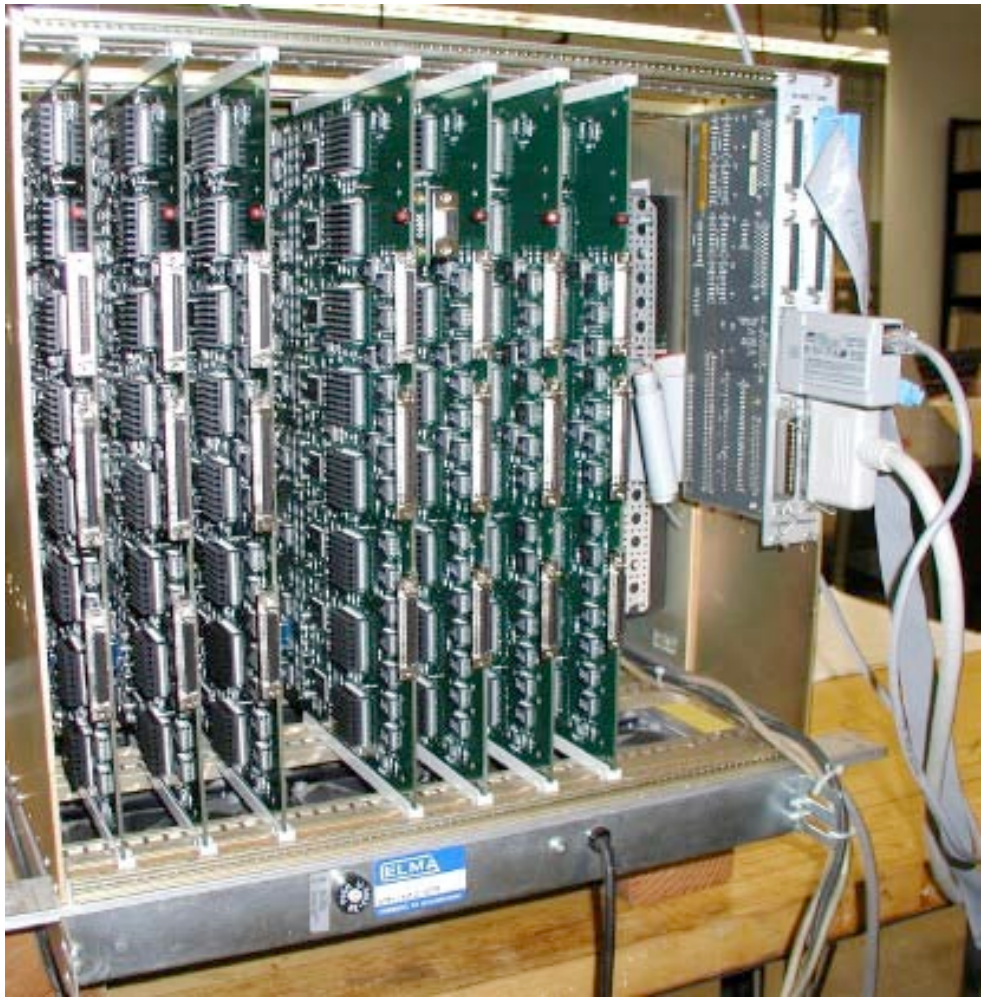
Uses SORT ASICs to find top four e/γ, threshold for quiet bits. Receives 8 HF regions with Rec. Mezz. Card. Full crate test – all output/input paths verified, electron sort, jet output all verified. Integration test with GCT Done

18/25 for operation/including spares

Revision B 100% validated, Revision C (final) in production.

RCT Full Crate Test - U. Wisconsin

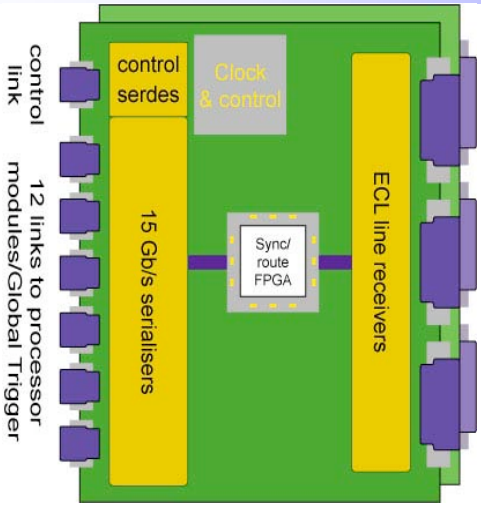
Full System Test of all pre-production prototypes in final configuration.



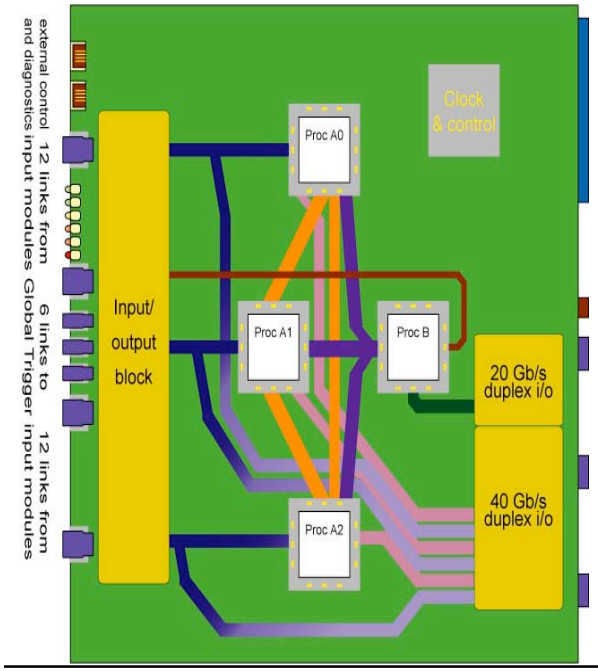
Rear: Receiver Cards

Front: Electron, Jet, Clock Cards

Global Calorimeter Trigger
— Bristol U.

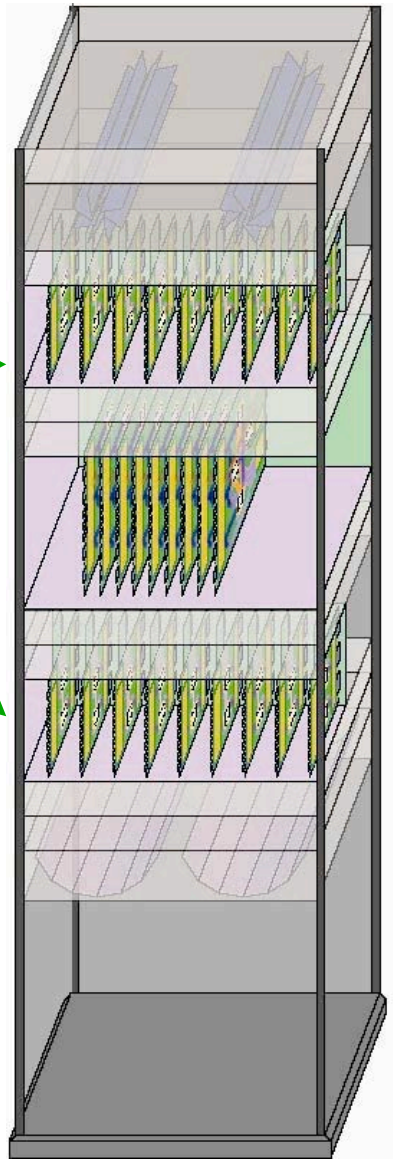


crates of input modules



Processor module crate

Housed in a single rack



2U monitoring unit
4U tangential fan unit
2U heat exchanger

6U input crate

2U fan tray
2U heat exchanger

9U processor crate

2U fan tray
2U heat exchanger

6U input crate

2U fan tray
2U heat exchanger
3U air flow guide

44U required for GCT
12U spare

Global Calorimeter Trigger: Input module prototyping —Bristol U.

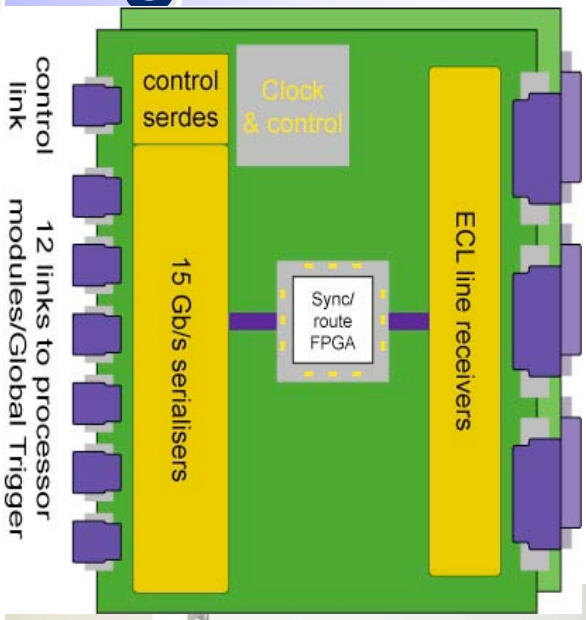
Tested first proto-IM in 2003

- Full function, half channel count
- Demonstrated data transfer input from RCT, out to GT
- Reported to 2003 Annual Review

Now testing pre-production IMs

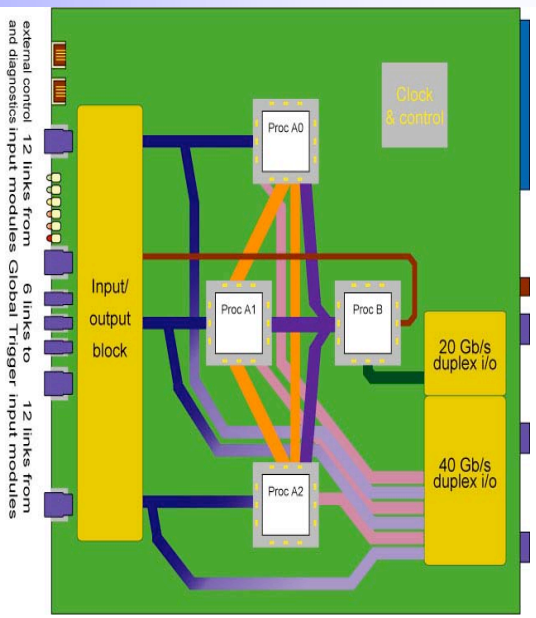
- Verified clocking, FPGA, TPM interface
- Built test boxes for ECL input stage
- Testing finished in Oct ’04

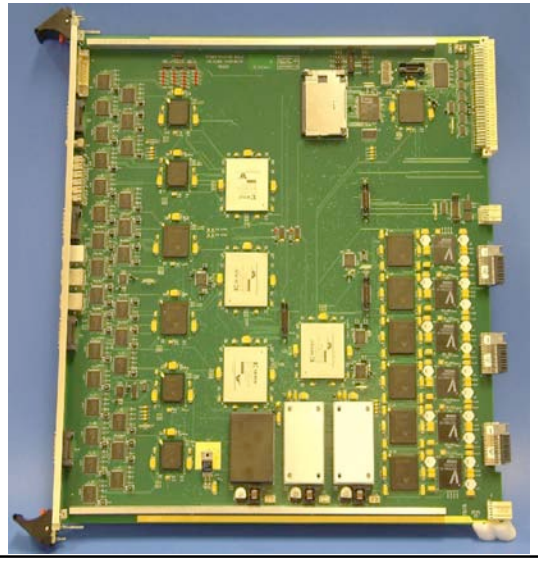
IM production to start Dec ’04



GCT Trigger Processor Module
— Bristol U.

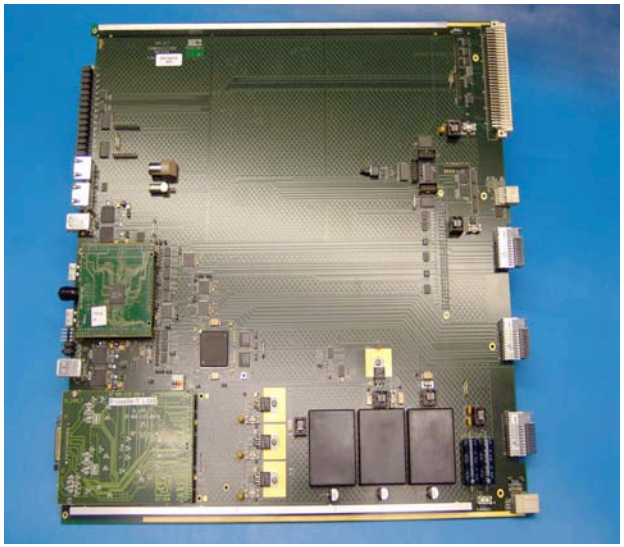
- Prototype TPMs were delivered in January 2004
- Verified clocking, links and data paths
- Second iteration prototype is required
  - Routing of TPM2 has started
  - Out to manufacture end Nov
- Aiming for final production July-Aug ’05



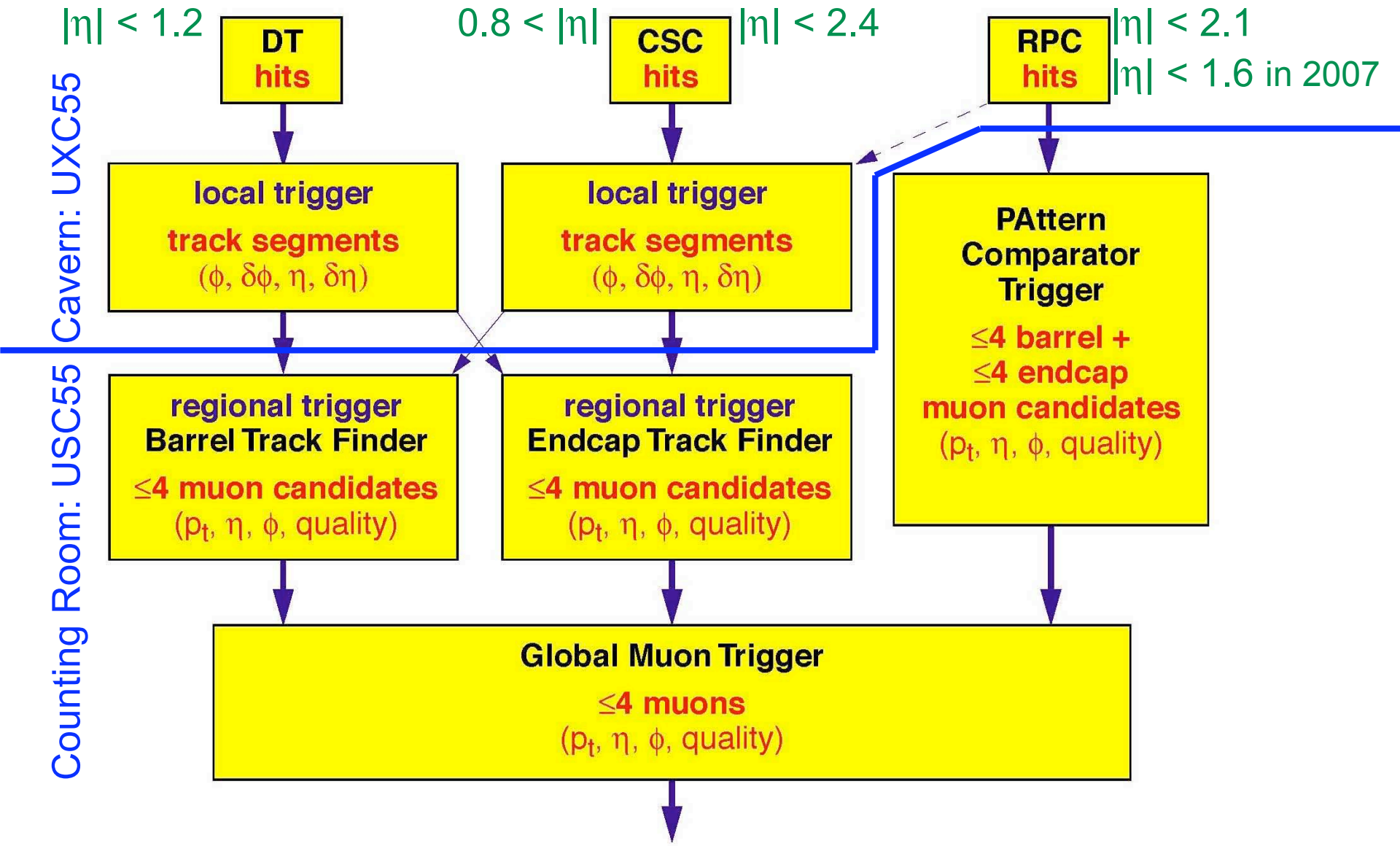


GCT hardware components
— Bristol U.

- Crates, cables used in lab testing
  - Placing orders for final production items
- Communications Module for clock fanout and DAQ interface
  - Testing started mid-August
  - Looks good so far
  - Firmware effort needed



Muon Trigger Overview

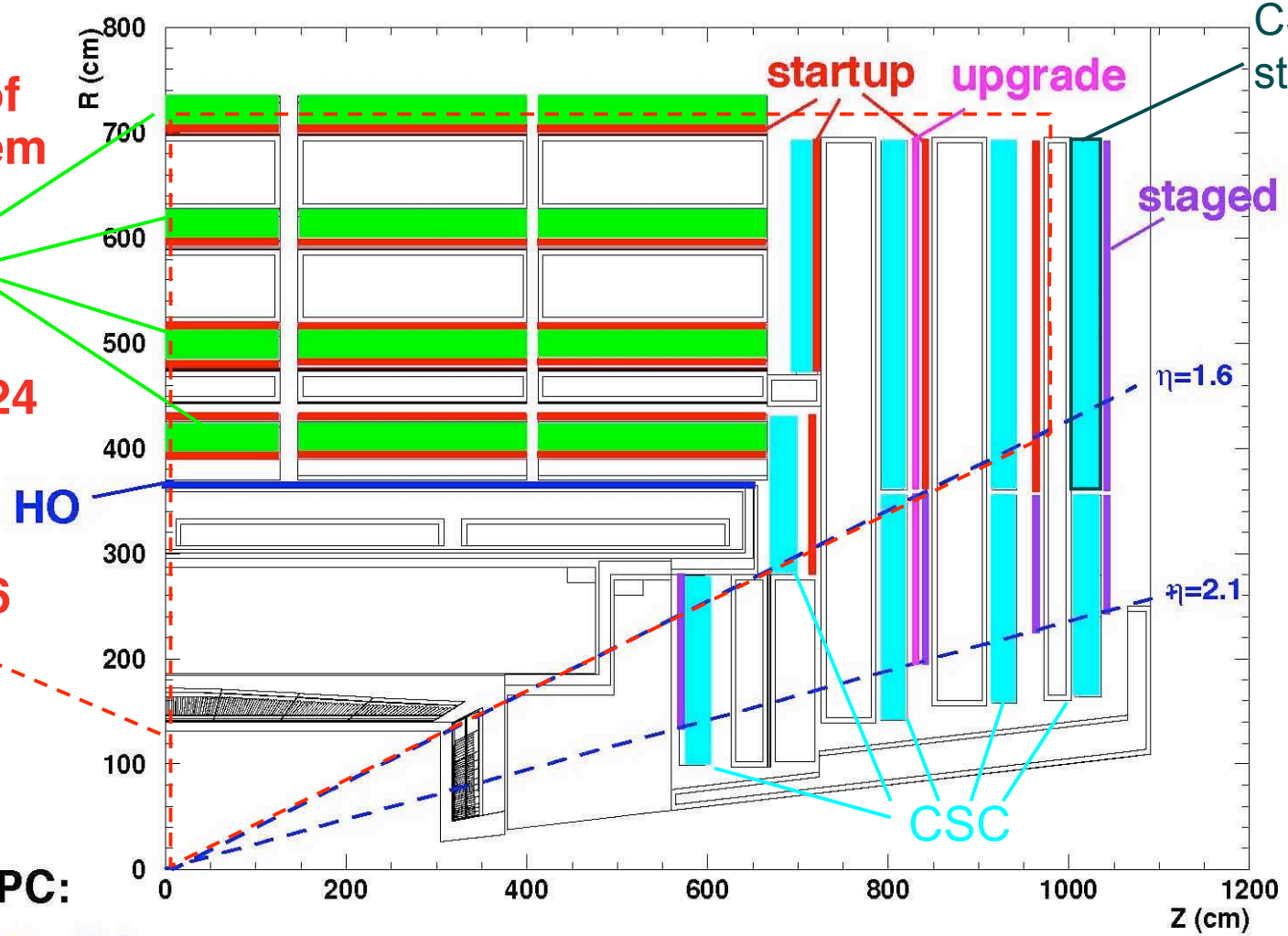


RPC Trigger Geometry

Coverage of initial system in 2007:

4 stations: up to η~ 1.24

3 stations: up to η ~1.6



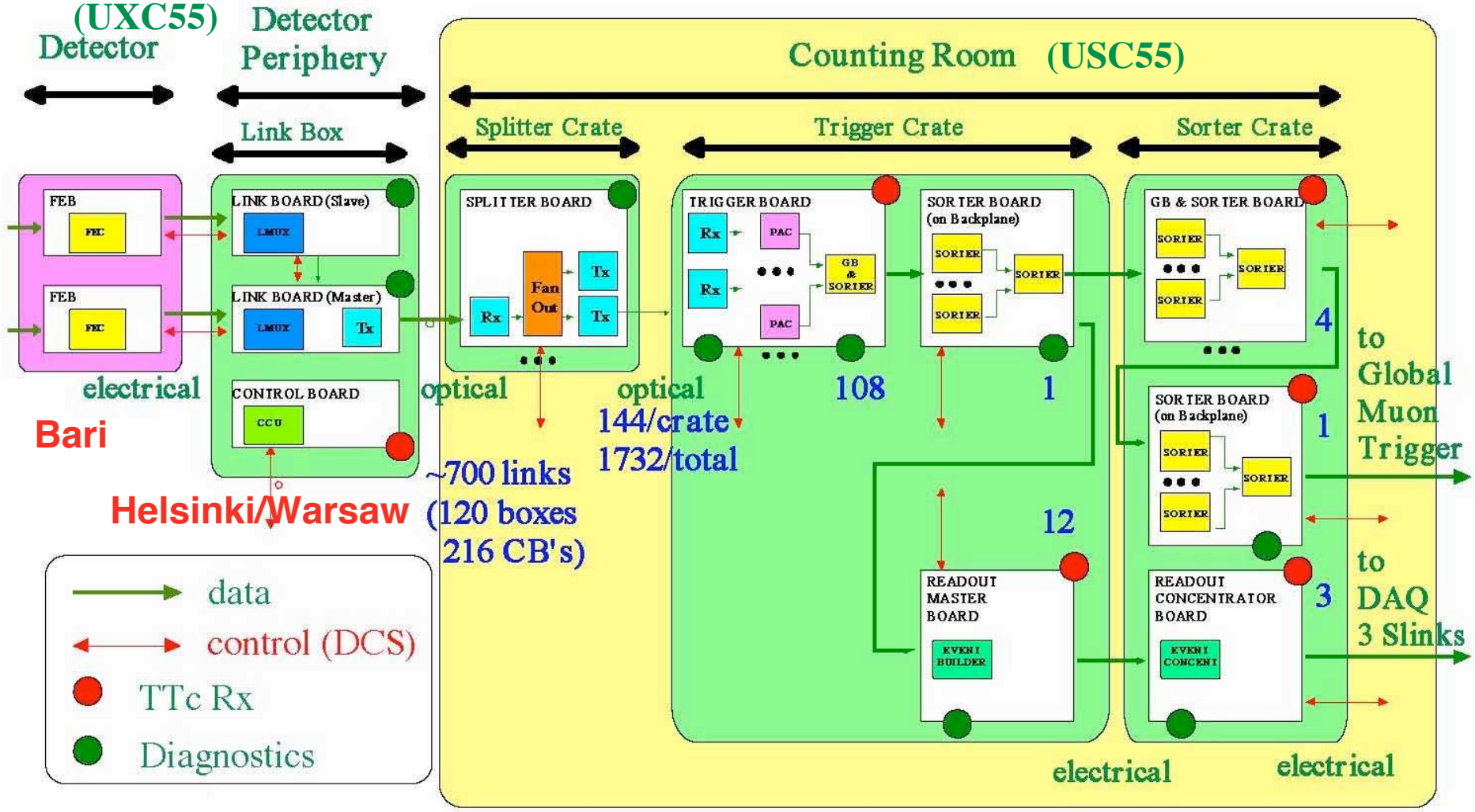
Barrel RPC:

- RB 1,2 = 2 layers
- RB 3,4 = 1 layer

Endcap RPC:

- RE 1,2,3,4,(5) = 1 layer

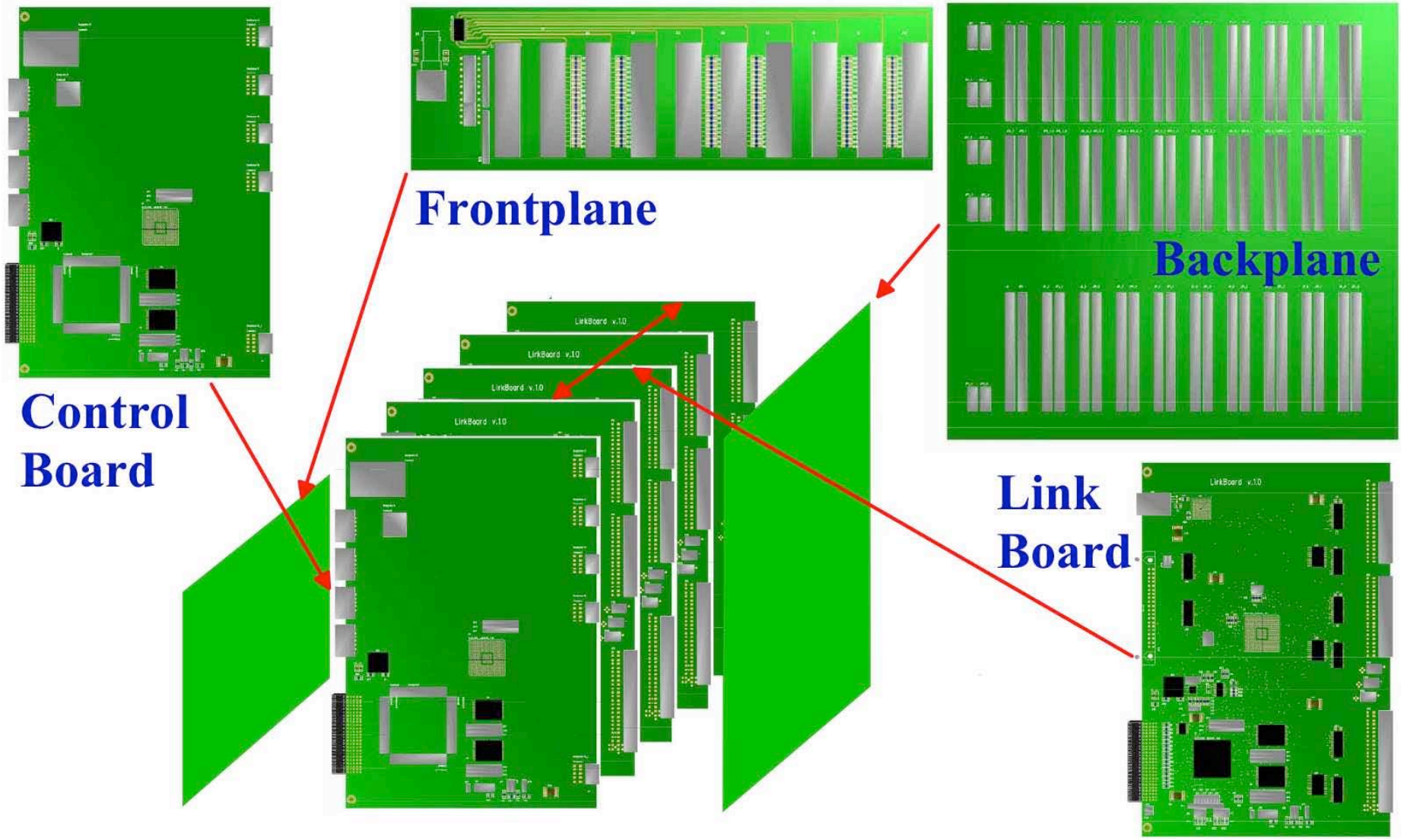
RPC Electronics Layout



RPC Link Boxes on Detector

— Bari, Helsinki, Lappeenranta, Warsaw

Link System tested & approved for production, cables & fibres ~ defined

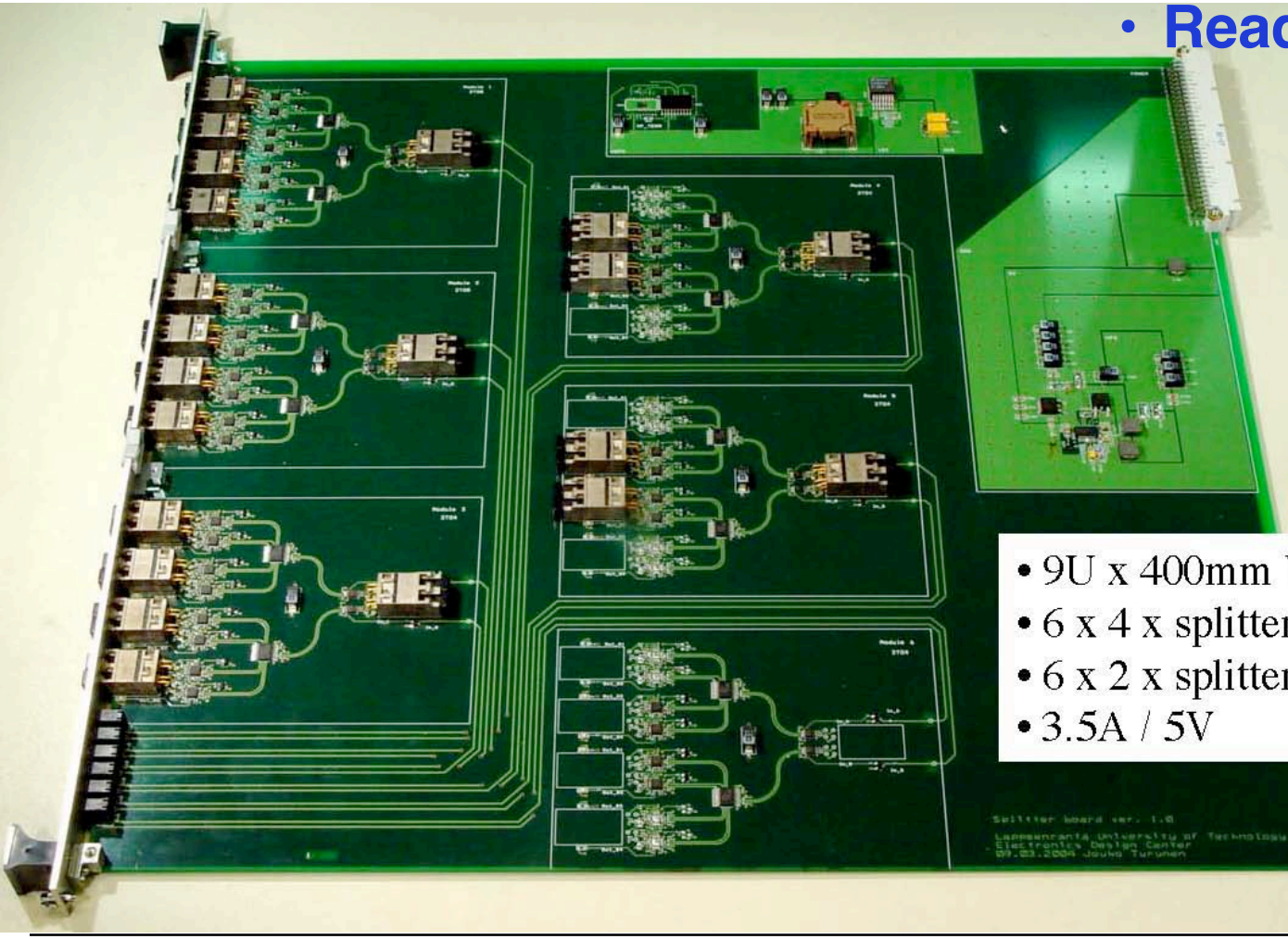


RPC Trigger Splitter in USC55

— Lappeenranta

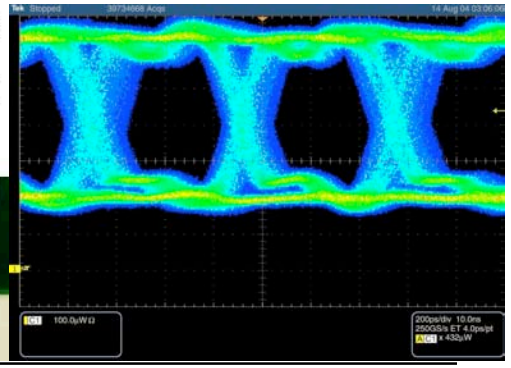
Full size & function pre-production prototype tested

- BER tests passed for 60 – 100 MHz clocks
- Ready for production with minor mods



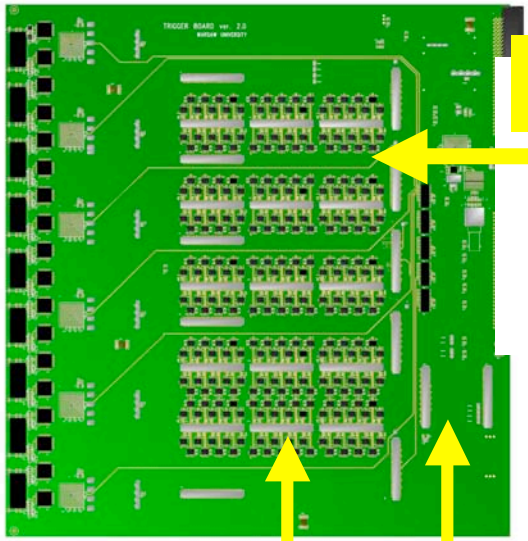
- 9U x 400mm VME board
- 6 x 4 x splitter
- 6 x 2 x splitter
- 3.5A / 5V

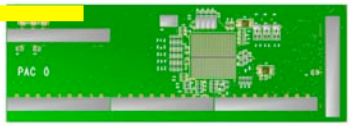
- splitter output after 100 m fiber
- 80 MHz clock
- 200 ps scale



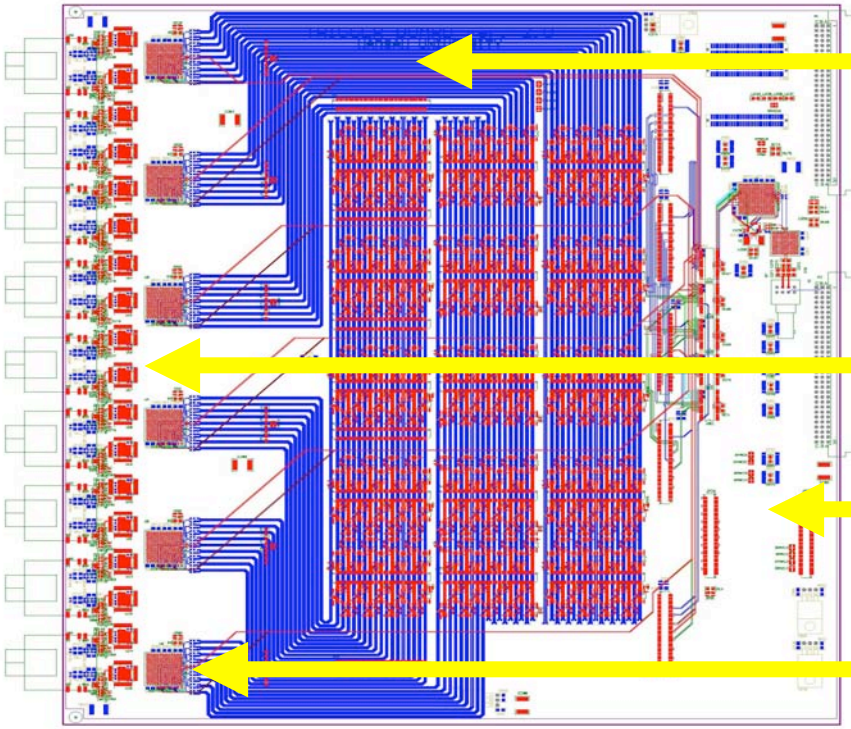
RPC Trigger Board
— Warsaw

Pre-production prototype now being manufactured





4 PAC mezzanines



Bus of 54 lines@ 160 MHz

18 Optical Links

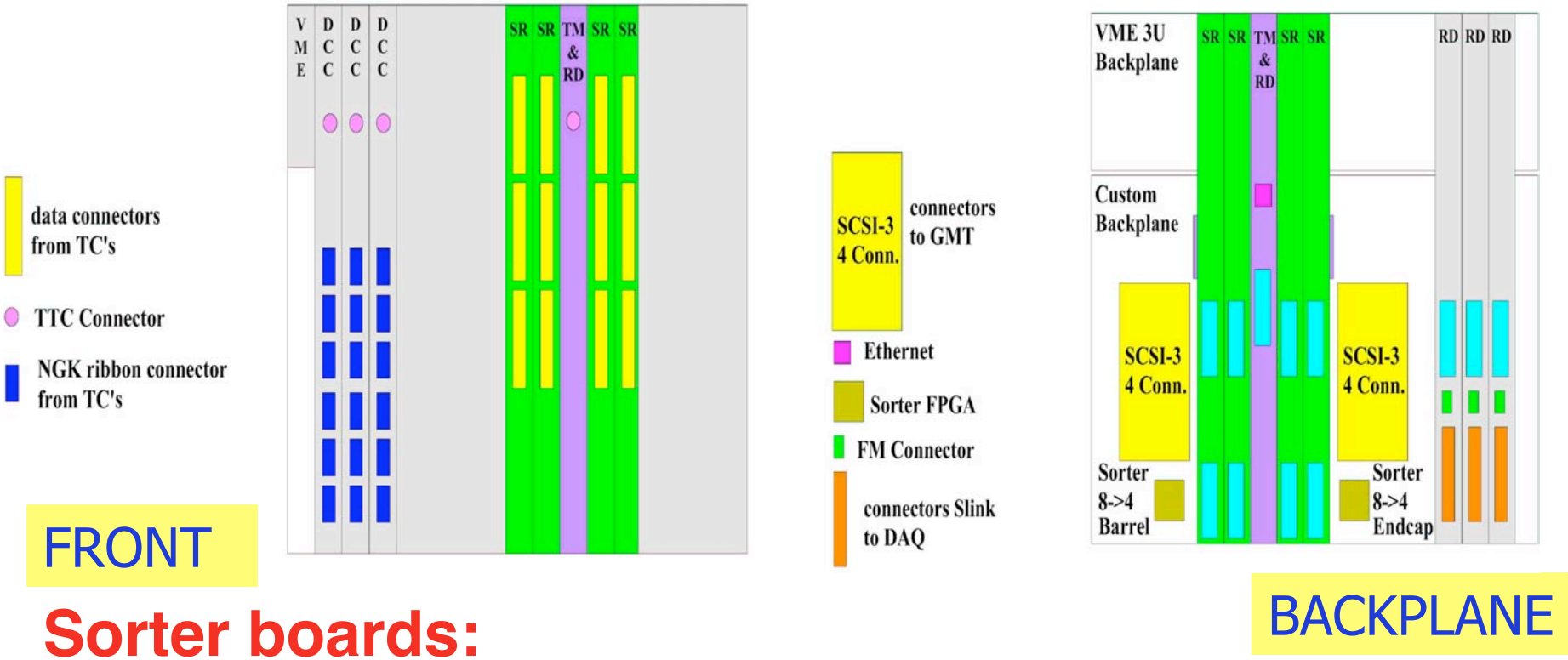
Ghost Buster

LDEMUX FPGA

Readout mezzanine

Ghost Buster mezzanine

New RPC Sorter Crate
— Bari



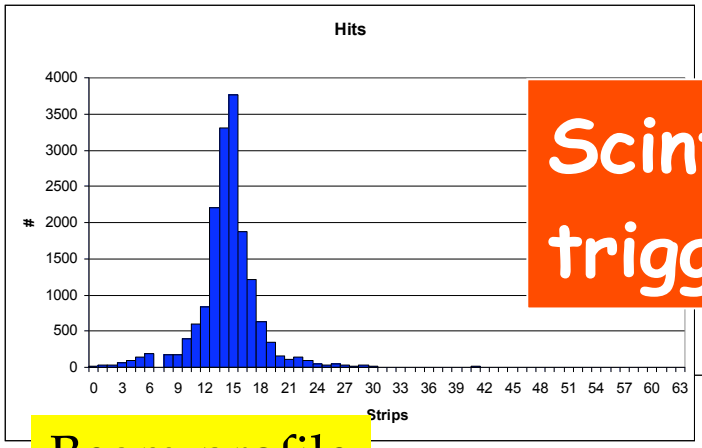
Sorter boards:

- Under design

Read out Subsystem:

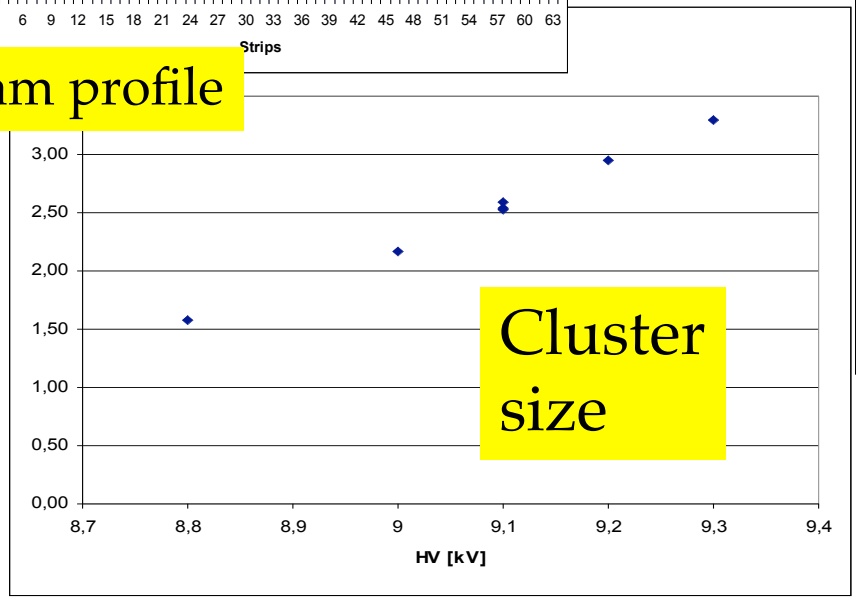
- Customized DCC (ECAL) to be tested in October 2004

RPC Trigger in June 2004 structured test beam

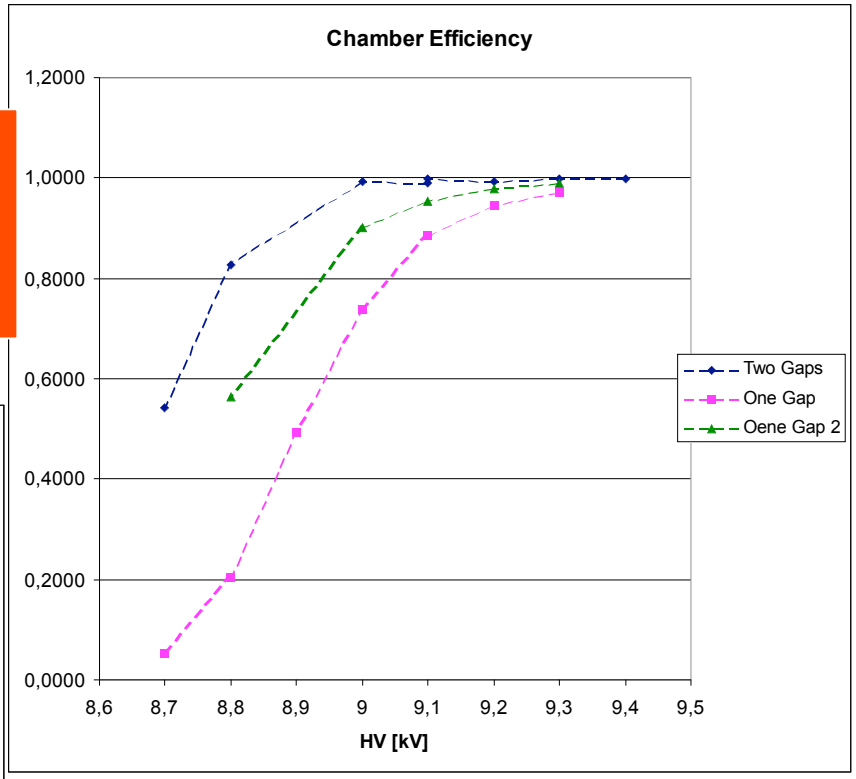


Scintillator trigger

Beam profile



Cluster size



RE12 RPC efficiency: global, 1st gap, 2nd gap

June 2004 RPC Trigger Synchronization with CSC Trigger

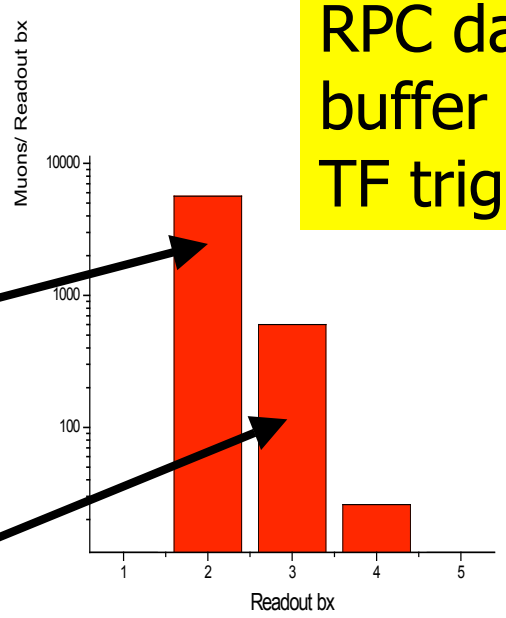
Initial results promising

More tests during the October 25ns beam test.

It seems that the RPC data will be useful for the CSC TF

TF trigger and RPC data at The same BX

TF trigger 1BX too early

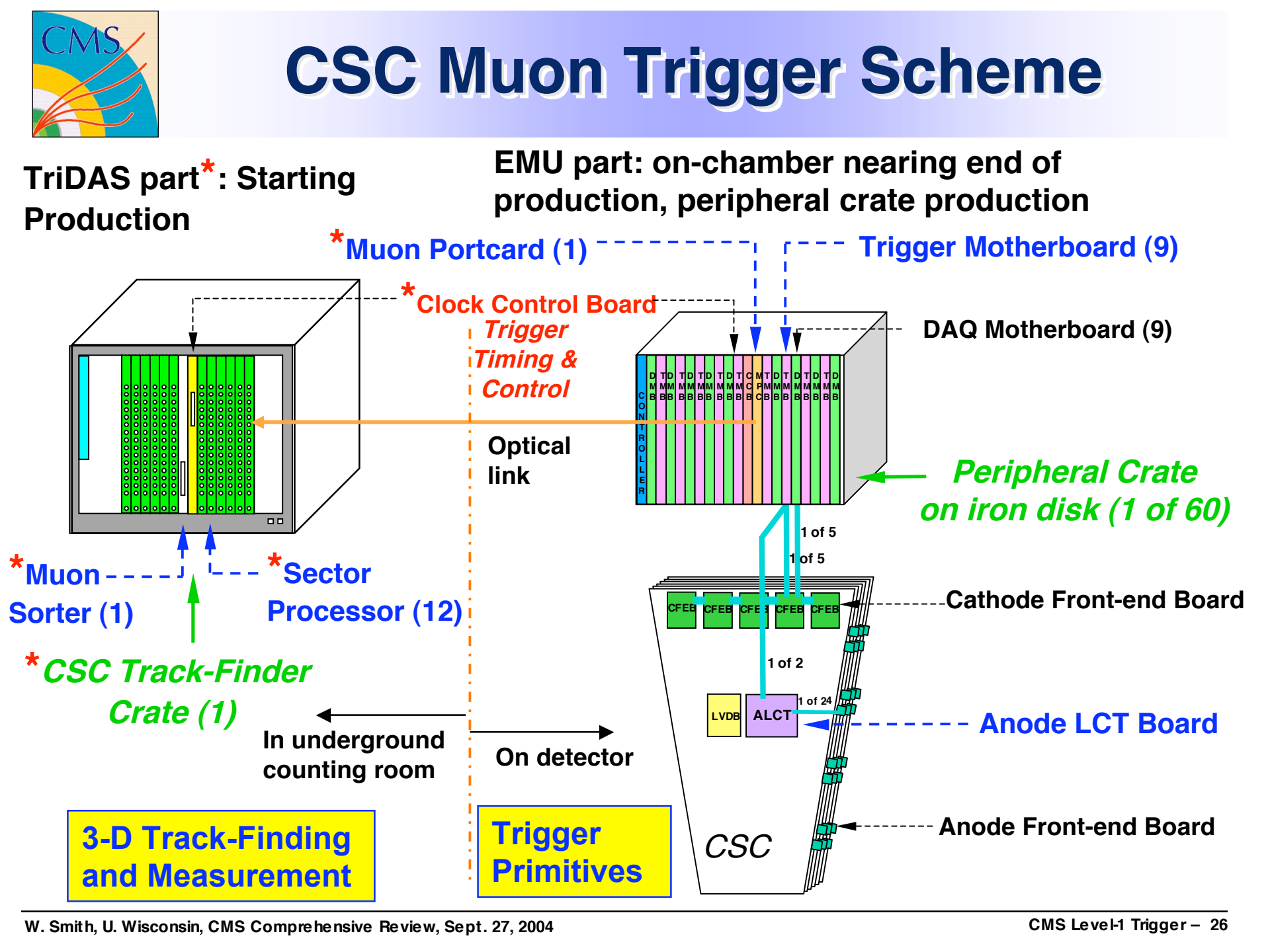


RPC data in the buffer for TF trigger

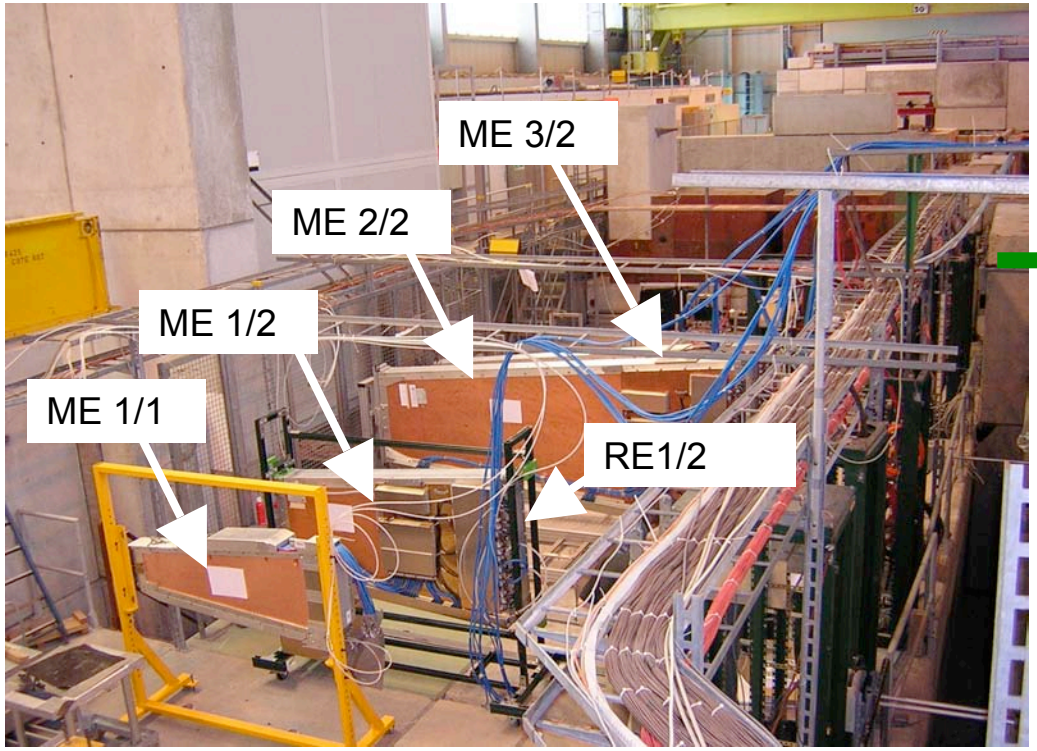
CSC Muon Trigger Scheme

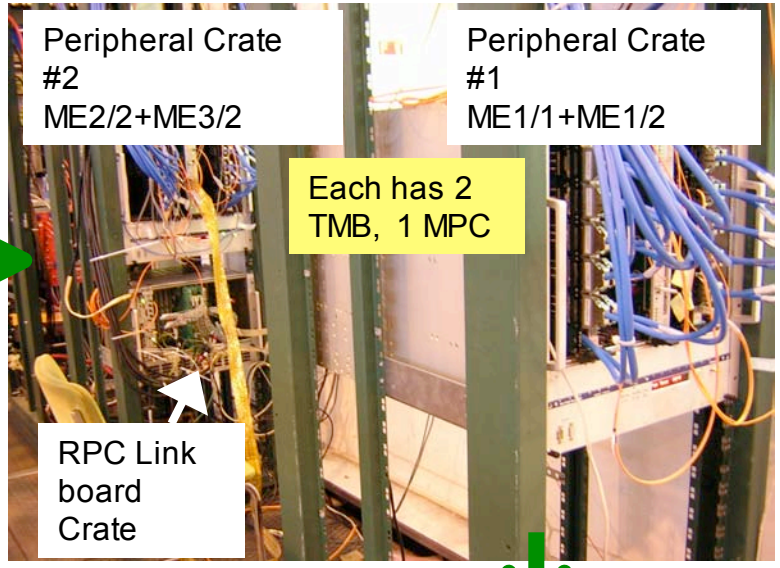
TriDAS part*: Starting Production

EMU part: on-chamber nearing end of production, peripheral crate production



CSC Trigger June 2004 Structured Beam Tests





Track-Finder Crate (next slide)

First time used full Track-Finding logic to identify tracks in data

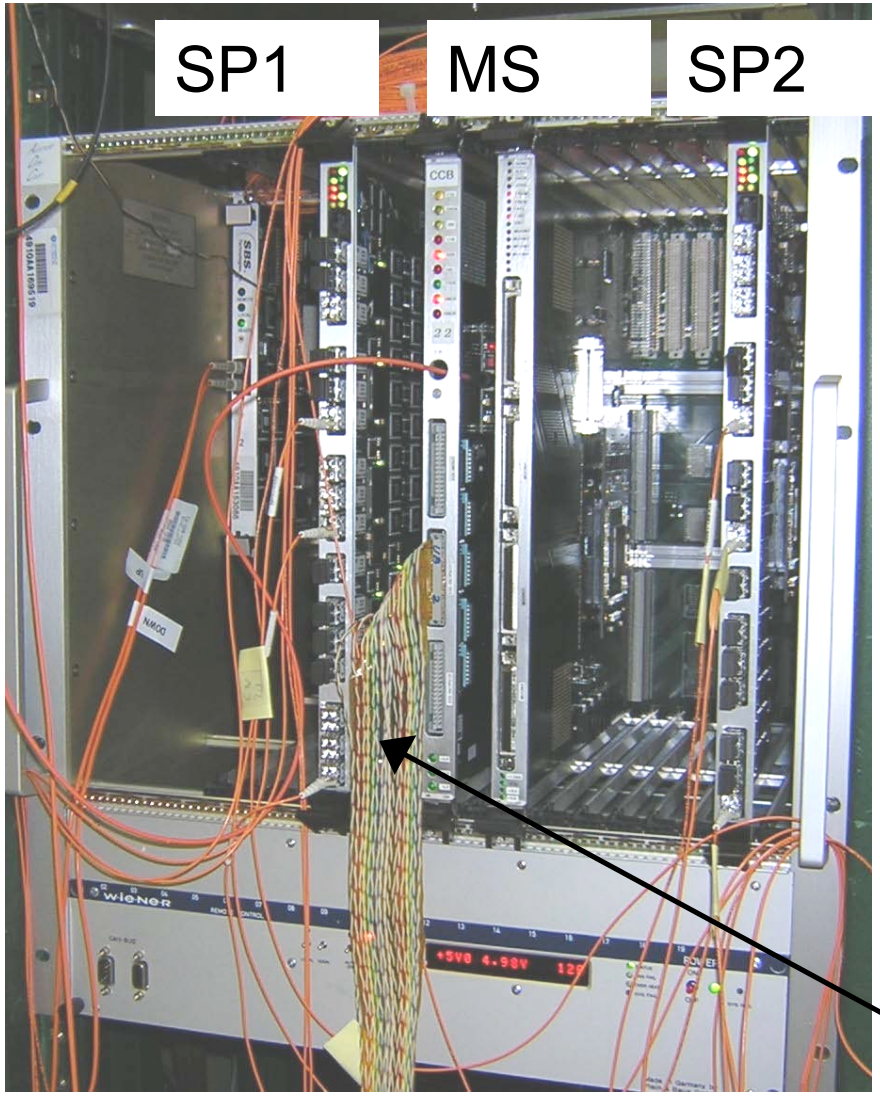
Full DAQ logging of inputs and outputs for offline comparisons

- **Compare with data sent by Peripheral Crates & internal TF logic**

L1A generation a major synchronization accomplishment for trigger

- **Data must be aligned spatially and temporally**
- **Very useful for slice tests**

Track-Finder Crate Tests
— Florida, Rice, UCLA



First test of multiple peripheral crates (multiple MPC) to TF crate

- Synchronization test

Various clocking solutions tried to test robustness of optical links

- MPC used QPLL 80 MHz clock on backplane for all 25 ns runs

First test of multiple Sector Processors (SP) to one Muon Sorter (MS)

L1A signal distributed out of crate

CSC Track-Finder Beam Tests

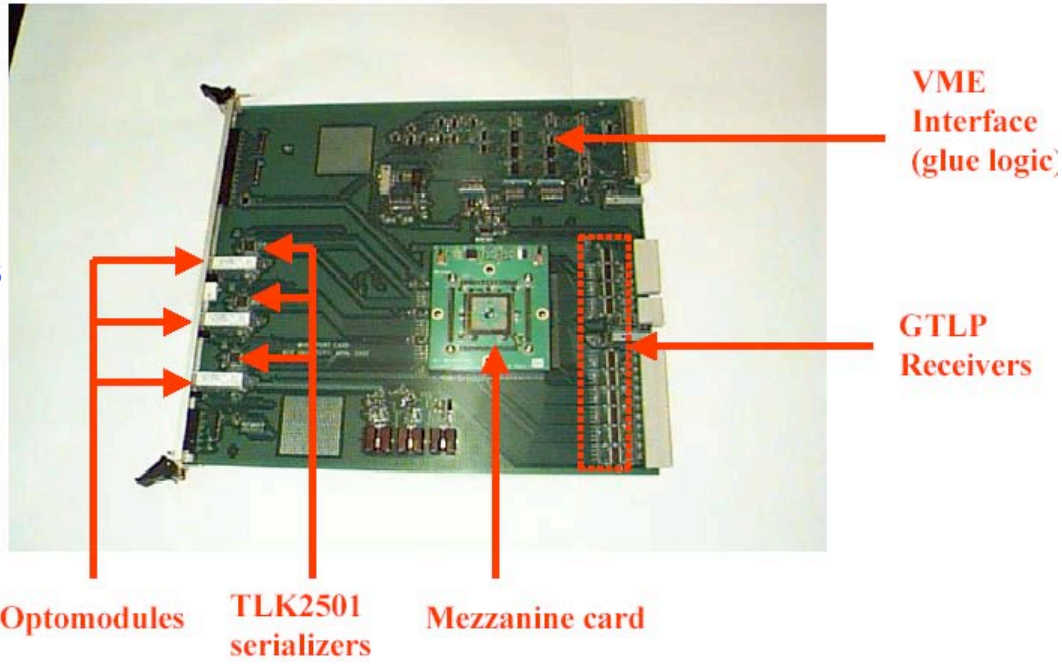
— Florida, Rice, UCLA

- Fully operational CSC TF tested with full data format
- Agreement between the output of the Sector Processor (SP) with simulation based on logged inputs is 100%
- Agreement between the recorded trigger primitive data (via DAQ from Trigger Mother Board) and received SP data is generally at the level of 99.7%
  - Same level of agreement as obtained from the Sep.'03 beam test
- The SP in conjunction with a specially modified Clock and Control Board was able to self-trigger the experiment (including RPC)
- Muon Sorter winner bits appear to be properly recorded
- New DT/CSC transition card works

CSC Trigger Muon Port Card & Clock & Control Board – Rice

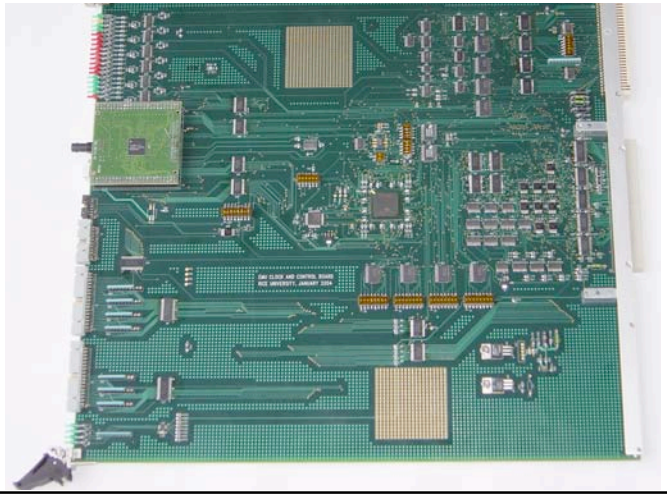
Muon Port Card:

- 6 boards built in 2002, equipped with FPGA mezzanines
- Tested on the bench
- Tested w/7 Trigger Motherboards & one Sector Processor
- Checked in peripheral crates in beam test at CERN in Sept. 2003 & June 2004
- Radiation tested at UC Davis cyclotron



Clock & Control Board;

- 6 boards built in spring 2004, equipped with TTCrq mezzanines
- Tested on the bench
- Tested w/7 Trigger Motherboards & one Sector Processor
- Checked in peripheral crates in beam test at CERN in June 2004
- Radiation tested at UC Davis cyclotron



CSC Track-Finder Status
— Florida & Rice

DT/CSC Transition Card (Florida):

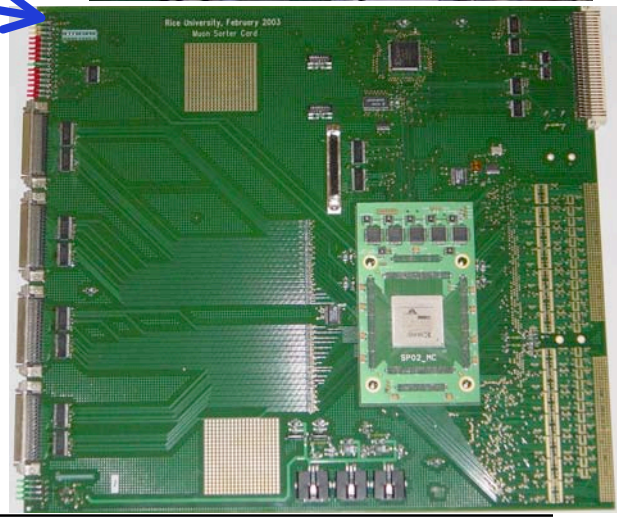
- New version tested June '04

Sector Processor Board (Florida):

- Schematics for final design modifications completed
- Routing modifications submitted to vendor, about 2 weeks to complete
- Production to commence in October

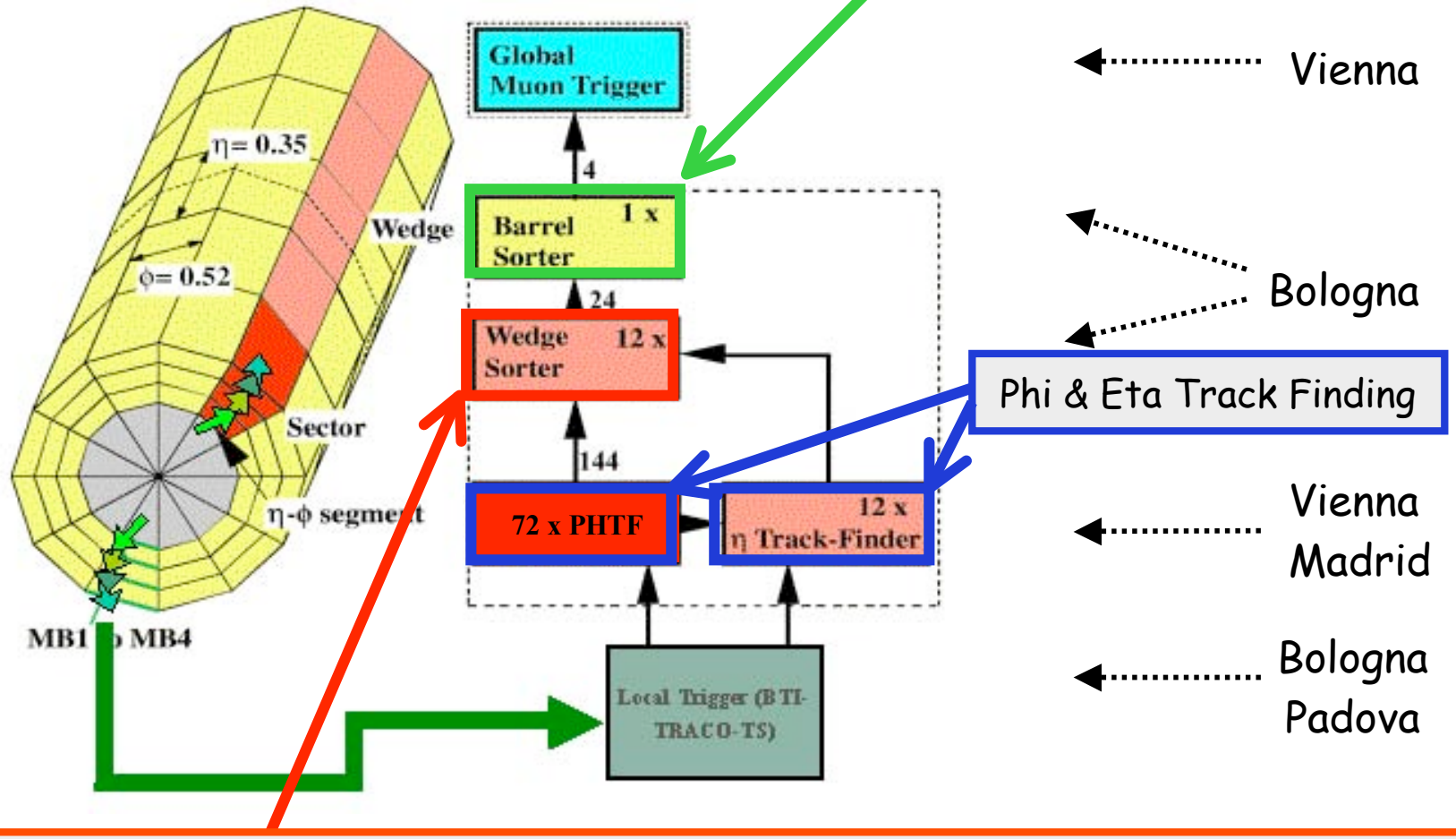
Sorter Board (Rice):

- 4 boards built in 2003, 3 boards assembled
  - Need only 1 in final system
- 2 mezzanines assembled
- Two MS boards w/mezzanines bench tested
- Tested with Sector Processor prototype
- Checked in the Track Finder crate during beam test at CERN in June 2004
- Does not require irradiation test



Drift Tube Track Finder & Sorter

1 BS sorts the "best" 4 tracks out of max 24 tracks from 12 WS of barrel

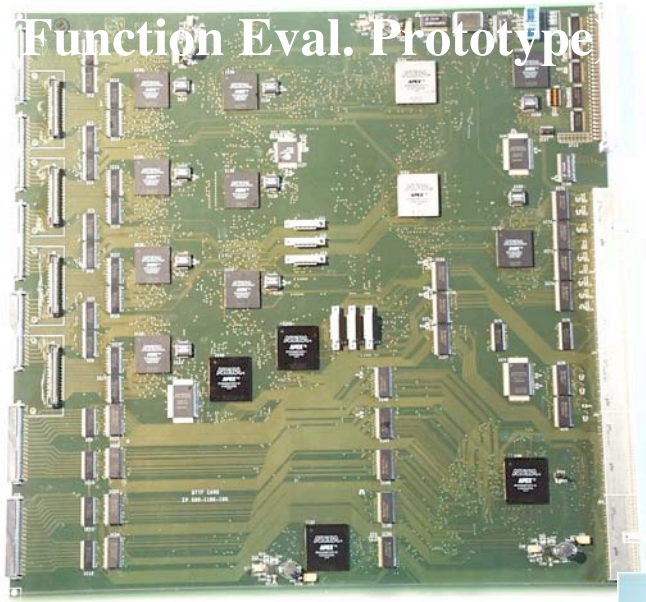


12 WS, each sorts the "best" 2 tracks out of max 12 tracks from 6 PHTF of a wedge

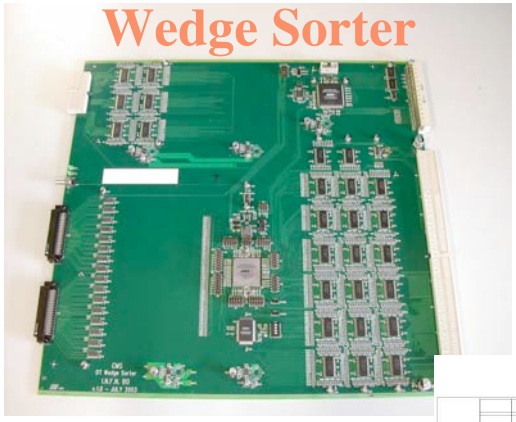
Drift Tube Track Finder Crate

Sector Processor (PHTF)

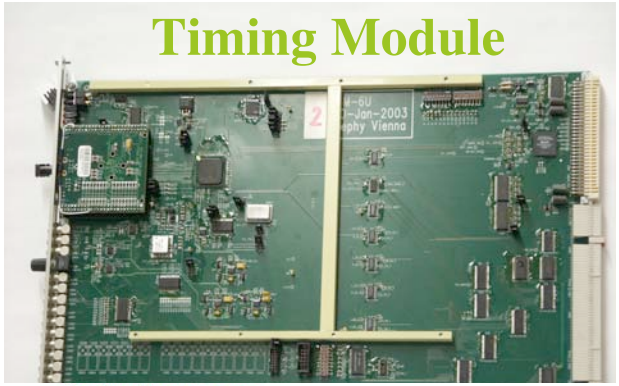
Function Eval. Prototype



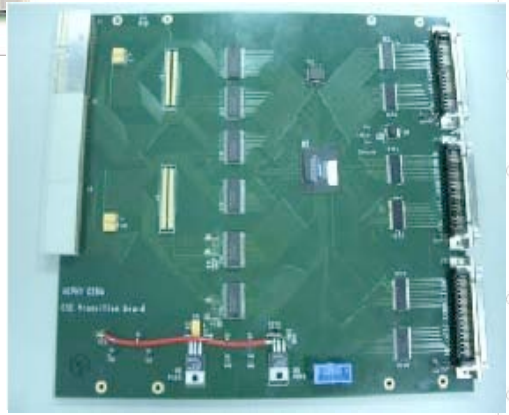
Wedge Sorter

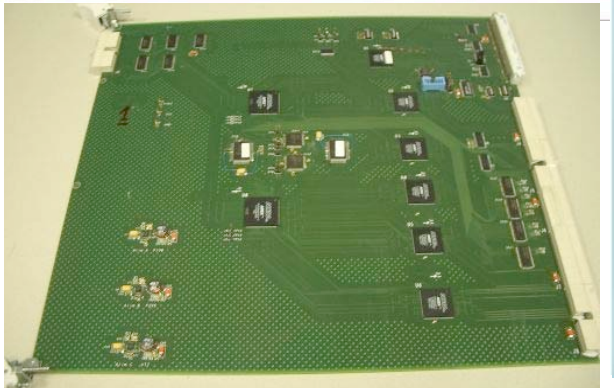


Timing Module



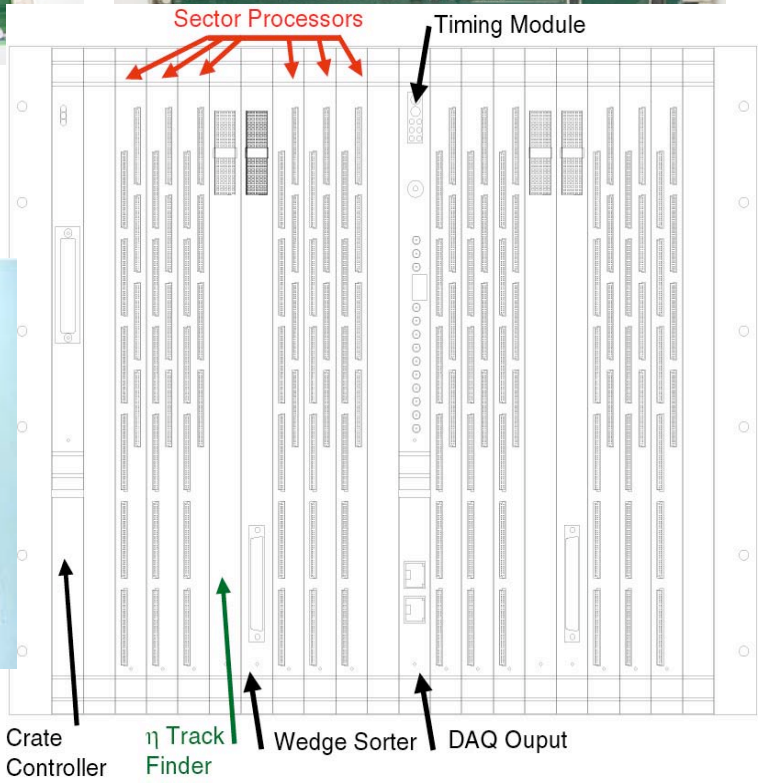
DT/CSC Transition Board





Eta Track Finder

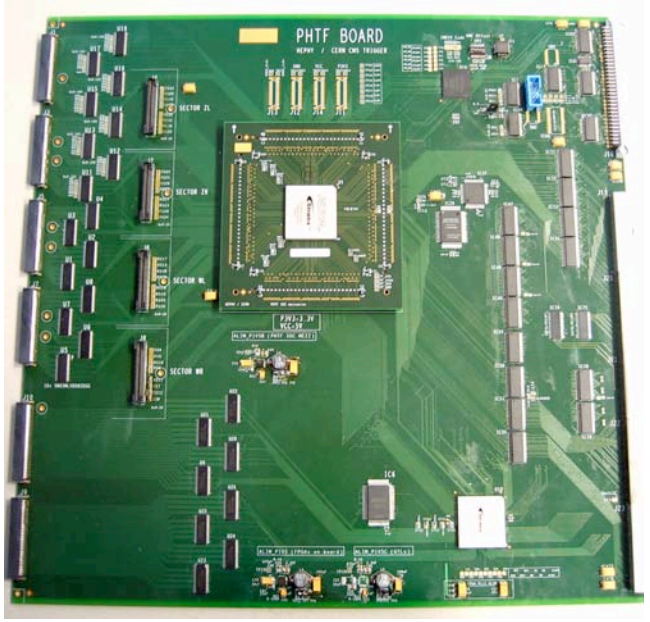
6 Crates:



Phi & Eta Track Finders
— Vienna & Madrid

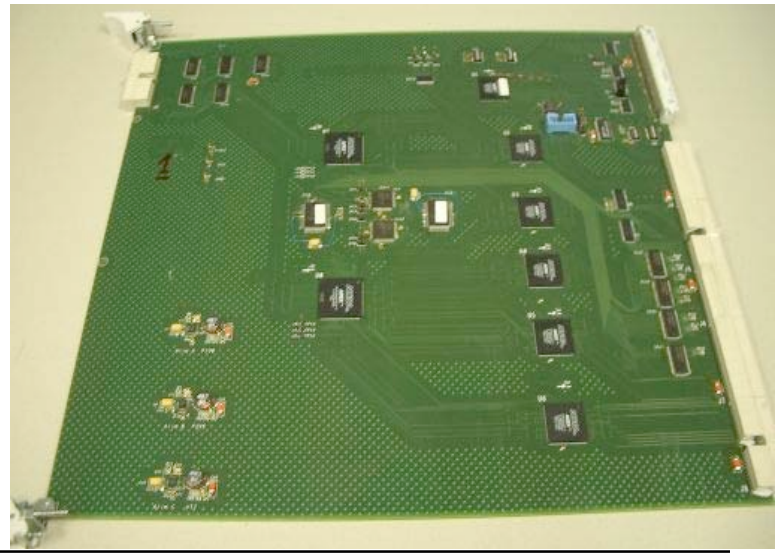
Phi Track Finder PPP:

- Sector processor:"System on Chip"
- Altera Stratix: 1020 pins on mezzanine
- JTAG chain & track-finding work
- Quality control protocol being developed
- Will test in Oct. test beam



Eta Track Finder PPP:

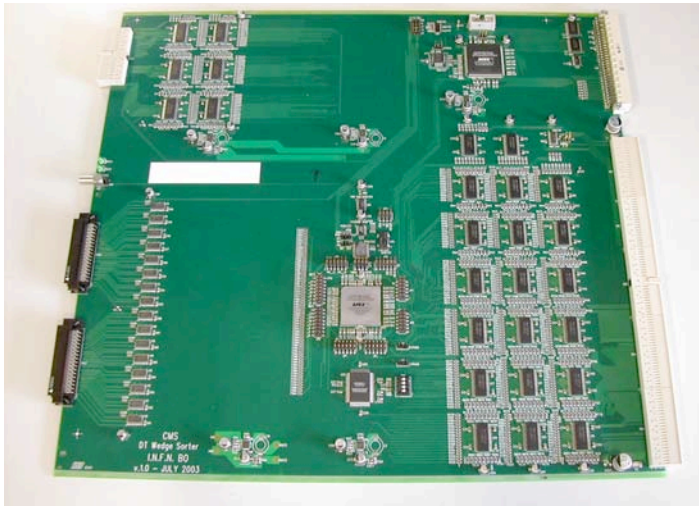
- VDHL model done and tested
- Agreement with ORCA is 100%.
- Tests were used to establish standard quality control protocol for Production
- 2 boards available
- Integration test with PHTF will follow



Drift Tube Wedge & Barrel Sorters
— Bologna

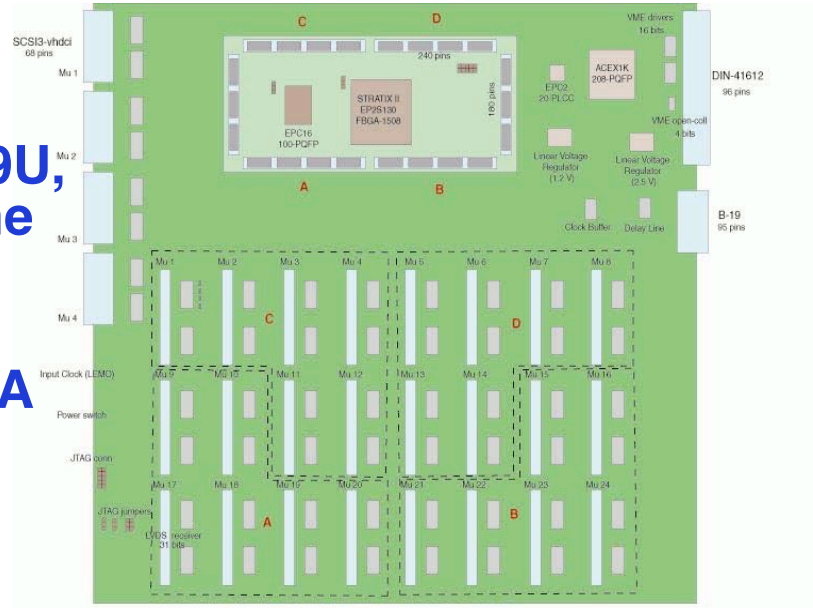
Wedge Sorter:

- Prototype fully tested @ 40 MHz standalone
- Combined static test done with old PHTF
- Combined test @ 40 MHz w/new PHTF now
- Will test in October test beam
- Tender for production done
- Production starts Oct 04, ends Dec 04 on schedule



Barrel Sorter:

- Electrical design for main board (VME 9U, with all connectors & transceivers) done
- Mezzanine design under way: ghost busting & sorting 4 out 24 in 3 BX is complex fits only in a big Stratix II FPGA (1508 pins)
- Prototype expected by end Nov 04



Barrel Sorter board layout (1:2) v7 - A.Montanari, 25-Aug-04

Global Muon Trigger Overview
— Vienna

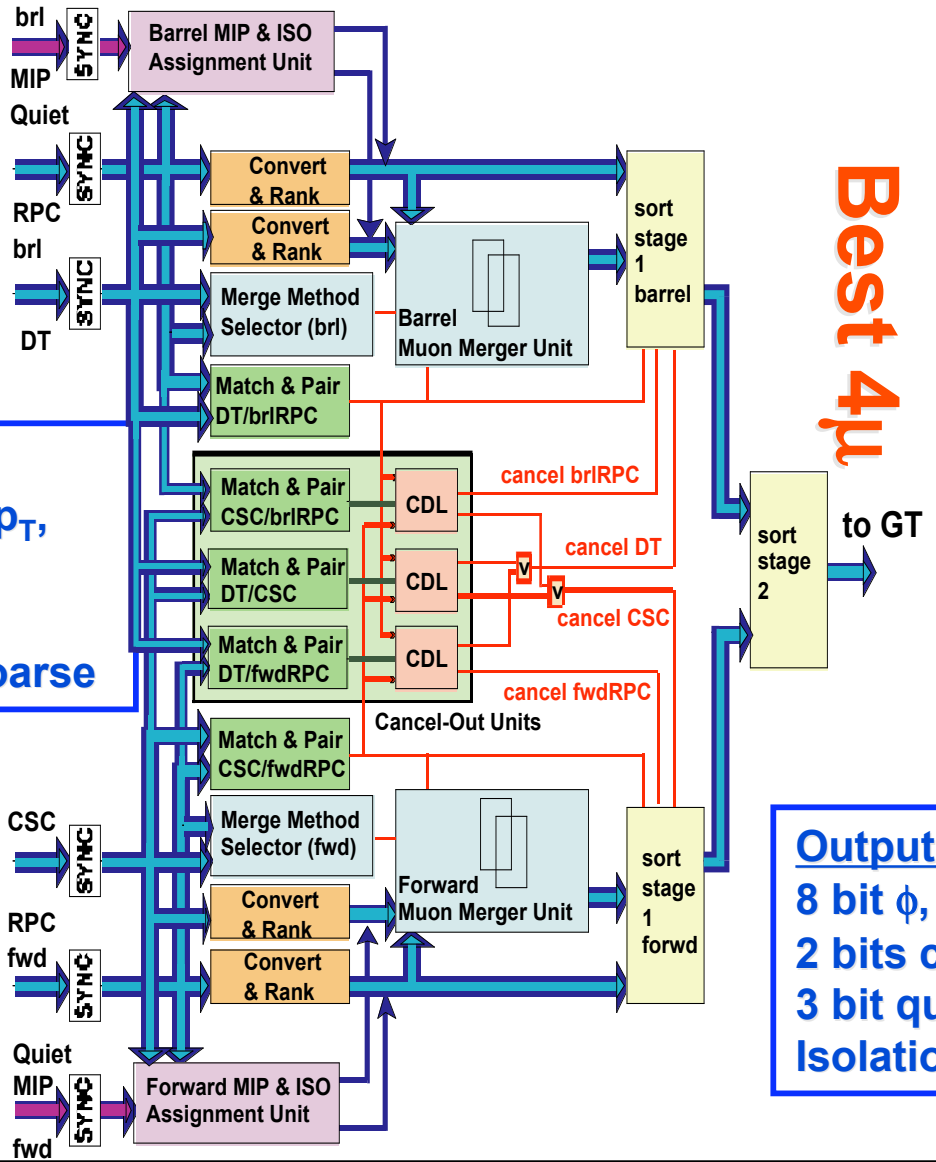
252 MIP bits
252 Quiet bits

4 μ RPC brl

4 μ DT

4 μCSC

4 μRPC fwd



Inputs:
8 bit ϕ, 6 bit η, 5 bit p_T,
2 bits charge,
3 bit quality,
1 bit halo/eta fine-coarse

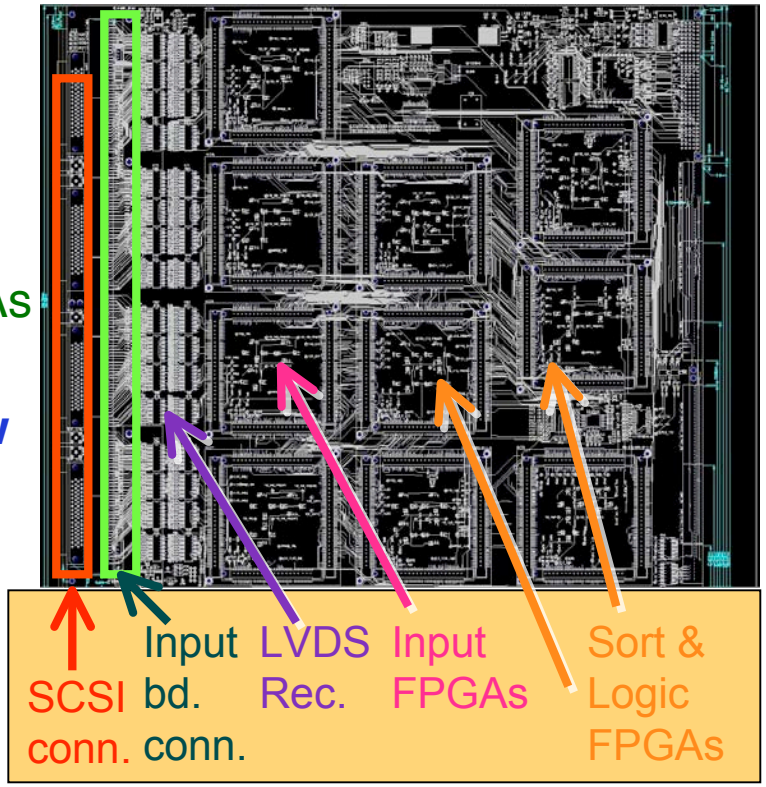
- Synchronization
- Matching & Pairing
  - DT & brlRPC
  - CSC & fwdRPC
- Merging of muon parameters
- Scale conversion (η)
- Detecting ghosts and fake triggers
- Canceling out duplicated candidates in overlap region
- Extrapolation to calorimeter for MIP/iso bit assign
- Ranking & Sorting

Output:
8 bit ϕ, 6 bit η, 5 bit p_T,
2 bits charge/synch,
3 bit quality, MIP bit,
Isolation bit

Global Muon Trigger Status
— Vienna

Logic Board

- **Mezzanine for FF896 package built & tested**
  - For Input FPGAs
- **Mezzanine for BF957 produced & under test**
  - For Logic, MIP/ISO Assignment, Sort FPGAs
- **Schematics complete**
- **Layout & routing complete, final checks now**
  - For both GMT Logic Board and Input Board
- **Production planned this month,**
  - Available Oct./Nov. 2004, tests until Dec. 04
  - Integration tests possible from Jan. 05



Firmware: 10 Xilinx Virtex II FPGAs

- **All chips completed (New: Sorter, Input FPGAs, Readout Processor)**
- **All verified against ORCA simulation. 100% agreement.**

Online Software

- **Developed generic JTAG Access Library (JAL) to program the flash PROMs via VME (common project with DT, GT)**

Boards in Global Trigger Crate
— Vienna

The Global Trigger Processor consists of the following electronics boards:

PSB (Pipelined Synchronizing Buffer)	Synchronization of inputs (7 modules)
GTL (Global Trigger Logic)	Global Trigger logic (1–2 modules)
GMT (Global Muon Trigger)	Global Muon Trigger logic (1 module, 4 slots wide)
FDL (Final Decision Logic)	Trigger decision (1 module)
TCS (Trigger Control System Module)	Central trigger control (1 module, 2 slots wide)
CONV6U (Conversion Boards)	Reception of fast signals
L1A (Level-1 Accept Module)	Distribution of trigger decision (2 modules)
TIM (Timing Board)	Timing (1 module)
GTFE (Global Trigger Frontend)	Readout (1 module)

GT Backplane & Pipeline Synchronizing Buffer (PSB9U)

— Vienna

Backplane:

- Transfer of signals GTL+ 80 MHz
- 4 needed: 1 for GT + 3 spares

Status & Tests:

- 6U prototype available
- 2 9U final backplanes tested
- 2 final GT crates delivered, 1 assembled

Pipelined Synchronizing Buffer:

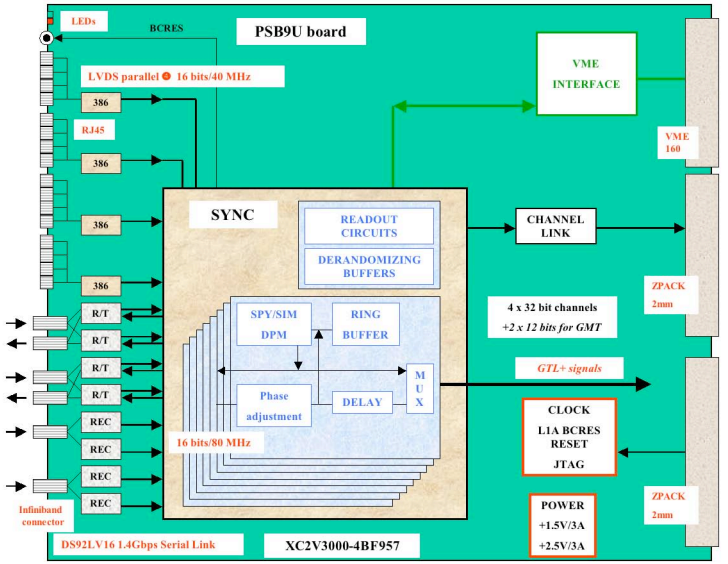
- Receive & synchronize inputs
- 15 needed: 4 for GT, + 3 for GMT + 8 spares

Status

- 6-channel 6U prototype PSB6U available
- No pre-production prototype foreseen
- Layout in progress
- All boards produced in one step by end 04
- Existing test PSB6U SW will be upgraded

Tests

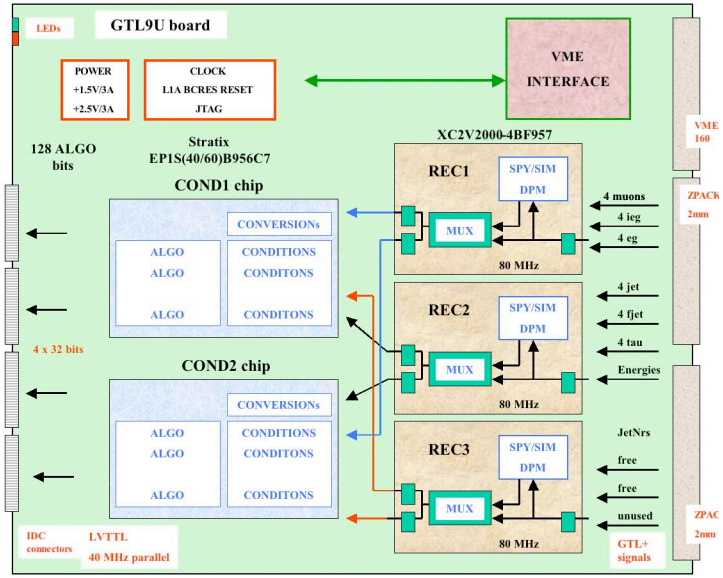
- PSB6U prototype is fully tested
- Successful integration test with GCT input module July 03



Global Trigger Logic & Final Decision Logic Boards – Vienna

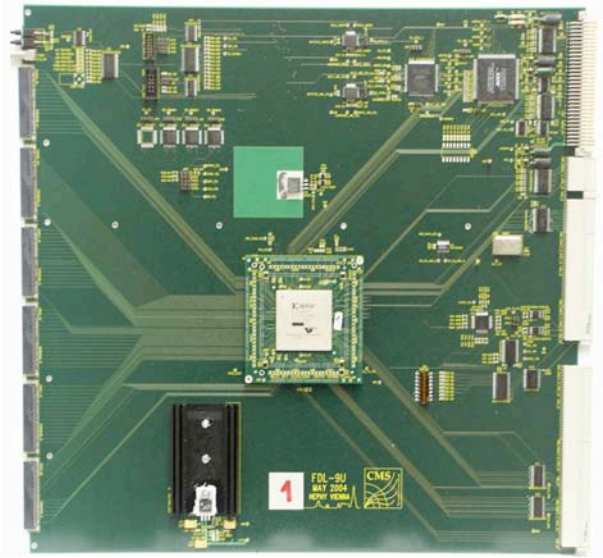
Global Trigger Logic Board

- 4 needed: 1 for GT + 3 spares
- 20-channel 6U prototype GTL6U tested
- GTL-CONV module for testing is available
- Schematic design almost finished
- Production Oct-Nov 04
- Software from GTL6U being upgraded



Final Decision Logic Board

- 4 needed: 1 for GT + 3 spares
- 1 assembled final board under test & MEZZ-957 incorporated
- 3 empty boards available
- Test software under development

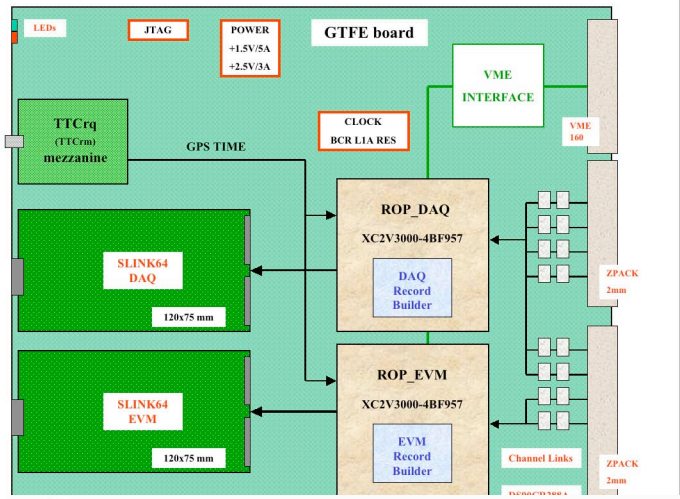


Global Trigger Frontend & Central Trigger Control Boards

— Vienna

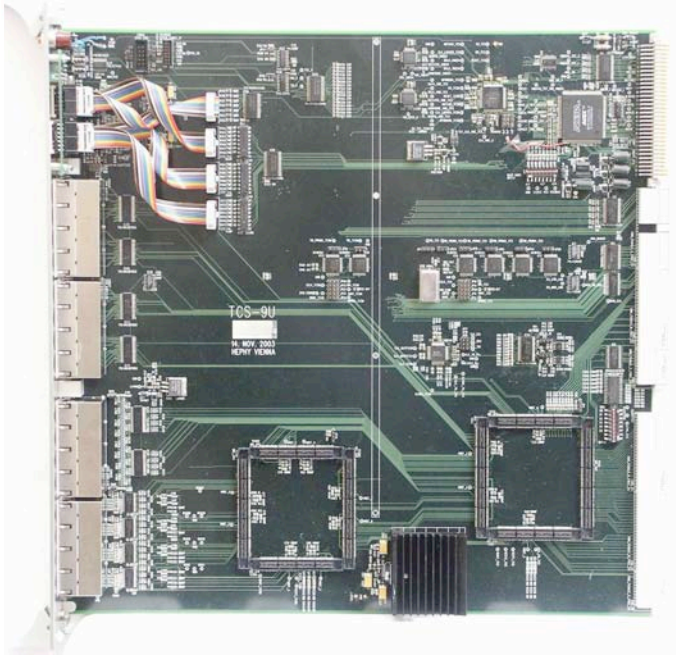
Front End Board (GTFE)

- Provides readout
- 4 needed: 1 for GT + 3 spares
- Schematic to be done
- Production: Jan – Feb 05



Final Decision Logic (FDL9U)

- All boards produced in one step
- 1 board under test,
- Have components for 2 more
- First version software for hardware tests exists



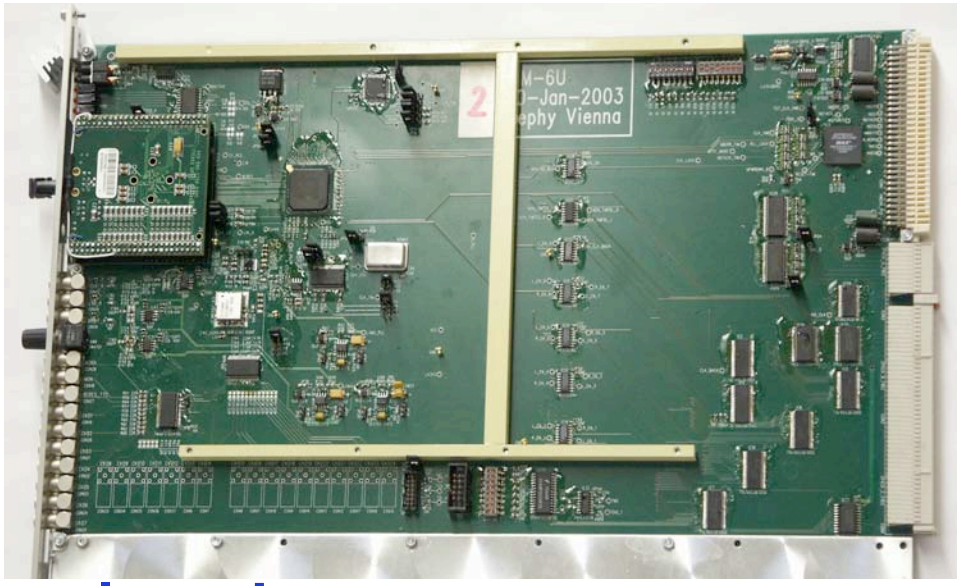
Global Trigger Timing Board – Vienna

13 Needed:

- 1 for GT+ 7 for DTTF + 5 spares

Status

- 2 preproduction boards tested & 1 under test
  - Use TTCrm
- New boards for TTCrq developed
- Old boards have same functionality as new ones
- New boards will be produced by Feb. 2005
- Final test software with GUI exists



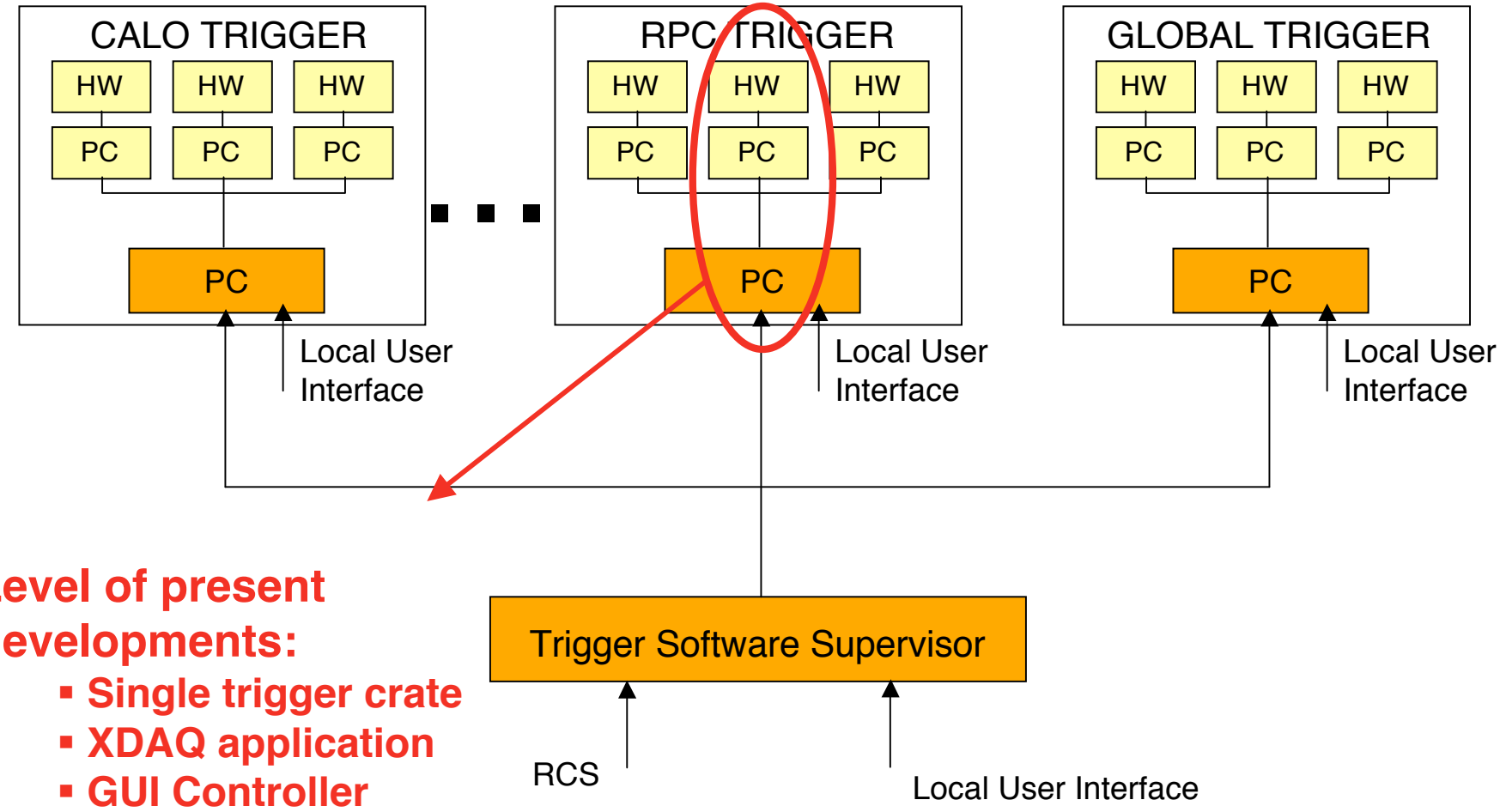
Trigger Module Database

Subsys.	Item	Explanation	Needed	Total	Responsible	Status	Prod. Start	Prod. Finish	Prod. Test Start	Prod. % Compl.	Prod. Test Finish	Prod. Test % Compl.	Ready for 904	Ready for USC55
CSC	CCB	CSC Clock & Control Board	1	3	Rice	PPP	Oct-04	Jan-05	Dec-04	0%	Mar-05	0%	Apr-05	Jun-05
CSC	CSC Bckpl	CSC Track - Finder Crate Backplane	1	3	U. Florida	PPP	Oct-04	Jan-05	Dec-04	0%	Mar-05	0%	Apr-05	Jun-05
CSC	MPC	CSC Muon Port Card	60	72	Rice	PPP	Oct-04	Jan-05	Dec-04	0%	Mar-05	0%	Apr-05	Jun-05
CSC	SR/SP	CSC Sector Processor/ Receiver	12	15	U. Florida	PPP	Oct-04	Jan-05	Dec-04	0%	Mar-05	0%	Apr-05	Jun-05
CSC	Sort	CSC Track-Finder Sorter	1	3	Rice	PPP	Jan-05	Feb-05	Feb-05	0%	Mar-05	0%	Apr-05	Jun-05
DT	DT Backplane	Drift Tube Track-Finder Crate Backplane	6	8	Vienna	PPP	Jan-05	Mar-05	Mar-05	0%	Apr-05	0%	Feb-05	Jun-05
DT	PHTF	Drift Tube Phi Track-Finder	72	90	Vienna	PPP-Aug-04	Jan-05	Mar-05	Mar-05	0%	Apr-05	0%	Feb-05	Jul-05
DT	ETTF	Drift Tube Eta Track-Finder	12	15	Vienna	PPP	Nov-04	Dec-04	Dec-04	0%	Feb-05	0%	Feb-05	Jun-05
DT	Optical Input	DTTF Gigabit Optical Receiver	96	110	Bologna	PPP-Nov-04	Apr-05	Aug-05	Apr-05	0%	Aug-05	0%	May-05	Sep-05
DT	WS	Drift Tube Wedge Sorter	12	15	Bologna	PPP-Nov-04	Dec-04	Jan-05	Dec-04	0%	Feb-05	0%	Feb-05	Mar-05
DT	BS	Drift Tube Barrel Sorter	1	3	Bologna	PPP-Nov-04	Jan-05	Feb-05	Jan-05	0%	Mar-05	0%	Mar-05	Apr-05
DT	TIM	Timing Module	7	10	Vienna	PPP	Jan-05	Feb-05	Feb-05	0%	Apr-05	0%	Feb-05	Jun-05
DT	Data-Link	DTTF Data Concentrator Interface	6	8	Vienna	PPP-Sep-04	Oct-04	Jul-04	Sep-04	0%	Feb-05	0%	Feb-05	Jun-05
DT	CSC Transition	Data-Link between DTTF & CSC TF systems	24	30	Vienna	PPP	Oct-04	Dec-04	Jan-05	0%	Feb-05	0%	Feb-05	Jun-05
DT	Data Concentrator	DTTF Data Collection, Compression, DAQ Link	1	3	Vienna	PPP-Oct-04	Feb-05	Aug-04	Sep-04	0%	Apr-05	0%	Feb-05	Jun-05
DT	Control Backplane	DTTF Control Crate Backplane	1	3	Vienna	-	Nov-04	Dec-04	Dec-04	0%	Dec-04	0%	Feb-05	Jun-05
GCT	IM	Input Module	18	22	Bristol	PPP	Dec-04	Jan-05	Feb-05	0%	Mar-05	0%	Apr-05	Apr-05
GCT	IM Backplane	Input Module Crate Backplane	2	4	Bristol	PPP	Dec-04	Jan-05	Feb-05	0%	Mar-05	0%	Apr-05	Apr-05
GCT	TPM	Trigger Processor Module	9	12	Bristol	PPP-Oct-04	Jul-05	Aug-05	Aug-05	0%	Dec-05	0%	Mar-05	Dec-05
GCT	TPM Backplane	Trigger Processor Module Crate Backplane	1	3	Bristol	PPP	Jul-05	Aug-05	Aug-05	0%	Dec-05	0%	Mar-05	Dec-05
GCT	CM	Communications Module	1	4	Bristol	PPP-Jul-04	Jul-05	Aug-05	Aug-05	0%	Dec-05	0%	Mar-05	Dec-05
GMT	TLB	Trigger Logic Board	1	4	Vienna	Design	Aug-04	Oct-04	Oct-04	0%	Nov-04	0%	Dec-04	Jun-05
GMT	PSB	Pipeline Synchronization Buffer Board	3	6	Vienna	Final	Sep-04	Nov-04	Nov-04	0%	Dec-04	0%	Dec-04	Jun-05
GT	Backplane	Global Trigger Backplane	1	3	Vienna	Final	Dec-03	Apr-04	May-04	100%	Jun-04	100%	Oct-04	Jun-05
GT	PSB	Pipeline Synchronization Buffer Board	4	9	Vienna	Final	Sep-04	Nov-04	Nov-04	0%	Dec-04	0%	Dec-04	Jun-05
GT	GTL6U	Global Trigger Logic Board	1	4	Vienna	Proto	Oct-02	Nov-03	Nov-03	100%	Apr-04	100%	Oct-04	Jun-05
GT	GTL	Global Trigger Logic Board	1	4	Vienna	Final	Dec-04	Feb-05	Feb-05	0%	Apr-05	0%	Jun-05	Aug-05
GT	FDL	Final Decision Logic Board	1	4	Vienna	Final	Jun-04	Sep-04	Sep-04	50%	Nov-04	0%	Nov-04	Jun-05
GT	GTFE	Global Trigger Front End - Readout	1	3	Vienna	Final	Feb-05	Mar-05	Mar-05	0%	Jun-05	0%	Jun-05	Aug-05
GT	TCS	Central Trigger Control System Board	1	3	Vienna	Final	Dec-03	Jun-04	Jun-04	100%	Oct-04	50%	Oct-04	Jun-05
GT	L1A	Level 1 Accept Output Module	2	5	Vienna	Final	Mar-04	Aug-04	Jul-04	80%	Oct-04	50%	Oct-04	Jun-05
GT	CONV	Fast Signal Converter Boards	4	10	Vienna	Final	Dec-03	Jun-04	Jul-04	25%	Oct-04	50%	Oct-04	Jun-05
GT	TIM_V1 (for TTCrm)	Timing Module	1	3	Vienna	PPP	Jan-03	Mar-03	Mar-03	100%	Jun-03	100%	Oct-04	Jun-05
GT	TIM_V2 (for TTCrq)	Timing Module	1	3	Vienna	Final	Jan-05	Mar-05	Apr-05	0%	May-05	0%	May-05	Jun-05
RCT	Bckpl	Regional Cal Trigger Backplane	18	25	Wisconsin	Exist	Jan-04	Jun-04	Jun-04	100%	Oct-04	12%	Dec-04	Jun-05
RCT	CCC	Clock and Control Card	18	25	Wisconsin	Exist	Jan-04	Jun-04	Jun-04	100%	Oct-04	20%	Dec-04	Jun-05
RCT	RC	Receiver Card	126	154	Wisconsin	Exist	Jan-04	Aug-04	Nov-04	100%	Oct-04	2%	Dec-04	Jun-05
RCT	RMC	Receiver Mezzanine Card	1026	1420	Wisconsin	Done	Sep-03	Oct-03	Oct-03	100%	Dec-03	100%	Dec-04	Jun-05
RCT	EIC	Electron Identification Card	126	154	Wisconsin	Done	Jan-04	Mar-04	Mar-04	100%	Oct-04	100%	Dec-04	Jun-05
RCT	JSC	Jet/Summary Card	18	25	Wisconsin	PPP	Aug-04	Sep-04	Oct-04	0%	Nov-04	0%	Dec-04	Jun-05
RCT	MCC	Master Clock Card	1	3	Wisconsin	Design	Jan-05	Feb-05	Feb-05	0%	Mar-05	0%	Mar-05	Jun-05
RPC	LB	Link Box (includes front & back planes)	108	124	Lapp./Wars.	PPP	Mar-04	Jun-04	Oct-04	0%	Jun-05	0%	May-05	May-05
RPC	MLB	Master Link Board	588	676	Lapp./Wars.	PPP	Mar-04	Jun-04	Oct-04	0%	Sep-04	0%	May-05	May-05
RPC	SLB	Slave Link Board	980	1127	Lapp./Wars.	PPP	Mar-04	Jun-04	Oct-04	0%	Sep-04	0%	May-05	May-05
RPC	CB	Control Board	216	248	Lapp./Wars.	PPP	Mar-04	Jun-04	Oct-04	0%	Sep-04	0%	May-05	May-05
RPC	LBbox RE11	Link Box RE11 (includes front & back planes)	12	14	Lapp./Wars.	PPP	Apr-04	Jun-04	Oct-04	0%	Dec-04	0%	UX	UX
RPC	MLB RE11	Master Link Board RE11	72	84	Lapp./Wars.	Proto	Mar-04	May-04	Mar-05	0%	Dec-05	0%	UX	UX
RPC	CB RE11	Control Board RE11	12	14	Lapp./Wars.	Proto	Mar-04	May-04	Mar-05	0%	Dec-05	0%	UX	UX
RPC	Splitter	Splitter Board	60	69	Lappeenranta	PPP	Aug-04	Sep-04	Nov-04	0%	Feb-05	0%	Apr-05	Jul-05
RPC	Trigger Backplane	Trigger Crate Backplane	12	14	Warsaw	PPP-Oct04	Jul-04	Sep-04	Jan-05	0%	Mar-05	0%	Apr-05	Jul-05
RPC	TB	Trigger Board	108	124	Warsaw	PPP	Jun-04	Sep-04	Jan-05	0%	Dec-05	0%	Apr-05	Jul-05
RPC	Sorter Backplane	Sorter Crate Backplane	1	3	Bari/Warsaw	Design	Nov-04	Mar-05	Apr-05	0%	May-05	0%	Jun-05	Jul-05
RPC	SB	Sorter Board	1	3	Bari	Design	Mar-05	May-05	Jun-05	0%	Dec-05	0%	Jul-05	Jul-05
RPC	Final Sorter Board	Ghost-Buster & Sorter Board	2	4	Bari	Design	Jun-04	May-05	Jun-05	0%	Dec-05	0%	Jul-05	Jul-05
RPC	DCC	Data Concentrator Card	3	5	Warsaw/ECAL	PPP	Jan-05	May-05	Jun-05	0%	Dec-05	0%	Jul-05	Jul-05
RPC	CCS	Clock and Control System	3	5	Warsaw/Tracker	PPP	Jan-05	May-05	Jun-05	0%	Dec-05	0%	Jul-05	Jul-05

Trigger Software Status

- Software for test of trigger boards was developed for all trigger sub-systems
- Most of the software is based on standard CMS tools (XDAQ, HAL, SOAP, I2O) and can be re-used later in the experiment
- Configuration, Operation, Monitoring and Testing functions are becoming available
- Software teams for all trigger sub-systems are now in place
- Focusing on Coordination — J. Varela, Lisbon

Trigger Software Structure



Level of present developments:

- **Single trigger crate**
- **XDAQ application**
- **GUI Controller**

Trigger Software Functions

Configuration

- Hardware configuration
- Parameter settings
- Data base access
- Resources allocation

Test & Diagnostics

- Boundary scan tests
- Functional tests
- Interconnection tests
- Diagnosis user help

Resource Management

- User interface to data base
- Hardware management
- Firmware management
- Software management
- Configuration management

Operation

- State management
- Hardware initialization
- Start/stop/pause/resume
- Read spying events

Reporting

- Hardware status
- Alarms
- Statistics

Monitoring

- Analysis of spy events
- Histograming, visualization

Administration

- User registration
- Access permissions

Trigger Software Working Group

New composition:

Sub-System	People
Chair	Joao Varela
TS	Ildefons Magrans
GMT	Hannes Sakulin
CSC	Darin Acosta
RPC	Michal Pietrusinki
DTTF	Jorge Troconiz
DT	
GCT	Jim Brooke
RCT	Monika Grothe
ECAL	Nuno Almeida
HCAL	Jeremy Mans
GT	Joscko Strauss
TTC	Emlyn Corrin

Trigger SW Development Plan

Consolidate sub-systems software teams & present work:

- Document what exists
- Promote use of common technologies
  - XDAQ, HAL, SOAP, I2O, DSTORE

Consolidate hardware related layer:

- Hardware management in Equipment Database
  - Board description, identification & history
- Agree on scheme for storage and verification of Firmware and LUT contents

Configuration data

- Use CMS Configuration DB Infrastructure (need this)
- Sub-systems define their Configuration Data Schema

Trigger supervision

- Define requirements and architecture → Documentation
- Integrate with RCS and trigger sub-systems

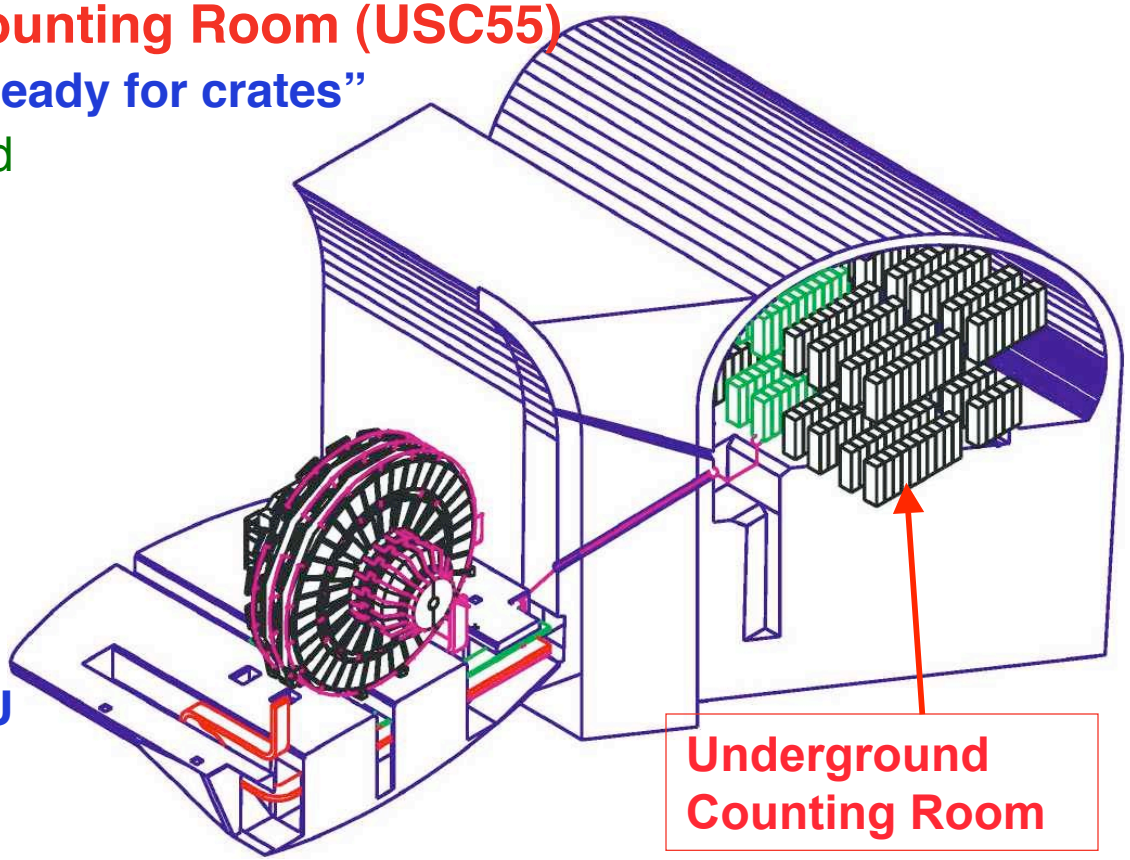
Trigger testing and monitoring

- Translate Integration Test Plans into Software → Bldg 904 setup
- Trigger Online Monitoring → Use DAQ Monitoring Infrastructure
- Test & run trigger emulation

Trigger Installation Startup

Installation in Underground Counting Room (USC55)

- **Expect start by Nov 30 '05 —"ready for crates"**
  - Racks & Infrastructure installed
  - Date was June '05 in CR03
- **Sufficient time for installation & some testing but not for complete commissioning with detectors**
  - Significant time needed for integration in synchronous pipelined system



Surface tests in SX5

- **Soon with both HCAL and EMU**
- **More during magnet test**
- **Verify trigger functions & interfaces w/detectors on surface.**

Tests in Electronics Integration Center

- **Labs and row of racks for all electronics subsystems**
- **Test interfaces & integration as much as possible before move to USC55**
- **Prevessin 904 (next slides)**

USC55 central core racks

see: http://cmsdoc.cern.ch/~wsmith/USC55_racks.html

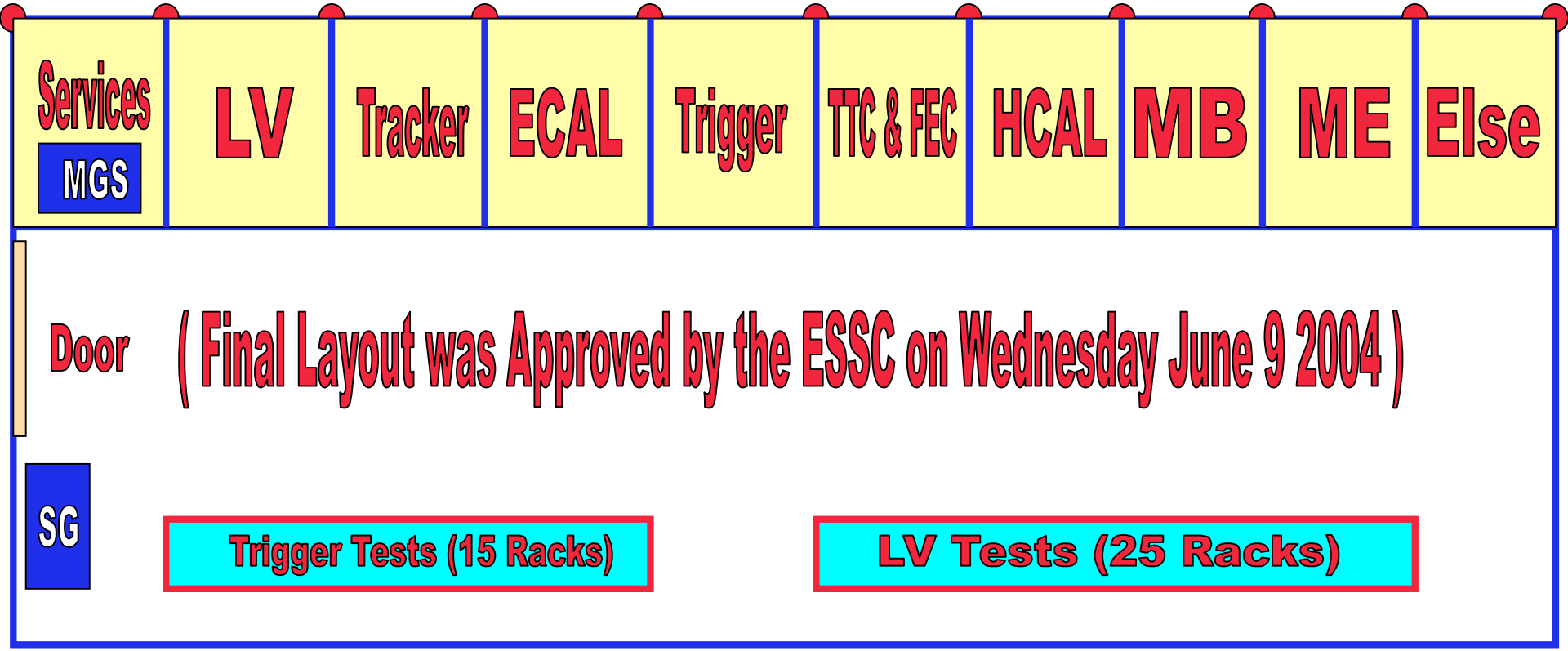
Upper Floor (Zone S2)

+Z	A	B	C	D	E	F	G	-Z H
01	--	--	--	ECAL spare	Cal Reg Trig	HCAL HTR	--	--
02	TOTEM	TOTEM	DAQ	ECAL ULR	Cal Reg Trig	HCAL HTR	DAQ	x
03	TOTEM	TOTEM	HCAL Calib	ECAL ULR	Cal Reg Trig	HCAL HTR	EBE DCS	x
04	TOTEM	TOTEM	HCAL Calib	ECAL ULR	Cal Reg Trig	HCAL HTR	EBE DCS	x
05	TOTEM	DAQ	HCAL Calib	ECAL SRP/TTC	%Cal Reg Trig	%HCAL HTR	Presh. DCS	x
06	ASSM	EB HV	HCAL DCS	ECAL ULR	Cal Reg Trig	HCAL HTR	EB HV	x
07	ASSM	EB HV	HCAL DCS	ECAL ULR	Cal Reg Trig	HCAL HTR	EB HV	x
*08	ASSM	EB HV	HCAL SrcDrv	ECAL ULR	Cal Reg Trig	HCAL HTR	EB HV	x
*09	ASSM	EE HV	HPD HV	DAQ	Cal Reg Trig	DAQ	EE HV	x
10	ASSM	Presh. LV/HV	HPD HV	Presh. FED	Cal Reg Trig	x	Presh. LV/HV	x
11	ASSM	Presh. LV/HV	HPD HV	Presh. FED	TOTEM Trig	EBE Lt Mn	Presh. LV/HV	F.D.
12	ASSM	Presh. LV/HV	HPD HV	DAQ	CASTOR Trig	EBE Lt Mn	Presh. LV/HV	F.D.
13	ASSM	Presh. Misc	HPD HV	ECAL Cool	x	EBE Lt Mn	EB LV	F.D.
14	ASSM	x	PMT HV	ECAL Cool	Align PCs	EBE Laser	EE LV	F.D.
15	ASSM	DSS	DSS	DSS	Align Laser	DSS	DSS	F.D.

Lower Floor (Zone S1)

+Z	A	B	C	D	E	F	G	-Z H
00	--	--	--	Presh. FEC	TK. FEC	TK. FEC	DT/RO/SC	--
01	--	--	--	DT TrkFnd	Opt.Cpl.	RPC Trig	Pixel FEC	--
02	TK. Ctrl	DAQ	DAQ	DT TrkFnd	TTC	RPC Trig	Pixel Ctrl	RPC B HV
03	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	DT TrkFnd	TTC	RPC Trig	Pixel FED	RPC B HV
04	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	CSC TrkFnd	Global	RPC Trig	Pixel FED	RPC B HV
05	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	CSC TrkFnd	%Cal Global	%RPC Trig	DAQ	RPC B HV
06	CSC HV	DAQ	DAQ	DAQ	TTS	RPC Trig	CSC FED	RPC B HV
07	CSC HV	FED PCs	DAQ	DT HV	TTS	RPC Trig	CSC FED	RPC B HV
*08	CSC HV	DAQ	DAQ#	DT HV	BPTX	RPC Trig#	CSC FED	RPC E+ HV#
*09	CSC HV	TK. FED TEC-	TK. FED TEC+#	DT HV	LHC	DAQ#	ME1/1 HV	RPC E+ HV
10	CSC HV	TK. FED TEC-	TK. FED TEC+	DT HV	BPM	DSS	ME1/1 HV	RPC E- HV
11	DAQ	TK. FED TEC-	TK. FED TEC+	DT HV	DSS	DSS	DSS	RPC E- HV

Approved Plan for B 904



Plans for the CMS Electronics Integration Centre at Prevessin (B 904)

Insuring Successful Installation

Trigger Component Interfaces

- Each interface specified by a CMS Internal Note signed by all parties to the individual interface
- Integration tests planned or already done for each interface before equipment bought to Point 5

Structured Beam Tests:

- Operation of trigger systems with detectors in 25 ns beam checks synchronization and phase offsets

Tests in Electronics Integration Center (B 904)

- Simulate conditions in USC55 as closely as possible

Surface test in SX5:

- Trigger components will participate in the surface tests & magnet tests in SX5 as permitted by front end electronics and detector availability

USC55 Trigger Install Schedule – I

Install/Commission Trig. Crates Dec '05 – Apr '06

- Tested Trigger Crates installed, re-tested, interconnected, inter-synchronized
- Regional and Global Detector trigger systems integrated with each other and Global Trigger

Integrate w/Detector Electronics May '06 – Oct '06

- Cal Trig connected to E/HCAL USC55 electronics
- Muon Triggers connected to optical fibers carrying trigger data from detector
- Global Trigger connected to TTC distribution system
- Operation with Local DAQ

USC55 Trigger Install Schedule – II

Integrate w/Central Trig. & DAQ Nov '06 – Apr '07

- Subset of triggers available to detectors in UXC55
- Dedicated testing with individual detectors
- Detailed synchronization testing of all systems
- Testing with Central DAQ

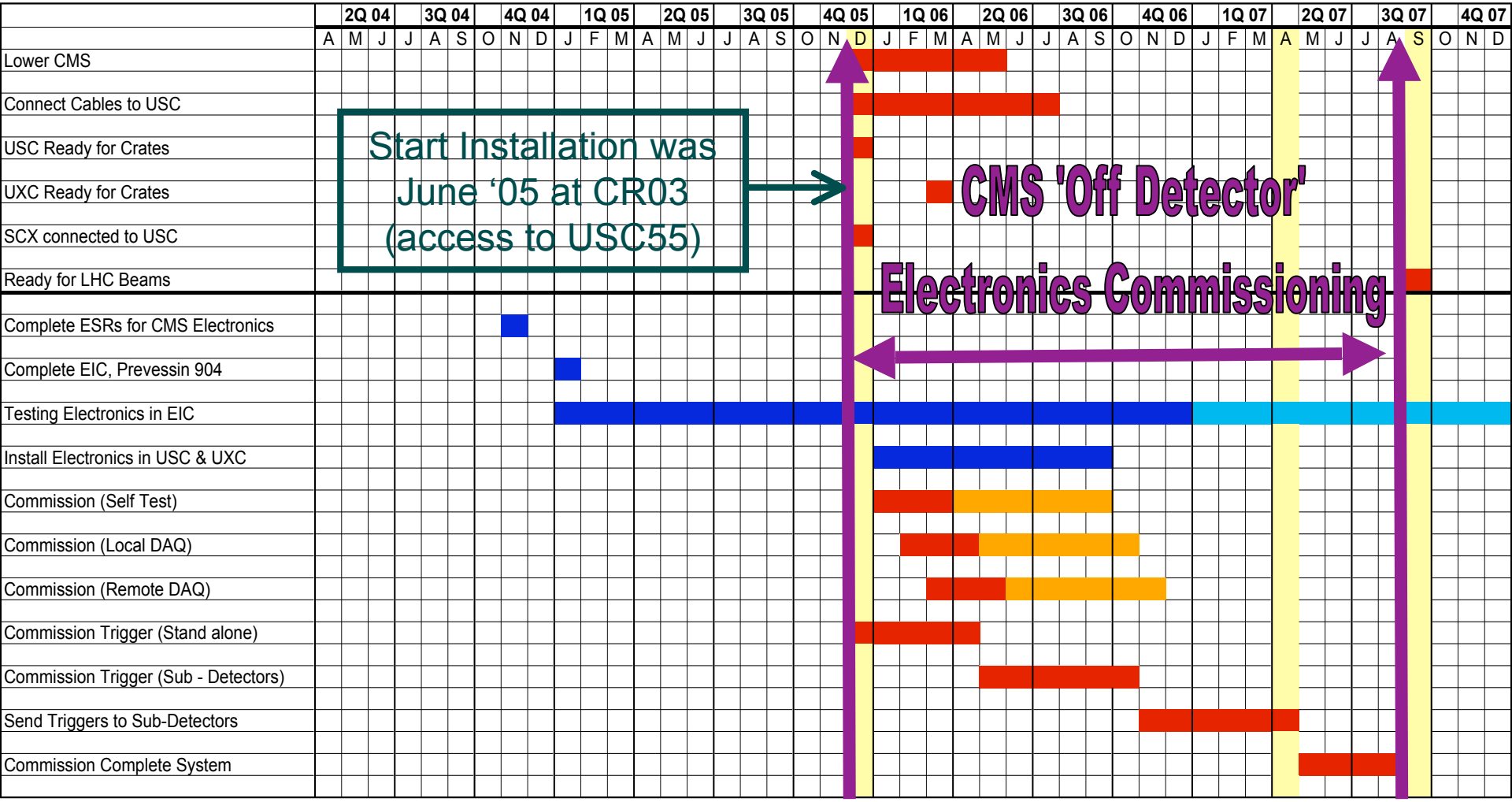
System Commissioning May '07 – Aug '07

- Full capability of trigger system available
- Tests with all detectors and trigger operating simultaneously together and partitioned
  - Trigger and DAQ can operate in 8 separate partitions

Ready for Data Taking August, 2007

CMS Electronics Installation Plans Consistent with Trigger Plans

4 month slip wrt. schedule shown at CR03



Trigger Conclusions

Good Progress on all fronts:

- Prototyping concluding & production starting or underway
- Integration tests complete or underway
- Software being developed
- Passed Trigger Electronics System Review May '04

Installation:

- Time is tight to accomplish the necessary tasks
- Steps taken, planning established to meet schedule
  - Interfaces: Documents, Integration Tests
  - Tests: Structured Beam, Surface Tests in SX5
  - Use of Electronics Integration Center in Prevessin 904
  - Careful layout and plan for USC55
  - Flexible system partitioning allows work in parallel