SLHC Electronics Upgrades

US CMS Meeting

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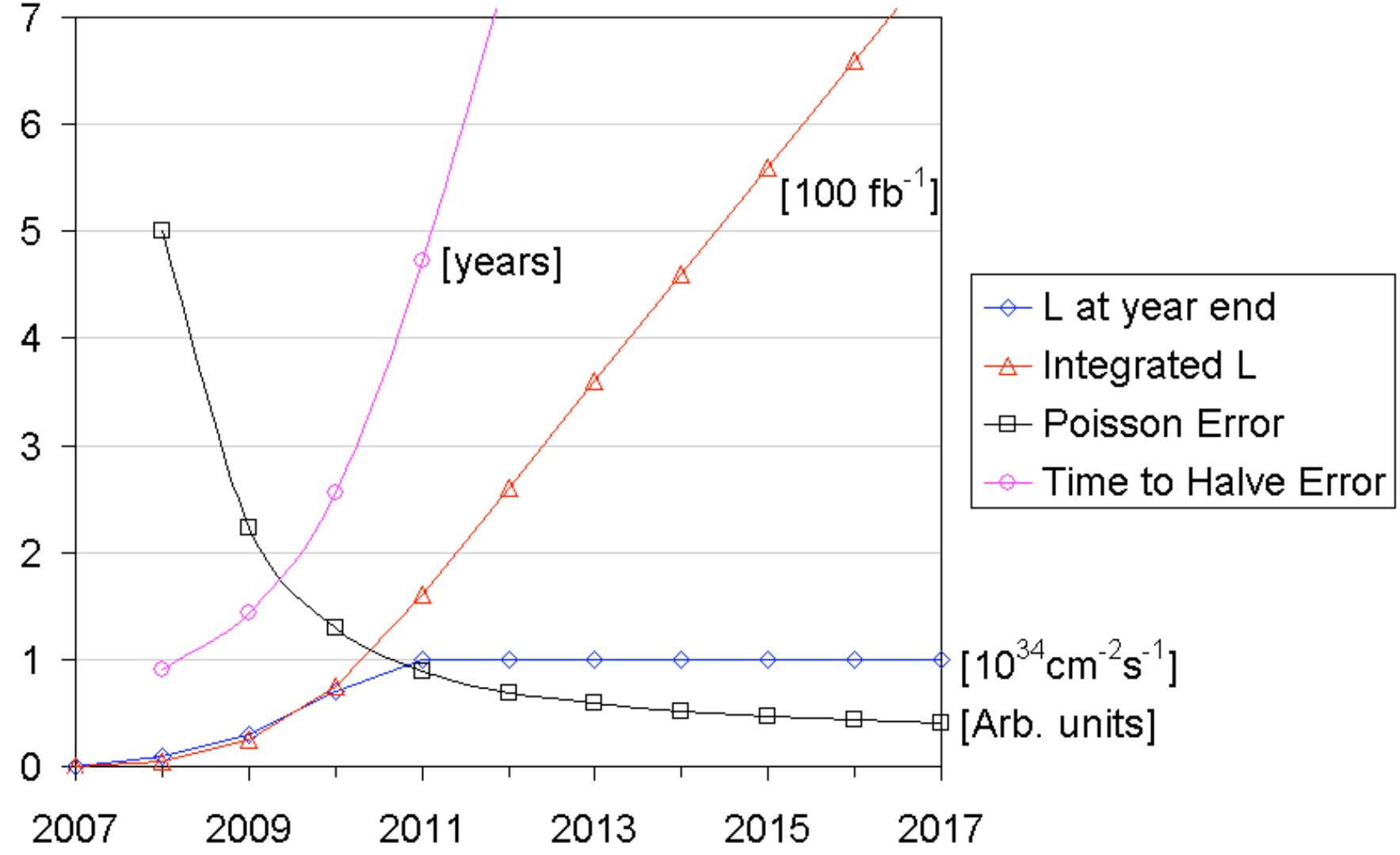
Outline:

- Schedule for Upgrades
- Impact of 10^{35} Luminosity & 12.5 ns Bunch Crossing interval
- Trigger Requirements & Menu
- Tracking electronics & trigger
- Muon & Calorimeter electronics & triggers
- Architecture & Latency
- DAQ upgrade

This talk is available on:
http://www.hep.wisc.edu/wsmith/cms/smith_SLHC_USCMS_May04.ppt

Schedule for Upgrades



CMS SLHC Planning

Input to this presentation:

- US CMS Trigger Workshop in Madison Feb 13:
- CMS Workshop at CERN Feb 26, 27

CMS Electronics Upgrade Workshop

- Imperial College, London
  - Mon, July 12 14:00 - Tues. July 13 17:00.
- Develop proposals for R&D to be presented to CMS MB
- Develop overall CMS plan for Electronics R&D
  - Not detailed, just timescales for development & reporting

Long Term:

- R&D 2005-7
- Prototype/Test 2008-10
- Construct/Install 2010-13

SLHC Trigger @ 10^{35}

Occupancy

- **Degraded performance of algorithms**
  - Electrons: reduced rejection at fixed efficiency from isolation
  - Muons: increased background rates from accidental coincidences
- **Larger event size to be read out**
  - Reduces the max level-1 rate for fixed bandwidth readout.

Trigger Rates

- **Attempt to hold max level-1 at 100 kHz by increasing readout bandwidth**
- **Implies raising E_T thresholds on electrons, photons, muons, jets and use of less inclusive triggers**
  - Need to compensate for larger interaction rate & degradation in algorithm performance due to occupancy

Radiation damage

- **Increases for part of level-1 trigger located on detector**

SLHC Trigger @ 12.5 ns

Choice of 80 MHz

- Reduce pile-up
- Be prepared for LHC Machine group electron-cloud solution
- Retain ability to time-in experiment
  - Beam structure vital to time alignment
- Higher frequencies ~ continuous beam

Rebuild level-1 processors to work with data sampled at 80 MHz

- Already CMS has internal processing up to 160 MHz and higher in a few cases
- Use 40 MHz sampled front-end data to produce trigger primitives with 12.5 ns resolution
- Save some latency by running all trigger systems at 80 MHz I/O

SLHC Trigger Requirements

High-P_T discovery physics

- Not a big rate problem since high thresholds

Completion of LHC physics program

- Example: precise measurements of Higgs sector
- Require low thresholds on leptons/photons/jets
  - Use more exclusive triggers since final states will be known

Control & Calibration triggers

- W, Z, Top events
- Low threshold but prescaled

SLHC Level-1 Trigger Menu

ATLAS/CMS Studies in hep-ph/0204087:

- **inclusive single muon p_T > 30 GeV (rate ~ 25 kHz)**
- **inclusive isolated e/γ E_T > 55 GeV (rate ~ 20 kHz)**
- **isolated e/γ pair E_T > 30 GeV (rate ~ 5 kHz)**
  - or 2 different thresholds (i.e. 45 & 25 GeV)
- **muon pair p_T > 20 GeV (rate ~ few kHz?)**
- **jet E_T > 150 GeV.AND.E_T(miss) > 80 GeV (rate ~ 1-2 kHz)**
- **inclusive jet trigger E_T > 350 GeV (rate ~ 1 kHz)**
- **inclusive E_T(miss) > 150 GeV (rate ~1 kHz);**
- **multi-jet trigger with thresholds determined by the affordable rate**

Calorimeter Electronics

HF: Possibly replaced

- **Very fast - gives good BX ID**
- **Modify logic to provide finer-grain information**
  - Improves forward jet-tagging

HCAL: Barrel stays but endcap replaced

- **Has sufficient time resolution to provide energy in correct 12.5 ns BX with 40 MHz sampling. HTR cards may be able to produce 80 MHz already.**

ECAL: Stays

- **Also has sufficient time resolution to provide energy in correct 12.5 ns BX with 40 MHz sampling, may be able to produce 80 MHz output already.**
- **Exclude on-detector electronics modifications for now -- difficult:**
  - Regroup crystals to reduce $\Delta\eta$ tower size -- minor improvement
  - Additional fine-grain analysis of individual crystal data -- minor improvement

Conclusions:

- **Front end logic same except where detector changes**
- **Need new TPG logic to produce 80 MHz information**
- **Need higher speed links for inputs to Cal Regional Trigger**

CSC Electronics

A. Korytov & D. Acosta, U. Florida

Bunch Crossing ID at 12.5 ns:

- **Use second arriving segment to define track BX**
  - Use a 3 BX window
- **Improve BX ID efficiency to 95% with centered peak, taking 2nd LCT, requiring 3 or more stations**
  - Requires 4 stations so can require 3 stations at L1
- **Investigate improving CSC performance: HV, Gas, …**
  - If 5 ns resolution ⇒ 4 ns, BX ID efficiency might climb to 98%

Occupancy at 80 MHz: Local Charged Tracks

- **Entire system: 4.5 LCTs /BX**
- **Worst case: ME1: 0.125/BX (ME2-4 3X smaller)**
- **P(≥ 2) = 0.7% (spoils di-μ measurement in 1 MPC)**
- **Conclude: not huge, but neglected neutrons and ghosts may be under-estimated⇒ need to upgrade trigger front end to transmit LCT @ 80 MHz**

Occupancy in Track-Finder at 80 MHz:

- **Using 4 BX window, find 0.5/50 ns in ME1 (every other BX!)**
  - ME2-4 3X smaller, possibly only need 3 BX
- **Need studies to see if these tracks generate triggers**

DT & RPC Electronics

DT:

- Operates at 40 MHz
- Could produce results for 80 MHz with loss of efficiency…or…
- Could produce large rate of lower quality hits for 80 MHz for combination with a tracking trigger with no loss of efficiency

RPC:

- Operates at 40 MHz
- Can produce results with 12.5 ns window with some loss of efficiency with planned FE to LB cable…or..
- Can produce results with 12.5 ns window with less or no loss in efficiency (tbd) if use skew-clear for FE to LB

Tracking Electronics - I

G. Hall & R. Horisberger

Pixel and Tracker Upgrades

- **8 cms – 15 cms Pixels 1 100 μ * 150 μ**
  - Present System at 8, 11, 14 cms
- **15 cms – 25 cms Pixels 2 160 μ * 650μ**
  - at 18, 22 cms
- **25 cms – 50 cms Pixels 3 200 μ * 5000 μ**
  - at 30, 40, 50 cms
- **50 cms - Silicon Strips**
  - Rationalize Module Types

R&D Issue:

- **Tracker interface to Calorimeters & μ Systems**

Tracking Electronics - II

Tracker upgrade will require DSM Electronics

- Will need to Characterize the 130 nm Processes
- Will need to Characterize < 130 nm Processes
  - Propose 65 nm

Plan:

- Continue to Develop Relationship with DSM Vendors and obtain access to Design Tools to continue to optimize the use of DSM

Cost :

- Must get design right in < 2 Iterations
- Must use > 100,000 chips / Design
- Then Cost / Chip is no worse than 250 nm

Power Consumption may be critical issue, Plan:

- Study the whole Power Management System, learn from commercial developments, transmit Power at higher voltage & Convert / Regulate locally, Review Cooling Technologies, Reduce Tracker Mass

SLHC L-1 Tracking Trigger

Additional Component at Level-1

- **Actually, CMS already has a L-1 Tracking Trigger**
  - Pixel z-vertex in $\Delta\eta \times \Delta\phi$ bins can reject jets from pile-up
- **Could use on-detector wire-/fiber-less interconnects?**
  - Line of sight VCSELS? - reduce cable material
- **Provides outer stub and inner track**
  - Combine with cal at L-1 to reject π^0 electron candidates
  - Reject jets from other crossings by z-vertex
  - Reduce accidentals and wrong crossings in muon system
  - Provide sharp P_T threshold in muon trigger at high P_T
- **Cal & Muon L-1 must produce output with suitable granularity to combine with L-1 tracking trigger**
  - Also need to produce hardware to make combinations

Move some HLT algorithms into Level-1

Use of L1 Tracking Trigger

- D. Acosta, U. Florida

Combine with L1 CSC as is now done at HLT:

- **Attach tracker hits to improve P_T assignment precision from 15% standalone muon measurement to 1.5% with the tracker**
  - Improves sign determination & provides vertex constraints
- **Find pixel tracks within cone around muon track and compute sum P_T as an isolation criterion**
  - Less sensitive to pile-up than calorimetric information *if* primary vertex of hard-scattering can be determined (~100 vertices total at SLHC!)

To do this requires η–ϕ information on muons finer than the current 0.05–2.5°

- **No problem, since both are already available at 0.0125 and 0.015°**

SLHC Calorimeter Trigger

Electrons/Photons:

- Report on finer scale to match to tracks

τ-jets:

- Cluster in 2x2 trigger towers with 2x2 window sliding by 1x1 with additional isolation logic

Jets:

- Provide options for 6x6, 8x8, 10x10, 12x12 trigger tower jets, sliding in 1x1 or 2x2

Missing Energy:

- Finer grain geometric lookup & improved resolution in sums

Output:

- On finer-grain scale to match tracking trigger
  - Particularly helpful for electron trigger

Reasonable extension of existing system

- Assuming R&D program starts soon

SLHC Trigger Architecture

LHC:

- Regional to Global Component to Global

SLHC Proposal:

- Combine Level-1 Trigger data between tracking, calorimeter and muon at Regional Level at finer granularity
- Forward physics objects made from tracking, calorimeter and muon regional trigger data to the global trigger
- Implication: performing some of tracking, isolation and other regional trigger functions in combination between regional triggers
  - New “Regional” cross-detector trigger crates

Data Link Architecture

Synchronous or Asynchronous?

- **Do we keep all links running synchronously at 80 MHz or do we allow arbitrary link frequencies as high as available and put FIFOs for resynchronization at input and output**
- **Advantage: use the latest link and low jitter crystal clocking technology**
- **Disadvantage: requires extra synchronization circuitry**
  - Latency for synchronization
  - Need to keep bunch crossing number with data, check it and report/correct errors
  - Extra circuitry and failure points

Clocking

TTC System:

- **Modification?**
- **Use as is and generate higher frequency clocks locally?**
  - What frequencies are needed?
- **Replace with 80 MHz system more able to drive next generation of links?**
  - Build in very good peak-to-peak jitter performance
- **Do we need to be able to transmit additional data with the Level-1 accept?**
  - Trigger type: special immediate readout handling?
  - Even more…event building…DAQ upgrade ⇒

Technologies for SLHC Trig.

Complicated Algorithms & Low Latency:

- FPGA's: faster, more logic
- Faster and larger memories

Moving more data at higher speed:

- Link technology: speed & integration
- Backplane technology: connectors & newer interconnect technology

Higher Crossing Frequency:

- High speed clocking: low jitter - design for links

Overall Complexity:

- Design for test, diagnostics, algorithm validation

Level-1 Latency

Present Latency of 3.2 μsec becomes 256 crossings

- Assuming rebuild of tracking & preshower electronics will store this many samples

Do we need more?

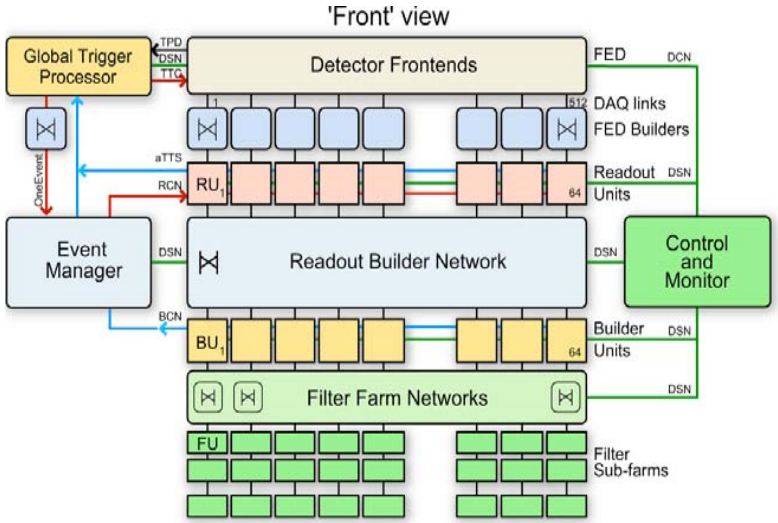
- Yield of crossings for processing only increases from ~70 to ~140
  - It's the cables!
- Parts of trigger already using higher frequency

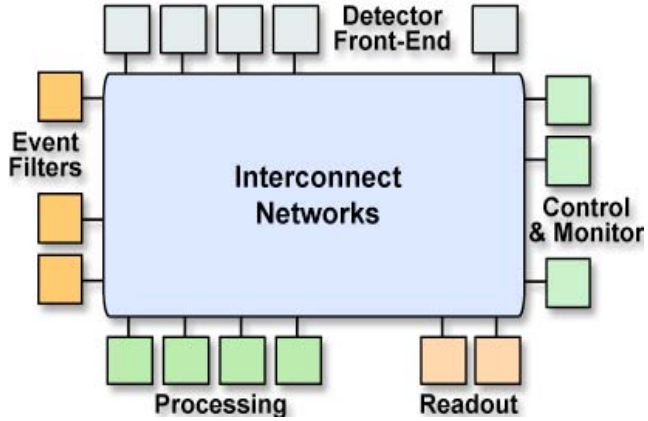
How much more? Justification?

- Combination with tracking logic
- Increased algorithm complexity
- Asynchronous links or FPGA-integrated deserialization require more latency
- Finer result granularity may require more processing time
- ECAL digital pipeline memory is 256 40 MHz samples = 6.4 μsec
  - Propose this as SLHC Level-1 Latency baseline

DAQ: Possible structure upgrade

- S. Cittolin





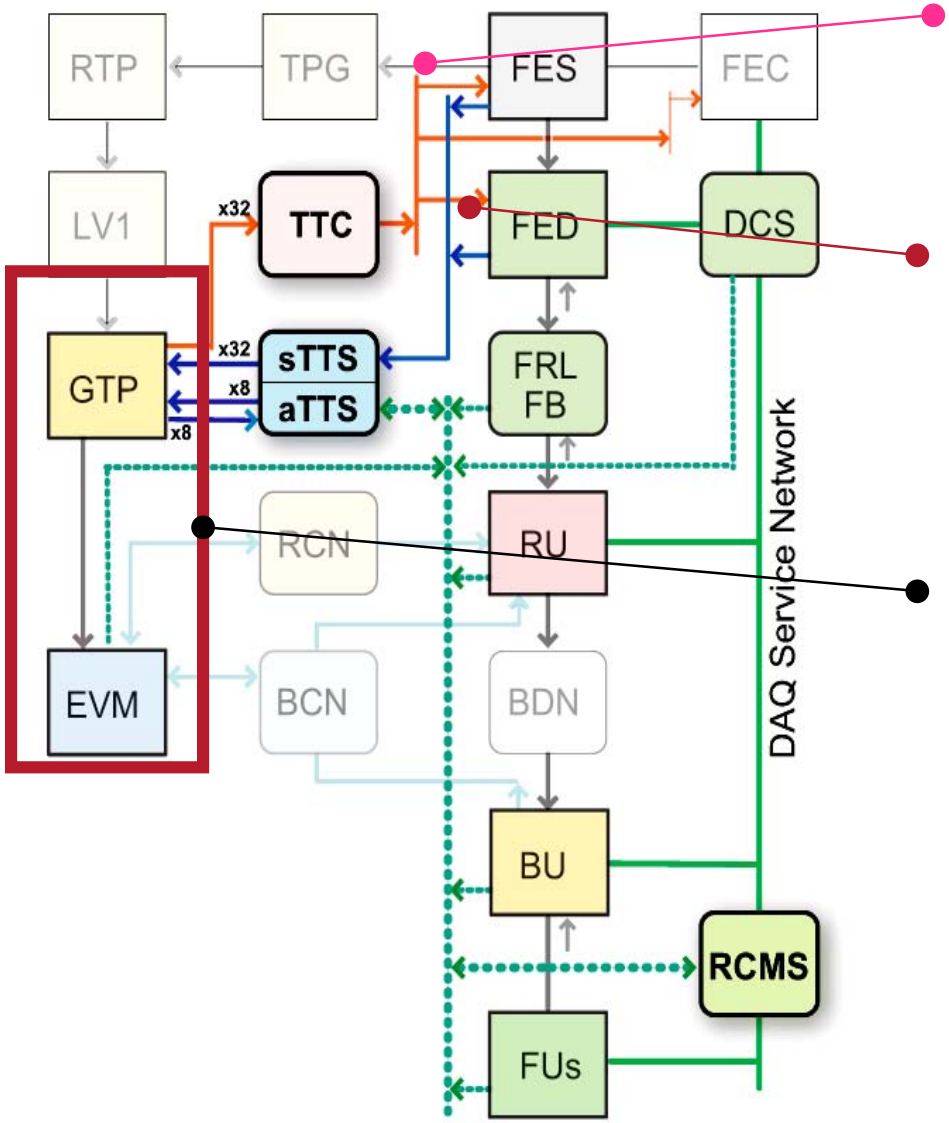
LHC DAQ design:

A network with Terabit/s aggregate bandwidth is achieved by two stages of switches and a layer of intermediate data concentrators used to optimize the EVB traffic load.
RU-BU Event buffers ~100GByte memory cover a **real-time interval of seconds**

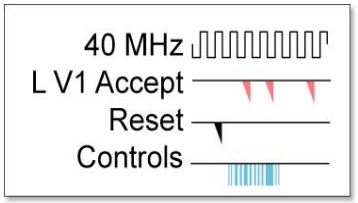
SLHC DAQ design:

A **multi-Terabit/s network** congestion free and scalable (as expected from communication industry).
In addition to the Level-1 Accept, the Trigger has to transmit to the FEDs additional information such as the event type and the event destination address that is the processing system (CPU, Cluster, TIER..) where the event has to be built and analyzed.
The event fragment delivery and therefore the **event building will be warranted by the network protocols** and (commercial) network internal resources (buffers, multi-path, network processors, etc.)
Real time buffers of Pbytes temporary storage disks will cover a **real-time interval of days**, allowing to the event selection tasks a better exploitation of the available distributed processing power.

Distribute Time, Trigger & INFO



LHC-TTC signals from GTP to FED



+INFO:
Trigger type
Filter ID…

The Event Manager and Global Trigger Processor must have a tight interface

The EVM will update the 'list' of the available event filter services (CPU-IP, Farms, Tiers, etc.) where to send the events in function of their type. This information will be embedded in the event fragment and sent into the DAQ net which, by construction, will take care of the event building at destination.

SLHC Trigger Summary

Attempt to restrict upgrade to post-TPG electronics as much as possible where detectors are retained

New Features:

- **80 MHz I/O Operation**
- **Level-1 Tracking Trigger**
  - Inner pixel track & outer tracker stub
  - Reports "crude" P_T & multiplicity in ~ 0.1x 0.1 $\Delta\eta \times \Delta\phi$
- **Regional Muon & Cal Triggers report in ~ 0.1 x 0.1 $\Delta\eta \times \Delta\phi$**
- **Regional Level-1 Tracking correlator**
  - Separate systems for Muon & Cal Triggers
  - Separate crates covering $\Delta\eta \times \Delta\phi$ regions
  - Sits between regional triggers & global trigger
- **Latency of 6.4 μsec**

R&D Program needs to start soon. Planning starts now:

- **Realistic simulation of physics signals**
- **Technologies: FPGAs, Data-Links, Clocking, Backplanes**

Summary: DAQ R&D/upgrades

Event Builders

Upgrade: DAQ staging: follow network technologies

R&D: **IMPLEMENTATION of the DAQ-TDR**. Use the CMS DAQ staged approach as permanent test bed to evaluate new network technologies

Distributed Computing (DAQ-Grid standard architectures)

Upgrade: Integrate in the experiment Run Control and Monitor System (RCMS) the e-Grid and Web standards

R&D: **IMPLEMENTATION of the DAQ-TDR** Run Control system

Fast Controls (TTC-TTS trigger/readout signal loop)

Upgrade: Extend Level-1 information distribution to/from front-end. Trigger, Timing and Control (TTC) and Trigger Throttle System (TTS)

R&D: Develop a **TRIGGER-INFO DISTRIBUTION** . A new GHz TTC system or an ancillary fast message distribution system (Mega meesages/s)

Data to Surface (LVDS_FRL detector readout):

Upgrade: Double the readout bandwidth (ev. size x LV-1rate) and improve the front-end data merging and sampling facilities

R&D: **INTEGRATE 10 Gb/s** standard links into font-end readout custom systems