WBS	Task Name
3	Trigger and Data Acquisition

WBS	Task Name

3.1 Trigger

3.1.1 CSC Muon Trigger

Notes

This WBS element includes all the effort to develop, produce, assemble, install and commission the Regional Muon Trigger. The budget is for a de-scoped system with 3 muon stations, however, the design allows easy recovery of a 4 station system.

This element's costs are generated as the sum of lower–level WBS elements.

3.1.1.1 Muon Port Cards (MPC)

Notes

This WBS element includes all the effort to develop, produce, assemble, install and commission the Muon Port Card portion of the Regional Muon Trigger. These cards input muon stub data generated by the muon chambers on copper channel-link connections, and output data on optical fiber to the Track Finder system. In the reverse direction, the MPCs fan out the clock signals from the TTC interfaces to the muon chambers. There is no data generated by the Muon Port Cards.

The system contains 48 of these cards plus 7 spares. Each card is approximately 30cm x 45cm and is mounted on the Endcap Muon Detector, requiring power, cooling, and mounting. This element's costs are generated as the sum of lower–level WBS elements.

3.1.1.1.1 MPC Design

Notes

This WBS element represents all of the engineering required to design the Muon Port Cards.
The design engineering will proceed in two stages: an initial period in which the interfaces to Motherboards, Track Processors, and the system clock (TTC) are defined, and a prototype design stage in which these interfaces are realized.

The EDIA is based on experience with recent track stub finding prototype development for the CMS muon trigger (LCT card, J. Kubic), and comparable trigger projects in CDF (XFT, R. Hughes/B. Winer). The logic on the Muon Port Card will be very similar to that on the CSC Trigger Mother Board. This logic for the prototype is being implemented in a standard FPGA. Therefore, this element is rated to be of average difficulty. The maturity is that of a conceptual design.

3.1.1.1.1.1 MPC Initial System Design

Notes

Engineering work required in the initial formulation of a design document for the Muon Port Cards.

WBS	Task Name

3.1.1.1.1.2 MPC Initial Prototype Design

Notes

Engineering work required to begin a detailed, fully documented design for the Prototype Muon Port Cards.

3.1.1.1.1.3 MPC Prototype Design

Notes

Engineering work required to complete a detailed, fully documented design for the Prototype Muon Port Cards.

3.1.1.1.2 MPC Proto. Construction

Notes

This WBS element represents the sequential construction of two MPC prototypes which will be bench-tested as well as installed into a working chain of prototype devices. The first prototype is a performance prototype in which the functions of the MPC will be implemented as fully as possible. The second prototype is an engineering prototype in which mass production techniques and cost reductions are implemented.

The cost for this item is generated as the sum of lower-level WBS elements: active components, primarily FPGA and optical link devices, and board costs (M&S). EDIA is included for oversight of the construction of these prototypes.

3.1.1.1.2.1 MPC Proto. Constr. Manage

Notes

Engineering required to oversee construction of the MPC prototypes.

3.1.1.1.2.2 MPC Proto. Cables

Notes

Prototype cabling costs include data connections and clock fanout to 9 Trigger Motherboards, optical data connection to Muon Track Finder, and optical input from TTC system (Trigger and Timing Control).

3.1.1.1.2.3 MPC Proto. Components

Notes

Prototypes will require more expensive FPGAs than used in the final versions, since the price decreases with time for these devices. More chips will be socketed than in the final design.

The component cost used (6K/board x 2 boards) is typical of recent prototypes built for CMS (LCT card and Trigger Motherboard card).

3.1.1.1.2.4 MPC Proto. Boards

Notes

Prototypes will require more expensive boards, since in small volume the setup costs dominate the board cost. We expect to require quick board delivery in order to optimize

WBS Task Name

"MPC Proto. Boards" continued

Notes

the use of engineering manpower.

These boards are approximately 30cm x 45cm. The board cost used (4K/board x 2 boards) is typical of recent prototypes built for CMS (LCT card and Trigger Motherboard card).

3.1.1.1.2.5 MPC Proto. Optical Links

Notes

There are seven optical links per MPC. Cost/unit in small quantities is $714 (catalog).

3.1.1.1.2.6 MPC Proto. TTC Links

Notes

The prototype system requires one TTC link per board, but the main elements are the laser and associated controller logic, which is contained in a 3U mini-VME rack supplied by Bruce Taylor (Rutherford).

The cost of the total package has been fixed at $10K by Taylor to any CMS institution.

3.1.1.1.3 MPC Proto. Test

Notes

This WBS element represents engineering required for testing of the MPC prototypes.

The engineering EDIA is based on experience with prototype testing for front-end CSC muon trigger cards. Since the MPC will be built from standard FPGA’s and/or ASIC’s the difficulty is average. The maturity is that of a conceptual design.

3.1.1.1.4 MPC ASIC and Board Design

Notes

This WBS element represents all work required to turn prototype MPC designs into production version devices having optimized cost and reliability.

The cost estimate is based on experience with recent track stub finding prototype development for the CMS muon trigger, and comparable trigger projects in CDF. Since the MPC will be built from standard FPGA’s and/or ASIC’s,the difficulty is average. The maturity is that of a conceptual design.

3.1.1.1.5 MPC Active Components

Notes

This WBS element represents the purchase of the active components that are installed on the the 96 MPC boards required to operate the CSC Muon trigger, not including spares.

The board costs represent the sum of active components, primarily FPGA devices and Glink optical links.We assume 7 Gbaud links are required per MPC. Since high-speed

WBS Task Name

"MPC Active Components" continued

Notes

optical fiber links are new technology, this task is rated as difficult. The maturity is that of a conceptual design.

3.1.1.1.5.1 MPC FPGAs

Notes

The Muon Port Cards select the best muon stubs from those presented to it by 9 Motherboards. Each Motherboard sends 2 stubs, each is 31 bits. In order to handle the I/O required, it has been estimated that 5 FPGAs are required - 4 for data flow, and another to serve as controller. Present 10K50-series Altera chips can clock at 40 MHz and meet the I/O requirement, however, it appears that for production units, 80 MHz operation will probably be necessary to meet latency requirements. Future chips have already been announced by AT&T and Altera which should allow this.

Costing is done using 5 FPGAs per board. There are 48 boards in the base configuration. Since we are extrapolating to better performance, we use current pricing on the 10K50 Altera chips, which are $240 for the 10K50VBC356-1 (356-pin BGA package) in quantity 100-499 (Arrow Semiconductor).

3.1.1.1.5.2 MPC JTAG controller

Notes

Each MPC contains a JTAG controller chip for slow control interface.

The cost is $13.60 per JTAG controller (Texas Instruments SN74LVT8980DWR, quote from Arrow Semiconductor), and there is one chip per MPC, for a total of 48 chips.

3.1.1.1.5.3 MPC EPROM

Notes

The simplest way to configure FPGAs is to load them at power-on from EPROMs, even if a path for downloading the or modifying their configuration through a slow control system also exists. It is also simplest to assign one (relatively) inexpensive EPROM per FPGA.

Costing is done assuming one EPROM per FPGA, i.e. 5 per MPC . There are 48 boards in the base configuration, for a total of 240 chips. The price per EPROM is $7.80 in quantities of 100-499 (Altera EPC1, Newark), plus socket is $1.06 in quantities of 250-499 (Augat 808-AG11D, Newark). The total cost is $9.59/EPROM x 5 EPROM/board x 48 boards.

3.1.1.1.5.4 MPC Glinks to Track Finder

Notes

The Glink chips convert muon data signals to approximately 1 Gbaud data transfer to the Muon Track Finder (Sector Receiver cards). We require 7 Gbaud transmission rate out of the MPC cards to transmit 3 muon stubs (each 37 bits) in 25ns. Each data connection

WBS Task Name

"MPC Glinks to Track Finder" continued

Notes

requires a gigabit copper to optical transceiver such as from Finisar, gigabit parallel to serial transmitter chip such as the HP Glink HDMP-1012, and an optical connector.

There are 7 Glinks per MPC and 48 MPC cards in the base configuration, for a total of 336 links. Cost per link is from HCAL costing: optical transmitter $120, serializer $25, connector $10 for a total of $155/link (J. Elias, private communication).

3.1.1.1.5.5 MPC TTC optical links

Notes

The TTC (Timing and Control) chips are a custom device built by Rutherford laboratory to receive clock and control signals from a central location on optical fiber. The MPC receives these signals and fans them out to the Trigger Motherboards (TMB's). We assume that a rad-hard (i.e. expensive) chip will be used, since these chips are extensively used in the central detector.

There is one TTC per MPC and 48 MPC cards in the base configuration. Each TTC is costed at $300 (W. Smith, private communication).

3.1.1.1.5.6 MPC Channel Links to TMBs

Notes

Channel links are high-speed 28-bit parallel to serial LVDS transmitter chips made by National Instruments. These are used by the MPC to receive data from the Trigger Motherboards (TMB). Two channel links are required by each TMB to send data to the MPC, while one channel link carries clock and possibly other signals to the TMBs. Each MPC receives channel-link signals from 9 TMB. There are thus 27 channel links per MPC.

With 27 channel links per MPC and 48 MPC cards, there are 1296 channel links in the base configuration. Each channel link is costed at $12.30 (Natl. Instruments DS90CR284MTD from Hamilton-Hallmark in quantities of 99+).

3.1.1.1.6 MPC Boards

Notes

This WBS element represents the production of 48 MPC circuit boards and their connectors and other passive elements.

The costs for this item represent the sum of lower-level WBS items. M&S items include board manufacturing, assembly, connectors, and other passive components. Engineering EDIA is included for management of the production, and technician EDIA is included for inspection and testing.The EDIA is extrapolated from past experience with production of boards for CDF, UA1, KTeV, and other experiments. Since these are standard boards, the difficulty is rated as average. The maturity is that of a conceptual design.

WBS	Task Name

3.1.1.1.6.1 MPC Board Prod. Manage

Notes

Engineering required to oversee construction of the MPC boards.

3.1.1.1.6.2 MPC Board Setup

Notes

This is a typical setup cost for manufacture of a 30cm x 45cm.

The cost is similar to that for prototypes built for CMS front-end electronics (LCT, J. Kubic, and TMB, P. Padley). Sales tax of 8.25% (California) is added.

3.1.1.1.6.3 MPC Board Fabrication

Notes

There are 48 boards, each 30cm x 45 cm. We assume a 10-layer PC board.

The cost is estimated using the result of a survey by D. Marlow (from TY Ling) that board costs can be approximated as $0.05/cm^2/layer pair. The cost is then (30cm x 45cm) x (5 layer pairs) x (48 boards) x $0.05/cm^2/layer pair. Sales tax of 8.25% (California) is added.

3.1.1.1.6.4 MPC Board Assembly

Notes

The system uses 48 boards. The cost per board for assembly is $150/board, which is typical of recent CMS projects (LCT card, J. Kubic; and TMB card, P. Padley). Sales tax of 8.25% (California) is added.

3.1.1.1.6.5 MPC Connectors-copper

Notes

There are 19 34-pin connector headers per MPC. Of these, 18 receive data from Trigger Motherboards (TMB), and another is used for slow control. There are 48 MPC, for a total of 912 connector headers.

The price per 34-pin connector header is estimated at $3.74 (Digi-Key catalog), times 912 connector headers in the system. Sales tax of 8.25% (California) is added.

3.1.1.1.6.6 MPC Misc components

Notes

Examples of miscellaneous components include: surface mount resistors and capacitors, tantalum capacitors, JTAG connector, test points, DIP switches, jumpers, LED's, miscellaneous chip sockets, miscellaneous buffers.

Miscellaneous components are budgeted at $100/board. A recent CMS prototype of smaller CAMAC size (LCT, J. Kubic) used $50 for capacitors, $10 for resistors, $5 for 10 LEDs. Sales tax of 8.25% (California) is added.

WBS	Task Name

3.1.1.1.6.7 MPC Inspection and Test

Notes

Technician work required for inspection and testing of boards. It is assumed that base program physicist labor will be used initially to set up a test station.

The cost is based on one technician-day per board.

3.1.1.1.7 MPC Mounting, Power, Cooling

Notes

The MPC cards are located near the periphery of the Endcap Muon system, on the endcap steel. It is anticipated that the location of these cards will not allow their mounting in standard crates. Therefore, there needs to be provision for mounting, and power and cooling services.

The estimated cost is $300/MPC times 48 MPC boards, based on experience with CMS prototypes as well as Zeus, KTeV, CDF, UA1, and TPC experiments. Sales tax of 8.25% (California) is added.

3.1.1.1.8 MPC Installation

Notes

This WBS element represents the engineering required for proper installation and debugging of the MPC cards in the CMS detector.

The engineering EDIA required is extrapolated from past experience on CDF, KTeV, and other experiments. A considerable fraction of the total effort will be physicist labor paid by the DOE base program. Since the installation will be a standard activity, the difficulty is rated as average. The maturity is that of a conceptual design.

3.1.1.1.9 MPC Spares

Notes

This WBS element represents the spare cards which are required to ensure a proper level of operation.
The difficulty is average, and the maturity is that of a conceptual design.

Spares are costed at the same price per board as the production units.There are 7 spares in addition to the 48 production boards.

3.1.1.1.10 MPC Motherboard Cables

Notes

There are 432 motherboards in the base system. By the use of channel-links chips to do high-speed parallel-to-serial conversion, all of the required trigger information can be carried from a Trigger Motherboards to an MPC on a 34-conductor connector. The average length of a TMB to MPC cable is 6 meters. An additional 64 cables are used as spares/wastage, for a total of 496 cables.

WBS Task Name

"MPC Motherboard Cables" continued

Notes

The quantity 496 is multiplied by the cost per cable of $64, which has been estimated as follows. Cost per 34-pin connector is $2.22 (Digi-Key catalog, >500 quantity). Cost for cable is $360/100ft (Electro-shield quote, TY Ling, 3/98), which is approximately $10/meter. Sales tax of 8.25% (California) is added.

3.1.1.2 Sector Receivers (SR)

Notes

This WBS element represents the design, prototyping, production, assembly, spares, installation, and testing of Sector Receiver (SR) cards. Each SR either receives data on 14 optical fibers from the Muon Port Cards (in the case that the cards are in the CSC-only crates), or equivalent data on copper cables (in the case that the cards are in the Overlap crates). Data is sent out of the SR cards on the Track Finder backplane. In the case that the SR is in a CSC-only crate, data is duplicated and sent out on copper to the Overlap crate. The SR also performs 2D to 3D muon stub conversion, chamber alignment corrections, and a modest data compression. The design is fully synchronous.

The cost estimate is derived as the sum of lower-level WBS items. There are 48 SR cards plus 8 spares. The cards are of size 9U x 400mm. We note that the cost per board is comparable to the estimated cost per board ($3220) for the Linker board of the XFT tracker for the CDF upgrade project. The boards use similar board space and part count for FPGA and other active components. The logic and function is relatively straightforward and therefore the difficulty is average. The maturity is that of a conceptual design.

3.1.1.2.1 SR Design

Notes

This WBS element represents all of the engineering required to design the Sector Receiver cards.
The design engineering will proceed in two stages: an initial period in which the interfaces to Muon Port Cards, the Track Finder crates (especially Sector Processors), and the duplication of data from SR cards in CSC-only crates to the SR cards in the Overlap crates are defined, and a prototype design stage in which these interfaces are realized.

The EDIA is based on experience with recent track stub finding prototype development for the CMS muon trigger (LCT card, J. Kubic), and comparable trigger projects in CDF (XFT, R. Hughes/B. Winer). This logic for the prototype is being implemented in a standard FPGA. Therefore, this element is rated to be of average difficulty. The maturity is that of a conceptual design.

3.1.1.2.1.1 SR Initial System Design

Notes

Engineering work required in the initial formulation of a design document for the Sector

WBS Task Name

"SR Initial System Design" continued

Notes

Receiver Cards.

3.1.1.2.1.2 SR Initial Proto. Design

Notes

Engineering work required to begin a detailed, fully documented design for the Prototype Sector Receiver Cards.

3.1.1.2.1.3 SR Proto. Design

Notes

ngineering work required to complete a detailed, fully documented design for the Prototype Sector Receiver Cards.

3.1.1.2.2 SR Proto. Construction

Notes

This WBS element represents the sequential construction of two SR prototypes which will be bench-tested as well as installed into a working chain of prototype devices. The first prototype is a performance prototype in which the functions of the SR will be implemented as fully as possible. The second prototype is an engineering prototype in which mass production techniques and cost reductions are implemented.

The cost for this item is generated as the sum of lower-level WBS elements: active components, primarily FPGA and optical link devices, and board costs (M&S). EDIA is included for oversight of the construction of these prototypes. Since the SR will be built from standard FPGA's and/or ASIC's the difficulty is average. The maturity is that of a conceptual design.

3.1.1.2.2.1 SR Proto. Constr. Manage

Notes

Engineering required to oversee construction of the SR prototypes.

3.1.1.2.2.2 SR Proto. Components

Notes

Prototypes will require more expensive FPGAs than used in the final versions, since the price decreases with time for these devices. More chips will be socketed than in the final design.

The component cost used (6K/board x 2 boards) is typical of recent prototypes built for CMS (LCT card and Trigger Motherboard card).

3.1.1.2.2.3 SR Proto. Boards

Notes

Prototypes will require more expensive boards, since in small volume the setup costs dominate the board cost. We expect to require quick board delivery in order to optimize

WBS Task Name

"SR Proto. Boards" continued

Notes

the use of engineering manpower.

The component cost used (4K/board x 2 boards) is typical of recent prototypes built for CMS (LCT card and Trigger Motherboard card).

3.1.1.2.3 SR Proto. Test

Notes

This WBS element represents engineering required for testing of the SR prototypes.

The cost estimate is based on comparable trigger projects in CDF and Zeus. Since the SR will be built from standard FPGA's and/or ASIC's,the difficulty is average. The maturity is that of a conceptual design.

3.1.1.2.4 SR ASIC and Board Design

Notes

This WBS element represents all work required to turn prototype SR designs into production version devices having optimized cost and reliability.

The cost estimate is based on comparable trigger projects in CDF and Zeus. Since the SR will be built from standard FPGA's and/or ASIC's,the difficulty is average. The maturity is that of a conceptual design.

3.1.1.2.5 SR Active Components

Notes

This WBS element represents the purchase of the active components that are installed on the SR boards required to operate the CSC Muon trigger, not including spares.

The cost is the sum of components in the lower-level WBS. The largest costs are for FPGA devices and Glink optical links. Since high-speed optical fiber receivers will be taken from other CMS designs, the task difficulty is rated as average. The maturity is that of a conceptual design.

3.1.1.2.5.1 SR FPGA's

Notes

In order to handle the I/O required, it has been estimated that 5 FPGAs are required - 4 for data flow, and another to serve as controller. Present 10K50-series Altera chips can clock at 40 MHz and meet the I/O requirement, however, it appears that for production units, 80 MHz operation will probably be necessary to meet latency requirements. Future chips have already been announced by AT&T and Altera which should allow this.

Costing is done using 5 FPGAs per board. There are 48 boards plus 8 spares. Since we are extrapolating to better performance, we use current pricing. Per board the FPGA

WBS Task Name

"SR FPGA's" continued

Notes

budget is $1110, described as follows. The 4 chips handling data use 10K50 Altera chips, which are $240 for the 10K50VBC356-1 (356-pin BGA package, high speed rating) in quantity 100-499 (Arrow Semiconductor). For the controller FPGA we use the $150 quote for the somewhat slower 10K50VBC356-2 (Arrow Semiconductor).

3.1.1.2.5.2 SR Glink Receivers

Notes

The Glink chips convert muon data signals to approximately 1 Gbaud data transfer to the Muon Track Finder (Sector Receiver cards). We require 7 Gbaud transmission rate from MPC cards to the Sector Receivers in order to transmit 3 muon stubs (each 37 bits) in 25ns. Each data connection requires a gigabit optical to copper transceiver such as from Finisar, gigabit serial to parallel converter chip such as the HP Glink HDMP-1014, and an optical connector.

There are 14 Glinks per SR and 24 SR cards (half) are instrumented with these transceivers in the base configuration, for a total of 336 links. Cost per link is from HCAL costing: optical receiver $101, deserializer $25, connector $10 for a total of $136/link (J. Elias, private communication).

3.1.1.2.5.3 SR EPROMs

Notes

The simplest way to configure FPGAs is to load them at power-on from EPROMs, even if a path for downloading the or modifying their configuration through a slow control system also exists. It is also simplest to assign one (relatively) inexpensive EPROM per FPGA.

Costing is done assuming one EPROM per FPGA, i.e. 5 per SR . There are 48 boards in the base configuration, for a total of 240 chips. The price per EPROM is $7.80 in quantities of 100-499 (Altera EPC1, Newark), plus socket is $1.06 in quantities of 250-499 (Augat 808-AG11D, Newark). Total cost is $9.59/EPROM x 240 EPROM.

3.1.1.2.5.4 SR FIFOs for DAQ

Notes

FIFO's are used by the Sector Receiver cards to store muon trigger information from the Muon Port Cards for DAQ readout during the Level 1 trigger latency period.The incoming information is 111 bits per MPC times 2 MPC connected to each SR, for a total of 222 bits. Additional bits for checksums, bunch crossing number, etc may be anticipated. FIFOs can also be used as cheap (relative to FPGA) pipeline storage of data which does not need processing directly by FPGAs. Typical FIFO's store 18 bits. Therefore, the assumption is that 15 FIFOs per board will be sufficient. The FIFOs on the market are "plenty deep", 1K is a typical lower limit.

The cost for a Texas Instruments 18bit x 1K FIFO is $15.25 (TI part SN74ACT780240PN

WBS Task Name

"SR FIFOs for DAQ" continued

Notes

quad flat package, from Arrow Semiconductor, quantities >120). The number of FIFO's in the system is 15 x 48 = 720.

3.1.1.2.5.5 SR Buffers

Notes

The SR cards either repeat the MPC data signals on copper, or receive them. In either case, buffer chips are needed to drive or receive the differential signals which pass between the CSC-only Track Finder crates and the CSC/Drift Tube Overlap Track Finder crates. There are 222 signals passed between each SR pair, which can be handled by 28 chips on each card, with each chip handling 8 signals.

The system contains 28 chips per board, times 48 SR cards, for a total of 1344 chips. The cost per buffer chip is estimated as approximately $5 (Digi-Key catalog, J. Kubic).

3.1.1.2.5.6 SR Memory Lookups

Notes

The SR boards will use memory look-up tables to translate 8-bit strip and wire pattern numbers into precise position coordinates in these two dimensions. They will also use memory look-up tables to do alignment corrections on the muon stub data. It is assumed that 24 memory lookup tables per card will suffice.

Cost for 32K (15-bit address) memory chips with 8-bit output and 15ns access time is $4.60 (Cypress CY7C1399-12VC from Arrow Semiconductor, quantity >100), times quantity of 24 chips/board x 48 boards = 1152 chips.

3.1.1.2.6 SR Boards

Notes

This WBS element represents the production of the 48 SR boards required to operate the CSC Muon trigger, not including 8 spares. Engineering EDIA is included for management of the production, and technician EDIA is included for inspection and testing.

The board costs represent the sum of board manufacturing costs, plus cables and connectors.The EDIA is extrapolated from past experience with production of boards for CDF, UA1, KTeV, Zeus and other experiments. Since these are standard boards, the difficulty is rated as average. The maturity is that of a conceptual design.

3.1.1.2.6.1 SR Const. Manage

Notes

Engineering required to oversee construction of the SR boards.

3.1.1.2.6.2 SR Board Setup

Notes

This is a typical setup cost for manufacture of a 30cm x 40cm.

WBS Task Name

"SR Board Setup" continued

Notes

The cost is similar to that for prototypes built for CMS front-end electronics (LCT, J. Kubic, and TMB, P. Padley).

3.1.1.2.6.3 SR Board Fabrication

Notes

There are 48 boards, each 30cm x 40 cm (9U x 400mm VME size). We assume a 10-layer PC board.

The cost is estimated using the result of a survey by D. Marlow (from TY Ling) that board costs can be approximated as $0.05/cm^2/layer pair. The cost is then (30cm x 40cm) x (5 layer pairs) x (48 boards) x $0.05/cm^2/layer pair.

3.1.1.2.6.4 SR Board Assembly

Notes

The system uses 48 boards. The cost per board for assembly is $150/board, which is typical of recent CMS projects (LCT card, J. Kubic; and TMB card, P. Padley).

3.1.1.2.6.5 SR Connectors-copper

Notes

There are 8 60-pin connector headers per SR, which connect to the cables carrying data between SR cards in CSC-only crates and the SR cards in the CSC/Drift Tube Overlap crates. There are 48 SR boards, for a total of 384 connector headers.

The price per 60-pin connector header is estimated at $3.74 (Digi-Key catalog), times 384 connector headers in the system.

3.1.1.2.6.6 SR Misc components

Notes

Examples of miscellaneous components include: surface mount resistors and capacitors, tantalum capacitors, JTAG connector, test points, DIP switches, jumpers, LED's, miscellaneous chip sockets, miscellaneous buffers.

Miscellaneous components are budgeted at $100/board. A recent CMS prototype of smaller CAMAC size (LCT, J. Kubic) used $50 for capacitors, $10 for resistors, $5 for 10 LEDs.

3.1.1.2.6.7 SR Front Panels and Hardware

Notes

These are standard VME modules, requiring a front panel milled for connector placement and LEDs, also with anodizing and silkscreening.

Recent experience with the LCT prototype (J. Kubic, 3/98) is used for costing as follows.

WBS Task Name

"SR Front Panels and Hardware" continued

Notes

Aluminum cost is negligible. The largest cost is the milling of aluminum panels, which takes 4 hours machinist for production quantities at $25/hr ($100/panel). Anodizing of aluminum panels costs $5/panel, silkscreening costs $10/panel, and screws and ejectors cost up to $10/board, for a base cost of $125. This is for a CAMAC-size front panel, a 9U front panel will be somewhat higher, also there are setup costs of $150 each on anodizing and silkscreening. Therefore, we use $150/board for front panels and mounting hardware.

3.1.1.2.6.7 SR Inspection and test

Notes

Technician work required for inspection and testing of boards. It is assumed that base program physicist labor will be used initially to set up a test station.

The cost is based on one technician-day per board.

3.1.1.2.7 SR Installation

Notes

This WBS element represents the engineering required for proper installation and debugging of the 48 SR Boards in the counting house.

The engineering EDIA required is extrapolated from past experience on CDF, UA1, KTeV, Zeus and other experiments. A considerable fraction of the total effort will be physicist labor paid by the DOE base program. Since the installation will be a standard activity, the difficulty is rated as average. The maturity is that of a conceptual design.

3.1.1.2.8 SR Spares

Notes

This WBS element represents the spare cards which are required to ensure a proper level of operating reliability.
The difficulty is average, and the maturity is that of a conceptual design. Because of the high cost of the optical links, the SR boards are stuffed in two different configurations (optical versus copper in).

The spares are costed at the same price as the production boards. There are 8 spares (4 of each type) budgeted in addition to the 48 production boards (24 of each type).

3.1.1.3 CSC Sector Processors (SP-CSC)

Notes

This WBS element represents the design, prototyping, production, assembly, and testing of the SP-CSC cards, which are Sector Processor cards which handle track finding in the CSC-only part of CMS.

The cost is derived as the sum of costs of lower-level WBS items: design, prototyping,

WBS Task Name

"CSC Sector Processors (SP-CSC)" continued

Notes

construction, inspection, installation, and spare units. There are 12 cards in the system, plus 3 spares. These are 9U x 400mm cards.
The interfaces to the SR boards and the Global Muon trigger, render this a difficult design. The maturity is that of a conceptual design.

3.1.1.3.1 SP-CSC Design

Notes

This WBS element represents all of the engineering required to design the Sector Processor cards for the CSC-only Track Finder crates (SP-CSC). The design engineering will proceed in two stages: an initial period in which the interfaces to the Track Finder crates (especially Sector Receivers), and the Global Muon trigger processor are defined, and a prototype design stage in which these interfaces are realized. In addition, however, the algorithm applied by this board for linking muon stubs will probably change as our knowledge of the muon background conditions in the CMS endcap region evolves over the next few years.

The EDIA is based on experience with recent track stub finding prototype development for the CMS muon trigger (LCT card, J. Kubic), and comparable trigger projects in CDF (XFT, R. Hughes/B. Winer). This logic for the prototype is being implemented in a standard FPGA. Because of the uncertainty in the algorithms to be applied by this board, this element is rated to have a high degree of difficulty. The maturity is that of a conceptual design.

3.1.1.3.1.1 SP-CSC Initial System Design

Notes

Engineering work required in the initial formulation of a design document for the Sector Processor cards in the CSC-only version.

3.1.1.3.1.2 SP-CSC Proto. Design

Notes

Engineering work required for a detailed, fully documented design for the Sector Processor cards (CSC-only version).

3.1.1.3.2 SP-CSC Proto. Construction

Notes

This WBS element represents the sequential construction of two SP-CSC prototypes which will be bench-tested as well as installed into a working chain of prototype devices. The first prototype is a performance prototype in which the functions of the SP-CSC will be implemented as fully as possible. The second prototype is an engineering prototype in which mass production techniques and cost reductions are implemented.

The cost for this item is generated as the sum of lower-level WBS elements: active

WBS **Task Name**

"SP-CSC Proto. Construction" continued

Notes

components, primarily FPGA and optical link devices, and board costs (M&S). EDIA is included for oversight of the construction of these prototypes. Since the SP-CSC will be built from standard FPGA's and/or ASIC's the difficulty is average. The maturity is that of a conceptual design.

3.1.1.3.2.1 SP-CSC Proto. Constr. Manage.

Notes

Engineering required to oversee construction of the SP-CSC prototypes.

3.1.1.3.2.2 SP-CSC Proto. Components

Notes

Prototypes will require more expensive FPGAs than used in the final versions, since the price decreases with time for these devices. More chips will be socketed than in the final design.

The component cost used (6K/board x 2 boards) is typical of recent prototypes built for CMS (LCT card and Trigger Motherboard card).

3.1.1.3.2.3 SP-CSC Proto. Boards

Notes

Prototypes will require more expensive boards, since in small volume the setup costs dominate the board cost. We expect to require quick board delivery in order to optimize the use of engineering manpower.

The component cost used (4K/board x 2 boards) is typical of recent prototypes built for CMS (LCT card and Trigger Motherboard card).

3.1.1.3.3 SP-CSC Proto. Test

Notes

This WBS element represents engineering required for testing of the SP-CSC prototypes. The cost estimate is based on comparable trigger projects in CDF and Zeus. This element is rated to be difficult. The maturity is that of a conceptual design.

3.1.1.3.4 SP-CSC ASIC and Board Design

Notes

This WBS element represents all work required to turn prototype SP-CSC design into production version devices having optimized cost and reliability.
The cost estimate is based on comparable trigger projects in CDF and Zeus. This element is rated to be difficult. The maturity is that of a conceptual design.

3.1.1.3.5 SP-CSC Active Components

Notes

This WBS element represents the purchase of the active components that are installed on

WBS Task Name

"SP-CSC Active Components" continued

Notes

the SP-CSC boards required to operate the CSC Muon trigger, not including spares. The board costs represent the sum of active components, primarily FPGA devices and ASIC's. This element is rated to be difficult. The maturity is that of a conceptual design.

3.1.1.3.5.1 SP-CSC FPGAs

Notes

In order to handle the track finding, it is estimated that 11 FPGAs per board are required - 10 for data processing, and another to serve as controller. Present 10K50-series Altera chips can clock at 40 MHz and meet the I/O requirement, however, it appears that for production units, 80 MHz operation will probably be necessary to meet latency requirements. Future chips have already been announced by AT&T and Altera which should allow this.
The 10 FPGA's/board is a good match to the 9U boards, and appears reasonable given the existence of a Vienna Sector Processor prototype to be used for the Drift Tube system. The Vienna Sector Processor prototype used 16 FPGAs on a
9U x 600mm card. The Vienna processor was simpler in that it used 22 bits/muon stub instead of the 31 bits/muon stub in the endcap system, and it handled track finding in the r-phi projection only. On the other hand, the SP-CSC and SP-OVR do not require signals from neighbor cards in the phi coordinate, which complicated the Vienna processor design.

There are 12 boards in the base system. Since we are extrapolating to better performance, we use current pricing. The SP-CSC budget for FPGAs is $2550 per board, described as follows. The 10 chips handling data use 10K50 Altera chips, which are $240 for the 10K50VBC356-1 (356-pin BGA package, high speed rating) in quantity 100-499 (Arrow Semiconductor). For the controller FPGA we use the $150 quote for the somewhat slower 10K50VBC356-2 (Arrow Semiconductor).

3.1.1.3.5.2 SP-CSC FIFOs

Notes

FIFO's are used by the Sector Processor cards to store output muon trigger information for DAQ readout during the Level 1 trigger latency period. It is assumed that 5 FIFOs per board will be sufficient. The FIFOs on the market are "plenty deep", 1K is a typical lower limit.

The cost for a Texas Instruments 18bit x 1K FIFO is $15.25 (TI part SN74ACT780240PN quad flat package, from Arrow Semiconductor, quantities >120). The number of FIFO's in the system is 5/board x 12 boards = 60.

3.1.1.3.5.3 SP-CSC EPROMs

Notes

The simplest way to configure FPGAs is to load them at power-on from EPROMs, even if a

WBS Task Name

"SP-CSC EPROMs" continued

Notes

path for downloading the or modifying their configuration through a slow control system also exists. It is also simplest to assign one (relatively) inexpensive EPROM per FPGA.

Costing is done assuming one EPROM per FPGA, i.e. 10 per SP-CSC . There are 12 boards in the base configuration, for a total of 120 chips. The price per EPROM is $7.80 in quantities of 100-499 (Altera EPC1, Newark), plus socket is $1.06 in quantities of 250-499 (Augat 808-AG11D, Newark). Total cost is $8.86/EPROM x 120 EPROM.

3.1.1.3.5.4 SP-CSC Buffers

Notes

The Sector Processor cards drive data signals to the Global Muon trigger on copper cables. Buffer chips are needed to drive the differential signals to the global muon trigger. Buffering may also be necessary for VME backplane signals or other external signals. It is assumed that these signals can be handled by 20 chips on each card, with each chip handling 8 signals.

The system contains 20 chips per board, times 12 SP-CSC cards, for a total of 240 chips. The cost per buffer chip is estimated as approximately $5 (Digi-Key catalog, J. Kubic).

3.1.1.3.6 SP-CSC Boards

Notes

This WBS element represents the production of the SP-CSC boards required to operate the CSC Muon trigger, not including spares. Engineering EDIA is included for management of the production, and technician EDIA is included for inspection and testing. The board costs represent the sum of board manufacturing costs, plus connectors.The EDIA is extrapolated from past experience with production of boards for CDF, UA1, KTeV, Zeus and other experiments. This element is rated to be difficult. The maturity is that of a conceptual design.

3.1.1.3.6.1 SP-CSC Constr. Manage

Notes

Engineering required to oversee construction of the SP-CSC boards.

3.1.1.3.6.2 SP-CSC Board Setup

Notes

This is a typical setup cost for manufacture of a 30cm x 40cm.

The cost is similar to that for prototypes built for CMS front-end electronics (LCT, J. Kubic, and TMB, P. Padley).

3.1.1.3.6.3 SP-CSC Board Fabrication

Notes

There are 12 boards, each 30cm x 40 cm (9U x 400mm VME size). We assume a

WBS Task Name

"SP-CSC Board Fabrication" continued

Notes

10-layer PC board.

The cost is estimated using the result of a survey by D. Marlow (from TY Ling) that board costs can be approximated as $0.05/cm^2/layer pair. The cost is then (30cm x 40cm) x (5 layer pairs) x (12 boards) x $0.05/cm^2/layer pair.

3.1.1.3.6.4 SP-CSC Board Assembly

Notes

The system uses 12 boards. The cost per board for assembly is $150/board, which is typical of recent CMS projects (LCT card, J. Kubic; and TMB card, P. Padley).

3.1.1.3.6.5 SP-CSC Connectors-copper

Notes

There are high-density connector headers on each SP-CSC for connecting to the data carried over the special backplane from the SR cards, as well as connector headers for the output signals to the Global Muon Trigger. The high-density connectors are about $10 each.

There are 5 high-density connectors per board at $10 each, for a cost of $50/board. There are 12 SP-CSC cards in the system.

3.1.1.3.6.6 SP-CSC Misc components

Notes

Examples of miscellaneous components include: surface mount resistors and capacitors, tantalum capacitors, JTAG connector, test points, DIP switches, jumpers, LED's, miscellaneous chip sockets, miscellaneous buffers.

Miscellaneous components are budgeted at $100/board. A recent CMS prototype of smaller CAMAC size (LCT, J. Kubic) used $50 for capacitors, $10 for resistors, $5 for 10 LEDs.

3.1.1.3.6.7 SP-CSC Front Panels and Hardware

Notes

These are standard VME modules, requiring a front panel milled for connector placement and LEDs, also with anodizing and silkscreening.

Recent experience with the LCT prototype (J. Kubic, 3/98) is used for costing as follows. Aluminum cost is negligible. The largest cost is the milling of aluminum panels, which takes 4 hours machinist for production quantities at $25/hr ($100/panel). Anodizing of aluminum panels costs $5/panel, silkscreening costs $10/panel, and screws and ejectors cost up to $10/board, for a base cost of $125. This is for a CAMAC-size front panel, a 9U front panel will be somewhat higher, also there are setup costs of $150 each on anodizing

WBS Task Name

"SP-CSC Front Panels and Hardware" continued

Notes

and silkscreening. Therefore, we use $150/board for front panels and mounting hardware.

3.1.1.3.6.8 SP-CSC Inspection and test

Notes

Technician work required for inspection and testing of boards. It is assumed that base program physicist labor will be used initially to set up a test station.

The cost is based on one technician-day per board.

3.1.1.3.7 SP-CSC Installation

Notes

This WBS element represents the engineering required for proper installation and debugging of the SP-CSC Boards in the counting house.
The engineering EDIA required is extrapolated from past experience on CDF, UA1, KTeV, Zeus and other experiments. A considerable fraction of the total effort will be physicist labor paid by the DOE base program. Since the installation will be a standard activity, the difficulty is rated as average. The maturity is that of a conceptual design.

3.1.1.3.8 SP-CSC Spares

Notes

This WBS element represents the spare cards which are required to ensure a proper level of operating reliability.
This element is rated to be difficult. The maturity is that of a conceptual design.

The spares are costed at the same price as the production boards. There are 3 spares budgeted in addition to the 12 production boards.

3.1.1.4 Overlap Sector Processors (SP-OVR)

Notes

This WBS element represents the design, prototyping, production, assembly, and testing of the SP-OVR cards, which are Sector Processor cards which handle track finding in the region of overlap between CSC muon chambers and Barrel muon chambers.

The cost is derived as the sum of costs of lower-level WBS items: design, prototyping, construction, inspection, installation, and spare units. There are 12 cards in the system, plus 3 spares. These are 9U x 400mm cards. The interfaces to the SR boards and the Global Muon trigger, render this a difficult design. The maturity is that of a conceptual design.

3.1.1.4.1 SP-OVR Design

Notes

This WBS element represents all of the engineering required to design the Sector Processor cards for the CSC-Drift Tube Overlap Track Finder crates (SP-OVR). The

WBS Task Name

"SP-OVR Design" continued

Notes

design engineering will proceed in two stages: an initial period in which the interfaces to the Track Finder crates (especially Sector Receivers), and the Global Muon trigger processor are defined, and a prototype design stage in which these interfaces are realized. In addition, however, the algorithm applied by this board for linking muon stubs will probably change as our knowledge of the muon background conditions in the CMS endcap region evolves over the next few years.

The EDIA is based on experience with recent track stub finding prototype development for the CMS muon trigger (LCT card, J. Kubic), and comparable trigger projects in CDF (XFT, R. Hughes/B. Winer). This logic for the prototype is being implemented in a standard FPGA. Because of the uncertainty in the algorithms to be applied by this board, this element is rated to have a high degree of difficulty. The maturity is that of a conceptual design.

3.1.1.4.1.1 SP-OVR Initial System Design

Notes

Engineering work required in the initial formulation of a design document for the Sector Processor cards in the CSC-DT Overlap version.

3.1.1.4.1.2 SP-OVR Proto. Design

Notes

Engineering work required for a detailed, fully documented design for the Sector Processor cards (CSC-DT overlap version).

3.1.1.4.2 SP-OVR Proto. Construction

Notes

This WBS element represents the sequential construction of two SP-OVR prototypes which will be bench-tested as well as installed into a working chain of prototype devices. The first prototype is a performance prototype in which the functions of the SP-OVR will be implemented as fully as possible. The second prototype is an engineering prototype in which mass production techniques and cost reductions are implemented.

The cost for this item is generated as the sum of lower-level WBS elements: active components, primarily FPGA and optical link devices, and board costs (M&S). EDIA is included for oversight of the construction of these prototypes. Since the SP-OVR will be built from standard FPGA’s and/or ASIC’s the difficulty is average. The maturity is that of a conceptual design.

3.1.1.4.2.1 SP-OVR Proto. Constr. Manage.

Notes

Engineering required to oversee construction of the SP-0VR prototypes.

WBS	Task Name

3.1.1.4.2.2 SP-OVR Proto. Components

Notes

Prototypes will require more expensive FPGAs than used in the final versions, since the price decreases with time for these devices. More chips will be socketed than in the final design.

The component cost used (6K/board x 2 boards) is typical of recent prototypes built for CMS (LCT card and Trigger Motherboard card).

3.1.1.4.2.3 SP-OVR Proto. Boards

Notes

Prototypes will require more expensive boards, since in small volume the setup costs dominate the board cost. We expect to require quick board delivery in order to optimize the use of engineering manpower.

The component cost used (4K/board x 2 boards) is typical of recent prototypes built for CMS (LCT card and Trigger Motherboard card).

3.1.1.4.3 SP-OVR Proto. Test

Notes

This WBS element represents engineering required for testing of the SP-OVR prototypes. The cost estimate is based on comparable trigger projects in CDF and Zeus. This element is rated to be difficult. The maturity is that of a conceptual design.

3.1.1.4.4 SP-OVR ASIC and Board Design

Notes

This WBS element represents all work required to turn the prototype SP-OVR design into production version devices having optimized cost and reliability.
The cost estimate is based on comparable trigger projects in CDF and Zeus. This element is rated to be difficult. The maturity is that of a conceptual design.

3.1.1.4.5 SP-OVR Active Components

Notes

This WBS element represents the purchase of the active components that are installed on the SP boards required to operate the CSC Muon trigger, not including spares.
The board costs represent the sum of active components, primarily FPGA devices and ASIC's. This element is rated to be difficult. The maturity is that of a conceptual design.

3.1.1.4.5.1 SP-OVR FPGAs

Notes

In order to handle the track finding, it is estimated that 11 FPGAs per board are required - 10 for data processing, and another to serve as controller. Present 10K50-series Altera chips can clock at 40 MHz and meet the I/O requirement, however, it appears that for production units, 80 MHz operation will probably be necessary to meet latency requirements. Future chips have already been announced by AT&T and Altera which

WBS Task Name

"SP-OVR FPGAs" continued

Notes

should allow this.
The 10 FPGA's/board is a good match to the 9U boards, and appears reasonable given the existence of a Vienna Sector Processor prototype to be used for the Drift Tube system. The Vienna Sector Processor prototype used 16 FPGAs on a
9U x 600mm card. The Vienna processor was simpler in that it used 22 bits/muon stub instead of the 31 bits/muon stub in the endcap system, and it handled track finding in the r-phi projection only. On the other hand, the SP-CSC and SP-OVR do not require signals from neighbor cards in the phi coordinate, which complicated the Vienna processor design.

There are 12 boards in the base system. Since we are extrapolating to better performance, we use current pricing. The SP-OVR budget for FPGAs is $2550 per board, described as follows. The 10 chips handling data use 10K50 Altera chips, which are $240 for the 10K50VBC356-1 (356-pin BGA package, high speed rating) in quantity 100-499(Arrow Semiconductor). For the controller FPGA we use the $150 quote for the somewhat slower 10K50VBC356-2 (Arrow Semiconductor).

3.1.1.4.5.2 SP-OVR FIFOs

Notes

FIFO's are used by the Sector Processor cards to store output muon trigger information for DAQ readout during the Level 1 trigger latency period. It is assumed that 5 FIFOs per board will be sufficient.

The cost for a Texas Instruments 18bit x 1K FIFO is $15.25 (TI part SN74ACT780240PN quad flat package, from Arrow Semiconductor, quantities >120). The number of FIFO's in the system is 5/board x 12 boards = 60.

3.1.1.4.5.3 SP-OVR EPROMs

Notes

The simplest way to configure FPGAs is to load them at power-on from EPROMs, even if a path for downloading the or modifying their configuration through a slow control system also exists. It is also simplest to assign one (relatively) inexpensive EPROM per FPGA.

Costing is done assuming one EPROM per FPGA, i.e. 10 per SP-OVR . There are 12 boards in the base configuration, for a total of 120 chips. The price per EPROM is $7.80 in quantities of 100-499 (Altera EPC1, Newark), plus socket is $1.06 in quantities of 250-499 (Augat 808-AG11D, Newark). Total cost is $8.86/EPROM x 120 EPROM.

3.1.1.4.5.4 SP-OVR Buffers

Notes

The Sector Processor cards drive data signals to the Global Muon trigger on copper cables. Buffer chips are needed to drive the differential signals to the global muon trigger.

WBS Task Name

"SP-OVR Buffers" continued

Notes

Buffering may also be necessary for VME backplane signals or other external signals. It is assumed that these signals can be handled by 20 chips on each card, with each chip handling 8 signals.

The system contains 20 chips per board, times 12 SP-OVR cards, for a total of 240 chips. The cost per buffer chip is estimated as approximately $5 (Digi-Key catalog, J. Kubic).

3.1.1.4.6 SP-OVR Boards

Notes

This WBS element represents the production of the SP-OVR boards required to operate the CSC Muon trigger, not including spares. Engineering EDIA is included for management of the production, and technician EDIA is included for inspection and testing. The board costs represent the sum of board manufacturing costs, plus connectors.The EDIA is extrapolated from past experience with production of boards for CDF, UA1, KTeV, Zeus and other experiments. This element is rated to be difficult. The maturity is that of a conceptual design.

3.1.1.4.6.1 SP-OVR Constr. Manage

Notes

Engineering required to oversee construction of the SP-OVR boards.

3.1.1.4.6.2 SP-OVR Board Setup

Notes

This is a typical setup cost for manufacture of a 30cm x 40cm.

The cost is similar to that for prototypes built for CMS front-end electronics (LCT, J. Kubic, and TMB, P. Padley).

3.1.1.4.6.3 SP-OVR Board Fabrication

Notes

There are 12 boards, each 30cm x 40 cm (9U x 400mm VME size). We assume a 10-layer PC board.

The cost is estimated using the result of a survey by D. Marlow (from TY Ling) that board costs can be approximated as $0.05/cm^2/layer pair. The cost is then (30cm x 40cm) x (5 layer pairs) x (12 boards) x $0.05/cm^2/layer pair.

3.1.1.4.6.4 SP-OVR Board Assembly

Notes

The system uses 12 boards. The cost per board for assembly is $150/board, which is typical of recent CMS projects (LCT card, J. Kubic; and TMB card, P. Padley).

WBS	Task Name

3.1.1.4.6.5 SP-OVR Connectors-copper

Notes

There are high-density connector headers on each SP-OVR for connecting to the data carried over the special backplane from the SR cards, as well as connector headers for the output signals to the Global Muon Trigger. The high-density connectors are about $10 each.

There are 5 high-density connectors per board at $10 each, for a cost of $50/board. There are 12 SP-OVR cards in the system.

3.1.1.4.6.6 SP-OVR Misc components

Notes

Examples of miscellaneous components include: surface mount resistors and capacitors, tantalum capacitors, JTAG connector, test points, DIP switches, jumpers, LED's, miscellaneous chip sockets, miscellaneous buffers.

Miscellaneous components are budgeted at $100/board. A recent CMS prototype of smaller CAMAC size (LCT, J. Kubic) used $50 for capacitors, $10 for resistors, $5 for 10 LEDs.

3.1.1.4.6.7 SP-OVR Front Panels and Hardware

Notes

These are standard VME modules, requiring a front panel milled for connector placement and LEDs, also with anodizing and silkscreening.

Recent experience with the LCT prototype (J. Kubic, 3/98) is used for costing as follows. Aluminum cost is negligible. The largest cost is the milling of aluminum panels, which takes 4 hours machinist for production quantities at $25/hr ($100/panel). Anodizing of aluminum panels costs $5/panel, silkscreening costs $10/panel, and screws and ejectors cost up to $10/board, for a base cost of $125. This is for a CAMAC-size front panel, a 9U front panel will be somewhat higher, also there are setup costs of $150 each on anodizing and silkscreening. Therefore, we use $150/board for front panels and mounting hardware.

3.1.1.4.6.8 SP-OVR Inspection and test

Notes

Technician work required for inspection and testing of boards. It is assumed that base program physicist labor will be used initially to set up a test station.

The cost is based on one technician-day per board.

3.1.1.4.7 SP-OVR Installation

Notes

This WBS element represents the engineering required for proper installation and debugging of the SP-OVR Boards in the counting house.

WBS Task Name

"SP-OVR Installation" continued

Notes

The engineering EDIA required is extrapolated from past experience on CDF, UA1, KTeV, Zeus and other experiments. A considerable fraction of the total effort will be physicist labor paid by the DOE base program. Since the installation will be a standard activity, the difficulty is rated as average. The maturity is that of a conceptual design.

3.1.1.4.8 SP-OVR Spares

Notes

This WBS element represents the spare cards which are required to ensure a proper level of operating reliability.
This element is rated to be difficult. The maturity is that of a conceptual design.

The spares are costed at the same price as the production boards. There are 3 spares budgeted in addition to the 12 production boards.

3.1.1.5 Clock&Control Cards (CCC)

Notes

This WBS element represents the design, prototyping, production, assembly, and testing of the Clock&Control cards (CCC), each of which acts as clock distribution and control cards for a Track Finder crate.

The cost is derived as the sum of costs of lower-level WBS items: design, prototyping, construction, inspection, installation, and spare units. There are 12 cards in the system, plus 3 spares. These are 9U x 400mm cards. The difficulty is average. Based on the existence of a very similar CCC card for the Calorimeter trigger, the maturity is that of a partial engineering design.

3.1.1.5.1 CCC Board Design

Notes

This WBS element represents all of the engineering required to design the CCC Boards. The cost is based on comparable trigger projects in CDF and Zeus. It is checked against the full-size CMS prototype calorimeter trigger Clock and Control Card already constructed and tested. The difficulty is average. Based on the existence of a very similar CCC card for the Calorimeter trigger, the maturity is that of a partial engineering design.

3.1.1.5.2 CCC Active Components

Notes

This WBS element represents the purchase of the active components that are installed on the CCC boards required to operate the CSC Muon trigger, not including spares.
The cost is based on comparable trigger projects in CDF and Zeus. It is checked against the full-size CMS prototype calorimeter trigger Clock and Control Card already constructed and tested. The difficulty is average. Based on the existence of a very similar CCC card for the Calorimeter trigger, the maturity is that of a partial engineering design.

WBS	Task Name

3.1.1.5.3 CCC Boards

Notes

This WBS element represents the production of the CCC (Clock and Control Cards) required to operate the CSC Muon trigger, not including spares. Engineering EDIA is included for management of the production, and technician EDIA is included for inspection and testing.

The cost is based on comparable trigger projects in CDF and Zeus. It is checked against the full-size CMS prototype calorimeter trigger Clock and Control Card already constructed and tested. The difficulty is average. Based on the existence of a very similar CCC card for the Calorimeter trigger, the maturity is that of a partial engineering design.

3.1.1.5.3.1 CCC Prod. Manage

Notes

Engineering required to oversee construction of the CCC boards.

3.1.1.5.3.2 CCC Setup and tooling

Notes

This is a typical setup cost for manufacture of a 30cm x 40cm.

The cost is similar to that for prototypes built for CMS front-end electronics (LCT, J. Kubic, and TMB, P. Padley).

3.1.1.5.3.3 CCC Boards

Notes

There are 8 boards, not including spares, each 30cm x 40 cm (9U x 400mm VME size). We assume a 10-layer PC board.

The cost is estimated using the result of a survey by D. Marlow (from TY Ling) that board costs can be approximated as $0.05/cm^2/layer pair. The cost is then (30cm x 40cm) x (5 layer pairs) x (8 boards) x $0.05/cm^2/layer pair.

3.1.1.5.3.4 CCC Board assembly

Notes

The system uses 8 boards. The cost per board for assembly is $150/board, which is typical of recent CMS projects (LCT card, J. Kubic; and TMB card, P. Padley).

3.1.1.5.3.5 CCC Connectors-copper

Notes

There are high-density connector headers on each CCC for connecting to the data carried over the special backplane from the SR cards, as well as connector headers for the output signals to the Global Muon Trigger. The high-density connectors are about $10 each.

There are 3 high-density connectors per board at $10 each, for a cost of $30/board. There are 8 CCC cards in the system.

WBS	Task Name

3.1.1.5.3.6 CCC Misc components

Notes

Examples of miscellaneous components include: surface mount resistors and capacitors, tantalum capacitors, JTAG connector, test points, DIP switches, jumpers, LED's, miscellaneous chip sockets, miscellaneous buffers.

Miscellaneous components are budgeted at $100/board. A recent CMS prototype of smaller CAMAC size (LCT, J. Kubic) used $50 for capacitors, $10 for resistors, $5 for 10 LEDs.

3.1.1.5.3.7 CCC Front Panels and Hardware

Notes

These are standard VME modules, requiring a front panel milled for connector placement and LEDs, also with anodizing and silkscreening.

Recent experience with the LCT prototype (J. Kubic, 3/98) is used for costing as follows. Aluminum cost is negligible. The largest cost is the milling of aluminum panels, which takes 4 hours machinist for production quantities at $25/hr ($100/panel). Anodizing of aluminum panels costs $5/panel, silkscreening costs $10/panel, and screws and ejectors cost up to $10/board, for a base cost of $125. This is for a CAMAC-size front panel, a 9U front panel will be somewhat higher, also there are setup costs of $150 each on anodizing and silkscreening. Therefore, we use $150/board for front panels and mounting hardware.

3.1.1.5.3.7 CCC Inspection and test

Notes

Technician work required for inspection and testing of boards. It is assumed that base program physicist labor will be used initially to set up a test station.

The cost is based on one technician-day per board.

3.1.1.5.4 CCC Installation

Notes

This WBS element represents the engineering required for proper installation and debugging of the CCC Boards in the counting house.
The engineering EDIA required is extrapolated from past experience on comparable trigger projects in CDF and Zeus. A considerable fraction of the total effort will be physicist labor paid by the DOE base program. The cost is checked against that required for the full-size CMS prototype calorimeter trigger Clock and Control Card already constructed and tested. The difficulty is average. Based on the existence of a very similar CCC card for the Calorimeter trigger, the maturity is that of a partial engineering design.

3.1.1.5.5 CCC Spares

Notes

This WBS element represents the spare cards which are required to ensure a proper level

WBS Task Name

"CCC Spares" continued

Notes

of operating reliability.
The maturity is that of an engineering design. This task is rated as easy.

Spares are costed at the same price per board as the production units. There are 2 spares in addition to the 8 production boards.

3.1.1.6 Crate Monitor Cards

Notes

This WBS element includes all the effort to develop, produce, assemble, install and test the Muon Track Finder Crate Monitor Card. This card receives, checks and logs voltages and temperatures in the Muon Trigger Crates.
These are 9U x 400mm boards.

There are 8 cards in the base system, plus 2 for spares/prototype crates. The M&S and EDIA is based on boards used in the Zeus calorimeter trigger system, and in other crate systems. This task is straightforward. The maturity is that of a conceptual design

3.1.1.7 Muon Backplanes

Notes

This WBS element includes all the effort to develop, produce, assemble, install and test Track Processor Trigger Backplanes. The backplane is a monolithic, custom, 9U high printed circuit board with front and back card connectors. The top 3U of the backplane holds 4 row (128 pin) DIN connectors, capable of full 32 bit VME. The first two front slots of the backplane will, however, use three row (96 pin) DIN connectors in the P1 and P2 positions with the standard VME pinout. The bottom 6U of the backplane, in the data processing section of the crate, utilizes a single high speed, controlled impedance, connector for both front and rear insertion at each card position. The design is based around a 340 pin connector, by AMP Inc, to handle the high volume of data transmitted from the Sector Receiver cards to the Sector Processor Cards.

Both M&S and EDIA costs are based on the full-size prototype backplane already constructed and tested for the CMS calorimeter trigger. The task difficulty is rated as average. The design maturity is that of a conceptual design.

3.1.1.7.1 Muon Backplane Design

Notes

This WBS element represents all of the engineering required to design the Muon Trigger Backplanes.
The EDIA costs are based on the full-size prototype backplane already constructed and tested for the CMS calorimeter trigger. The task difficulty is rated as average. The design maturity is that of a conceptual design.

WBS	Task Name

3.1.1.7.2 Muon Backplane Procure

Notes

Cost of the backplane printed circuit boards and connectors, including assembly.

3.1.1.8 Crate Controllers

Notes

This WBS element includes all the effort to develop, produce, assemble, install and test the Regional Muon Trigger Crate Monitor Card. This card receives, checks and logs voltages and temperatures in the Muon Trigger Crates.
The M&S and EDIA is based on boards used in the Zeus calorimeter trigger system, and in other crate systems. This task is rated as straightforward. The maturity is that of a conceptual design

3.1.1.9 Muon Crates

Notes

This WBS element includes all the effort to procure, install and test the Track Processor Trigger Crates. The crate is based on standard Eurocard hardware with custom fittings. The height is 9U and the depth is 400mm.

The cost is based on the full-size prototype CMS calorimeter trigger Crate already constructed and tested. The task is straightforward. The items will be ordered from a catalog. The maturity is that of a conceptual design

3.1.1.10 Muon Power Supplies

Notes

This WBS element includes all the effort to procure, install and test the Muon Trigger Track Processor crate power supplies.

The cost is based on the power supplies purchased for the prototype Regional Calorimeter Trigger Crate. The task is easy. The items will be ordered from a catalog. The maturity is that of a conceptual design

3.1.1.11 Additional Cables

Notes

This WBS element includes all the effort to procure, install and test the Track Processor Trigger Cables. Each Receiver card sends some of its data off crate at 40 MHz to two neighboring crates. In addition, each Receiver gets data from three Barrel Track Finder crates. The 24 crates are located in pairs in a row of 12 adjacent racks. Crate to crate communication is handled by special cables running between the Receiver cards. The maximum amount of information shared between two Receiver cards in different crates is carried on 204 twisted pair (102 in each direction) at 40 Mhz. Special LVDS drivers/receivers may increase this to 140 Mhz effective transmission rate per twisted pair. The amount of cable is based on the number of interchanged signals and the crate layout in the racks in the electronics barracks.

WBS Task Name

"Additional Cables" continued

Notes

The cost for the cable is based on the cost for halogen free twist and flat differential-pair signal cable that carried signals at the same frequency for the Zeus trigger system. The task is straightforward. The items will be ordered from a catalog. The maturity is that of a conceptual design

3.1.1.11.1 Output Cables to Global Trigger

Notes

The output data signals from Sector Processor cards are carried to the Global muon trigger. There are 24 Sector Processor cards. Each Sector Processor sends output data on 6 60-pin cables. The base system contains 6x24=144 cables, to which is added 12 spare/prototype cables, for a total of 156 cables.

The average cost per cable is $30.50. The cost per cable is derived in the following way: Cable costs $360/100ft roll (Electro-shield quote, TY Ling, 3/98), or $23.76 per 6.6ft cable (6ft cable plus 10% wastage). A pair of connectors costs $3.74 each (Digi-Key catalog, CHB60D-ND). Assembly is included at $3 per cable.

3.1.1.11.2 Optical Fibers from MPC to SR

Notes

There are 7 optical fibers carrying trigger data from each MPC to the SR cards in the CSC-only Track Finder crate.
There are 48 MPC in the base system require 336 optical fibers, to which is added 49 additional fibers used for spares as well as for prototyping.

The cost per optical fiber is based on the optical fiber cost assumed for the HCAL readout, which uses a huge number of optical links. The cost (J. Elias, private communication) is $20/pair of installed connectors, plus $30/100m fiber, for a total of $50/fiber. This cost is multiplied by the 385 optical fibers.

3.1.1.11.3 Cables from SR-CSC to SR-OVR

Notes

All of the data signals from MPC to the Track Finder are received by optical transceivers on the SR modules in the CSC-only crates. These signals are carried to the Overlap Track Finder crates on copper connectors. There are 111 signals from each MPC. These can be carried on 4 60-pin cables.

The system contains 4x48=192 such cables, at an average cost of $30.50. The cost per cable is derived in the following way: Cable costs $360/100ft roll (Electro-shield quote, TY Ling, 3/98), or $23.76 per 6.6ft cable (6ft cable plus 10% wastage). A pair of connectors costs $3.74 each (Digi-Key catalog, CHB60D-ND). Assembly is included at $3 per cable.

WBS	Task Name

3.1.1.12 Trigger System Tests

Notes

This WBS element represents engineering required during installation and debugging in order to successfully commission the Muon Trigger.

The engineering EDIA required is extrapolated from past experience on CDF, KTeV, and other experiments. A considerable fraction of the total effort will be physicist labor paid by the DOE base program. It is also assumed that prior to the system-wide tests, the prototype versions will have been thoroughly tested in the U.S. together with front-end Endcap Muon motherboards and other trigger boards. The task difficulty is average. The cost is based on a conceptual design.

3.1.1.13 Trigger Project Management

Notes

This WBS element includes all the effort to provide project management of the Muon Trigger project.

The required 5% of an FTE engineer is provided by the UCLA base program and therefore there is no cost to the US CMS project.

3.1.1.13.1 Tracking & Reporting

Notes

All the effort to provide tracking and reporting of the Calorimeter Trigger project.

The effort involved is based on the tracking and reporting of the Zeus Calorimeter System and the SDC Trigger System. The required 5% of an FTE engineer is provided by the UCLA base program and therefore there is no cost to the US CMS project.

WBS	Task Name

3.1.2 Calorimeter Regional Trigger

Notes

All the effort to develop, produce, assemble, install and commission the Regional Calorimeter Trigger. This system processes the electromagnetic and hadronic trigger tower sums from the calorimeter front end electronics and delivers regional information on electrons, photons, jets, and partial energy sums to the global calorimeter level 1 trigger system. The system begins after the data from the front end electronics is received on optical fibers and translated to signals on copper and ends with cables that transmit the results to the calorimeter global level 1 trigger system.

This element's costs are generated as the sum of lower–level WBS elements

3.1.2.1 Prototypes

Notes

All the effort to develop, produce, assemble, install and test the Regional Calorimeter Trigger prototypes that have not yet been built or tested before FY98. These include the prototype Receiver Card, Electron Identification Card, Jet Summary Card, and Clock and Control Card. It also includes the prototype Phase and Boundary Scan ASICs. Each of these items is described in its corresponding WBS category below.

Each of the prototype M&S and EDIA costs have been generated from the costs for the final part as identified in the corresponding WBS element below

3.1.2.1.1 Proto. Receiver Card

Notes

All the effort to develop, produce, assemble, install and test the Prototype Regional Calorimeter Trigger Receiver Cards. The Receiver card is 9U by 400mm. The rear side of the card receives the calorimeter data from optical fibers, translates from fiber to copper, and converts from serial to parallel format. The front side of the card contains circuitry to synchronize the incoming data with the local clock, and check for data transmission errors. There are also lookup tables and adder blocks on the front. The lookup tables translate the incoming information to transverse energy on several scales. The energy summation tree begins on these cards in order to reduce the amount of data forwarded on the backplane to the Jet Summary card. Separate cable connectors and buffering are also provided for intercrate sharing.

The board is designed, laid out and has been submitted for manufacture. There is a bid package that has been sent out. This task is judged difficult based on the experience of the engineering design work.

3.1.2.1.1.1 Design Proto. RC

Notes

Engineering design of the prototype Receiver Card.

WBS	Task Name

3.1.2.1.1.2 Order Proto. RC

Notes

Engineering and Techncial work to order the prototype Receiver Card.

3.1.2.1.1.3 Purchase Proto. RC

Notes

Parts, board, and assembly cost for two prototype Receiver Cards. The cost for the second is to provide for a revised version.

3.1.2.1.1.4 Test Proto RC

Notes

Engineering and technical work to test the prototype Receiver Card.

3.1.2.1.2 Proto. Electron ID Card

Notes

All the effort to develop, produce, assemble, install and test the Prototype Regional Calorimeter Trigger Electron Identification Card. The Electron Identification Card receives data at 160 MHz in a staged fashion from the Receiver Cards and performs the electron identification algorithm described above. The Electron Identification card is 9U x 280mm and resides in the front of the crate. The electron isolation algorithm is performed on this card and the final results sorted to identify the 4 highest rank electron candidates.

The M&S and EDIA costs are based on the conceptual design of the Electron Identification Card, analysis of the layout of the prototype Receiver Card, the full-size prototype Clock and Control Card already constructed and tested, and design and manufacture of the 9U x 400 mm 83 MHz cards built for the Zeus trigger system. This card is simpler than the Receiver Card and it uses much of the circuitry already developed for the Receiver Card. Therefore, it is judged to have average difficulty. The maturity is of a conceptual design.

3.1.2.1.2.1 Design Proto. EIDC

Notes

Engineering design of the Prototype Electron Identification Card.

3.1.2.1.2.2 Order Proto. EIDC

Notes

Engineering and Technical work to order the Receiver Card.

3.1.2.1.2.3 Purchase Proto. EIDC

Notes

Parts, board and assembly cost for two prototype Electron Identification Cards. The cost for the second is to provide for a revised version.

3.1.2.1.2.4 Test Proto EIDC

Notes

Engineering and technical work to test the prototype Electron Identification Card.

WBS	Task Name

3.1.2.1.3 Proto. Phase ASIC

Notes

All the effort to develop, produce, assemble, and test the prototype Phase ASIC. The Phase ASIC on the Receiver Card is designed to receive four channels of parallel data from the serial/parallel converters at 120 MHz and align this data with the local trigger clock at an output rate of 160 MHz. It also handles the error detection code logic.

The Phase ASIC's M&S and EDIA cost is based on the prototype 8 x 13-bit 160 MHz Adder ASIC already manufactured and tested by Vitesse in GaAs. The estimate of the cost is based on the quote and actual cost of the Adder ASIC. The maturity is that of a conceptual design. The experience in the design and production of the Adder ASIC indicates that this task is of average difficulty.

3.1.2.1.3.1 Phase ASIC Proto Des.

Notes

Engineering design of the prototype Phase ASIC. This task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.1.3.2 Phase ASIC Proto. Order

Notes

Engineering and Techncial work to order the prototype Phase ASIC. This task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.1.3.3 Phase ASIC Proto. Purchase

Notes

Vendor NRE charge for the prototype Phase ASIC

3.1.2.1.4 Proto. BScan ASIC

Notes

All the effort to develop, produce, assemble, and test the prototype Boundary Scan ASIC.The Boundary Scan ASIC will provide access to registers on the outputs of the boards, driving backplane lines and board registers placed for diagnostics.

The Boundary Scan ASIC's M&S and EDIA cost is based on the prototype 8 x 13-bit 160 MHz Adder ASIC already manufactured and tested by Vitesse in GaAs. The estimate of the cost is based on the quote and actual cost of the Adder ASIC. The maturity is that of a conceptual design. The experience in the design and production of the Adder ASIC indicates that this task is of average difficulty.

3.1.2.1.4.1 BScan ASIC Proto Des.

Notes

Engineering design of the prototype Boundary Scan ASIC. This task is 75% performed by Wisconsin base program engineering with no cost to the US CMS Project and 25% of cost on project.

WBS	Task Name

3.1.2.1.4.2 BScan ASIC Proto. Order

Notes

Engineering and Techncial work to order the prototype Boundary Scan ASIC. This task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.1.4.3 BScan ASIC Proto. Purchase

Notes

Vendor NRE charge for the Boundary Scan ASIC.

3.1.2.1.5 Proto. Jet Summary Card

Notes

All the effort to develop, produce, assemble, install and test the Prototype Regional Calorimeter Trigger Jet Summary Card. The Jet Summary Card is a 9U x 280mm board the middle of the trigger data processing section of each regional trigger crate. It collects and summarizes data from both the Receiver cards and the Electron Isolation cards at 160 MHz. It produces the jet, electron, total Et, Ex, and Ey information and transmits it to the Global Calorimeter Trigger Processor.

The M&S and EDIA costs are based on the conceptual design of the Jet Summary Card, analysis of the layout of the prototype Receiver Card, the full-size prototype Clock and Control Card already constructed and tested, and design and manufacture of the 9U x 400 mm 83 MHz cards built for the Zeus trigger system, particularly the Zeus calorimeter trigger Adder Card that summarized information in a crate and transmitted it to the Zeus Global Calorimeter Trigger. This card is simpler than the Receiver Card and it uses much of the circuitry already developed for the Receiver Card and Electron Identification Card. Therefore, it is judged to have average difficulty. The maturity is of a conceptual design.

3.1.2.1.5.1 Design Proto. JSC

Notes

Engineering design of the prototype Jet Summary Card.

3.1.2.1.5.2 Order Proto. JSC

Notes

Engineering and Techncial work to order the prototype Jet Summary Card.

3.1.2.1.5.3 Purchase Proto. JSC

Notes

Parts, board, and assembly cost for two prototype Jet Summary Cards. The cost for the second is to provide for a revised version.

3.1.2.1.5.4 Test Proto JSC

Notes

Engineering and technical work to test the prototype Jet Summary Card.

WBS	Task Name

3.1.2.1.6 Proto. Clock & Control Card

Notes

All the effort to develop, produce, assemble, install and test the Prototype Regional Calorimeter Trigger Clock and Control Card. This card receives, aligns and logs the external 160 MHz clock and control signals and distributes them with adjustable delays along individual lines to each of the cards in the regional trigger crate.

The M&S and EDIA costs are based on the boards produced for the Zeus Calorimeter Trigger system and checked against the full-size prototype Clock and Control Card already constructed and tested. Since this card is a revision of the prototype already constructed, its costs can be based on the quote for the first prototype. The maturity is of an engineering design. Experience with the first prototype showed that this card is relatively straightforward.

3.1.2.1.6.1 Design Proto. CCC

Notes

Engineering design of the prototype Clock and Control Card.

3.1.2.1.6.2 Order Proto. CCC

Notes

Engineering and Techncial work to order the prototype Clock and Control Card.

3.1.2.1.6.3 Purchase Proto. CCC

Notes

Parts, board, and assembly cost for two prototype Clock and Control Cards. The cost for the second is to provide for a revised version.

3.1.2.1.6.4 Test Proto CCC

Notes

Engineering and technical work to test the prototype Clock and Control Card. 60% of the engineering work is performed by Wisconsin base program engineering at no cost to the US CMS Project.

3.1.2.1.7 Proto. Crate Monitor Card

Notes

All the effort to procure, install and test the Prototype Regional Calorimeter Trigger Crate Monitor Card. This modules serves as the crate environment monitor which may or may not be a commercial board. The decision to purchase or create a custom design will depend on the final requirements of the environmental monitoring system

The cost, servicing, operation and maintenance of the Prototype Crate Monitor Card is the responsibility of the Lisbon CMS group and there is no cost for this to US CMS.

WBS	Task Name

3.1.2.1.7.1 Procure Proto. CMC

Notes

All costs related with the purchase of the Prototype Control and Monitor Card. This is not a US CMS cost.

3.1.2.2 Preproduction ASICs

Notes

All the effort to develop, produce, assemble, and test the Preproduction ASIC's. These include the Electron ID ASIC, Adder ASIC, Phase ASIC and Boundary Scan ASIC.

The ASIC M&S and EDIA cost is based on the prototype 8 x 13-bit 160 MHz Adder ASIC already manufactured and tested by Vitesse in GaAs. The costs included in this WBS item are only the engineering costs and costs for Vitesse or another vendor to produce a test run of ASIC's. The production costs are assigned to the individual boards. Based on the experience with the Adder ASIC, these tasks are of average difficulty. The maturity of all the ASICs except the Adder ASIC is of a conceptual design. The Adder ASIC maturity is that of an engineering design.

3.1.2.2.1 Electron ID ASIC

Notes

All the effort to develop, produce, assemble, and test the Preproduction Electron ID ASIC. The Electron Identification ASIC, used on the Electron Identification Card, inputs 4 electromagnetic energies on an 8-bit scale every 6.25 nsec, as well as hadronic tower information and implements the algorithm described above to identify electrons.

The Electron ID ASIC M&S and EDIA cost is based on the prototype 8 x 13-bit 160 MHz Adder ASIC already manufactured and tested by Vitesse in GaAs. The costs included in this WBS item are only the engineering costs and costs for Vitesse or another vendor to produce a test run of ASIC's. The production costs are assigned to the individual boards below. Based on the experience with the Adder ASIC, these tasks are of average difficulty. The maturity is of a conceptual design.

3.1.2.2.1.1 EID ASIC Design

Notes

Engineering design of the Electron Identification ASIC.

3.1.2.2.1.2 EID ASIC Order

Notes

Engineering and Techncial work to order the Preproduction Electron Identification ASIC. This task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.2.1.3 EID ASIC Purchase

Notes

Vendor NRE charge for the Preproduction Electron Identification ASIC.

WBS	Task Name

3.1.2.2.2 Adder ASIC

Notes

All the effort to develop, produce, assemble, and test the Preproduction Adder ASIC. The Adder ASIC, used on the Receiver Card and Jet Summary Card, sums 8 13-bit (10 bit value, and one bit for sign, input overflow and arithmetic overflow) numbers in a single 25 nsec crossing.

The Adder ASIC M&S and EDIA cost is based on the prototype 8 x 13-bit 160 MHz Adder ASIC already manufactured and tested by Vitesse in GaAs. The final Adder ASIC will be a modification of this prototype ASIC, which has the full speed and function of the final ASIC. The costs included in this WBS item are only the engineering costs and costs for Vitesse or another vendor to produce a test run of ASIC's. The production costs are assigned to the individual boards below. Based on the experience with the Adder ASIC, these tasks are of average difficulty and the costs are based on the engineering design and actual cost for the Adder ASIC

3.1.2.2.2.1 Adder ASIC Design

Notes

Engineering design of the Adder ASIC

3.1.2.2.2.2 Adder ASIC Order

Notes

Engineering and Techncial work to order the Preproduction Adder ASIC. This task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.2.2.3 Adder ASIC Purchase

Notes

Vendor NRE charge for Preproduction Adder ASIC.

3.1.2.2.3 Sort ASIC

Notes

All the effort to develop, produce, assemble, and test the Preproduction Sort ASIC. The Sort ASIC is used on the Jet Summary Card to find the four largest of 32 10-bit values by shifting data in at 8 values every 6.25 nsec and outputting the four largest of the 32 within 100 nsec.

The Sort ASIC M&S and EDIA cost is based on the prototype 8 x 13-bit 160 MHz Adder ASIC already manufactured and tested by Vitesse in GaAs. A prototype Sort ASIC will be produced by the CMS Bristol group at no charge to the US group and this design will be modified to form the final Sort ASIC design. The costs included in this WBS item are only the engineering costs and costs for Vitesse or another vendor to produce a test run of ASIC's. The production costs are assigned to the individual boards below. Based on the experience with the Adder ASIC, these tasks are of average difficulty. The costs are based on conceptual designs.

WBS	Task Name

3.1.2.2.3.1 Sort ASIC Design

Notes

Engineering design of the Sort ASIC.

3.1.2.2.3.2 Sort ASIC Order

Notes

Engineering and Techncial work to order the Preproduction Sort ASIC. This task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.2.3.3 Sort ASIC Purchase

Notes

Vendor NRE charge for Preproduction Sort ASIC.

3.1.2.2.4 Phase ASIC

Notes

All the effort to develop, produce, assemble, and test the Preproduction Phase ASIC. The Phase ASIC on the Receiver Card is designed to receive four channels of parallel data from the serial/parallel converters at 120 MHz and align this data with the local trigger clock at an output rate of 160 MHz. It also handles the error detection code

The Phase ASIC M&S and EDIA cost is based on the prototype 8 x 13-bit 160 MHz Adder ASIC already manufactured and tested by Vitesse in GaAs. The costs included in this WBS item are only the engineering costs and costs for Vitesse or another vendor to produce a test run of ASIC's. The production costs are assigned to the individual boards below. Based on the experience with the Adder ASIC, these tasks are of average difficulty. The costs are based on conceptual designs.

3.1.2.2.4.1 Phase ASIC Design

Notes

Engineering design of the Phase ASIC.

3.1.2.2.4.2 Phase ASIC Order

Notes

Engineering and Techncial work to order the preproduction Phase ASIC. This task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.2.4.3 Phase ASIC Purchase

Notes

Vendor NRE charge for Preproduction Phase ASIC.

3.1.2.2.5 Boundary Scan ASIC

Notes

All the effort to develop, produce, assemble, and test the Preproduction Boundary Scan ASIC. The Boundary Scan ASIC will provide access to registers on the outputs of the boards, driving backplane lines and board registers placed for diagnostics.

WBS Task Name

"Boundary Scan ASIC" continued

Notes

The Boundary Scan ASIC M&S and EDIA cost is based on the prototype 8 x 13-bit 160 MHz Adder ASIC already manufactured and tested by Vitesse in GaAs. The costs included in this WBS item are only the engineering costs and costs for Vitesse or another vendor to produce a test run of ASIC's. The production costs are assigned to the individual boards below. Based on the experience with the Adder ASIC, these tasks are of average difficulty. The costs are based on conceptual designs.

3.1.2.2.5.1 Boundary Scan ASIC Design

Notes

Engineering design of the Boundary Scan ASIC.

3.1.2.2.5.2 Boundary Scan ASIC Order

Notes

Engineering and Techncial work to order the preproduction Boundary Scan ASIC. This task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.2.5.3 Boundary Scan ASIC Purchase

Notes

Vendor NRE charge for Preproduction Boundary Scan ASIC.

3.1.2.3 Test Facilities

Notes

All the effort to develop, produce, assemble, test and commission the Regional Calorimeter Trigger test facilities that will be used to check, diagnose and repair the production trigger production boards.

The cost is based on the assembled full production test facilities for the Zeus trigger system, which continue to operate for maintenance of this system. The costs are also based on the CMS trigger test facility already assembled and operated for test of the CMS Calorimeter Trigger Clock and Control Board and Backplane. Based on this experience, these tasks are of average difficulty. The test facilities are based on a conceptual design.

3.1.2.3.1 Design Test Facil.

Notes

All the effort to design the Regional Calorimeter Trigger test facilities that will be used to check, diagnose and repair the production trigger production boards.

The cost is based on the assembled full production test facilities for the Zeus trigger system, which continue to operate for maintenance of this system. The costs are also based on the CMS trigger test facility already assembled and operated for test of the CMS Calorimeter Trigger Clock and Control Board and Backplane. Based on this experience, this tasks is of average difficulty. The test facilities are based on a conceptual design. This

WBS **Task Name**

"Design Test Facil." continued

Notes

engineering for this task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.3.2 Procure Test Facil.

Notes

All the cost to procure the Regional Calorimeter Trigger test facilities that will be used to check, diagnose and repair the production trigger production boards.

The cost is based on the assembled full production test facilities for the Zeus trigger system, which continue to operate for maintenance of this system. The costs are also based on the CMS trigger test facility already assembled and operated for test of the CMS Calorimeter Trigger Clock and Control Board and Backplane. Based on this experience, these tasks are of average difficulty. The test facility is based on a conceptual design.

3.1.2.3.3 Assemble Test Facil.

Notes

all the effort to assemble, test and commission the Regional Calorimeter Trigger test facilities that will be used to check, diagnose and repair the production trigger production boards.

The cost is based on the assembled full production test facilities for the Zeus trigger system, which continue to operate for maintenance of this system. The costs are also based on the CMS trigger test facility already assembled and operated for test of the CMS Calorimeter Trigger Clock and Control Board and Backplane. Based on this experience, this task is of average difficulty. The test facility is based on a conceptual design.

3.1.2.4 Power Supplies

Notes

All the effort to select and procure the Regional Calorimeter Trigger crate power supplies.

The cost is based on the power supplies purchased for the Zeus Calorimeter Trigger system and checked against those purchased for the prototype Regional Calorimeter Trigger Crate. This is a straightforward task. The supplies are ordered from a catalog. The maturity is that of an engineering design.The testing is included in the Crate Testing (WBS 3.1.2.5.3).

3.1.2.4.1 Select Power Supplies

Notes

All the effort to select the Regional Calorimeter Trigger crate power supplies.

The cost is based on the power supplies purchased for the Zeus Calorimeter Trigger system and checked against those purchased for the prototype Regional Calorimeter

WBS Task Name

"Select Power Supplies" continued

Notes

Trigger Crate. This is an easy task. The supplies are ordered from a catalog

3.1.2.4.2 Power Supply Procure

Notes

All the cost and effort to procure the Regional Calorimeter Trigger crate power supplies.

The cost is based on the power supplies purchased for the Zeus Calorimeter Trigger system and checked against those purchased for the prototype Regional Calorimeter Trigger Crate. This is a straightforward task. The supplies are ordered from a catalog

3.1.2.4.2.1 PS Procure Manage

Notes

Engineering and Techncial work to order the Power Supplies. This task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.4.2.2 Purchase Power Supplies

Notes

Cost to purchase the power supplies.

3.1.2.4.2.3 2 PS Spares

Notes

Cost to purchase Power Supply Spares.

3.1.2.5 Crates

Notes

All the effort to procure, install and test the Regional Calorimeter Trigger Crates. The crate is based on standard Eurocard hardware with custom fittings. The height is 9U and the depth approximately 700mm, as determined by the front and rear card insertion. It requires a rack 900 mm deep to handle the crate depth with some reserve for cabling, plumbing, and other services. The front section of the crate is designed to accommodate 280mm deep cards, leaving the major portion of the volume for 400mm deep rear mounted cards.

The M&S and EDIA costs are based on the costs to produce the crates for the Zeus Calorimeter Trigger system and checked against the full-size prototype CMS Trigger Crate already constructed and tested. This is a straightforward task. The Crates are ordered from a catalog. The maturity is that of an engineering design.

3.1.2.5.1 Design Crate

Notes

All the effort to design the Regional Calorimeter Trigger Crates.

The M&S and EDIA costs are based on the costs to produce the crates for the Zeus

WBS Task Name

"Design Crate" continued

Notes

Calorimeter Trigger system and checked against the full-size prototype CMS Trigger Crate already constructed and tested. This is a straightforward task. The Crates are ordered from a catalog. The maturity is that of an engineering design.

3.1.2.5.2 Procure Crates

Notes

All the effort to procure the Regional Calorimeter Trigger Crates.

The M&S and EDIA costs are based on the costs to produce the crates for the Zeus Calorimeter Trigger system and checked against the full-size prototype CMS Trigger Crate already constructed and tested. This is a straightforward task. The Crates are ordered from a catalog. The maturity is that of an engineering design.

3.1.2.5.2.1 Crate Procure Manage

Notes

Engineering and Techncial work to order the crates. This task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.5.2.2 Purchase Crates

Notes

Cost to purchase the Crates.

3.1.2.5.2.3 2 Crate Spares

Notes

Cost to purchase the spare crates.

3.1.2.5.3 Test Crates

Notes

All the effort to test the Regional Calorimeter Trigger Crates.

The M&S and EDIA costs are based on the costs to produce the crates for the Zeus Calorimeter Trigger system and checked against the full-size prototype CMS Trigger Crate already constructed and tested. This is a straightforward task. The maturity is that of an engineering design.

3.1.2.6 Backplane

Notes

All the effort to develop, produce, assemble, install and test the Regional Calorimeter Trigger Backplanes. The backplane is a monolithic, custom, 9U high printed circuit board with front and back card connectors. The top 3U of the backplane holds 4 row (128 pin) DIN connectors, capable of full 32 bit VME. The first two front slots of the backplane will, however, use three row (96 pin) DIN connectors in the P1 and P2 positions with the standard VME pinout. The bottom 6U of the backplane, in the data processing section of

WBS Task Name

"Backplane" continued

Notes

the crate, utilizes a single high speed, controlled impedance, connector for both front and rear insertion at each card position. The design is based around a 340 pin connector, by AMP Inc., to handle the high volume of data transmitted from the Receiver cards to the Electron Identification and Jet Summary Cards.

The M&S cost for the PC Board is based on extrapolations of the Zeus Trigger PC Boards. The cost for the connectors is based on verbal quotes from AMP, Inc. The EDIA cost is based on the design and production of the Zeus Trigger Boards. The total cost is also checked against the full-size prototype backplane already constructed and tested. This is a difficult task. The cost is based on the engineering design of the prototype backplane and on the actual cost of the prototype backplane.

3.1.2.6.1 Design Backplane

Notes

All the effort to design the Regional Calorimeter Trigger Backplanes.

The EDIA cost is based on the design of the Zeus Trigger Boards and of the full-size prototype backplane already constructed and tested. This is a difficult task. The cost is based on the engineering design of the prototype backplane and on the actual cost to design the prototype backplane.

3.1.2.6.2 Backplane Procure

Notes

All the effort to procure the Regional Calorimeter Trigger Backplanes.

The M&S cost for the Backplane PC Board is based on extrapolations of the Zeus Trigger PC Boards and on the full-size prototype backplane already constructed and tested. The cost for the connectors is based on verbal quotes from AMP, Inc. The EDIA cost is based on the production of the Zeus Trigger Boards. The total cost is also checked against the full-size prototype backplane already constructed and tested. This is a difficult task. The cost is based on the engineering design of the prototype backplane and on the actual cost of the prototype backplane.

3.1.2.6.2.1 Bkpl Procure Manage

Notes

Engineering and Techncial work to order the backplane. The engineering for this task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.6.2.2 Bkpl Parts (Connectors)

Notes

Cost of connectors for the backplane.

WBS	Task Name

3.1.2.6.2.3 Bkpl Board

Notes

Cost of the backplane printed circuit board.

3.1.2.6.2.4 Bkpl Assembly

Notes

Cost to assemble the backplanes.

3.1.2.6.2.5 2 Bkpl Spares/Preprod

Notes

Cost to purchase 2 completed spare backplanes. The cost for the first is to provide for a preproduction prototype for verification before full production proceeds. The preproduction prototype will also serve as a spare.

3.1.2.6.3 Test Bkpl

Notes

All the effort to test the Regional Calorimeter Trigger Backplanes.

The EDIA cost is based on the experience with production testing of the Zeus Trigger Boards and checked against the full-size prototype backplane already constructed and tested. This is a difficult task. The cost is based on the engineering design of the prototype backplane.

3.1.2.7 Clock & Control Card

Notes

All the effort to develop, produce, assemble, install and test the Regional Calorimeter Trigger Clock and Control Card. This card receives, aligns and logs the external 160 MHz clock and control signals and distributes them with adjustable delays along individual lines to each of the cards in the regional trigger crate.

The M&S and EDIA costs are based on the boards produced for the Zeus Calorimeter Trigger system and checked against the full-size prototype Clock and Control Card already constructed and tested. Based on the experience with the prototype Clock and Control Card, this is a relatively straightforward task. The cost is based on the engineering design of the prototype Clock and Control Card.

3.1.2.7.1 Design CCC

Notes

All the effort to design the Regional Calorimeter Trigger Clock and Control Card.

The EDIA costs are based on the boards produced for the Zeus Calorimeter Trigger system and checked against the full-size prototype Clock and Control Card already constructed and tested. Based on the experience with the prototype Clock and Control Card, this is a relatively straightforward task. The cost is based on the engineering design of the prototype Clock and Control Card.

WBS	Task Name

3.1.2.7.2 CCC Procure

Notes

All the effort to procure the Regional Calorimeter Trigger Clock and Control Card.

The M&S costs are based on the boards produced for the Zeus Calorimeter Trigger system and checked against the full-size prototype Clock and Control Card already constructed and tested. Based on the experience with the prototype Clock and Control Card, this is a relatively straightforward task. The cost is based on the engineering design of the prototype Clock and Control Card.

3.1.2.7.2.1 CCC Procure Manage

Notes

Engineering and Techncial work to order the clock and control cards. The engineering for this task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.7.2.2 CCC Parts

Notes

Parts cost for the clock and control cards.

3.1.2.7.2.3 CCC Board

Notes

Printed circuit board cost for the clock and control cards.

3.1.2.7.2.4 CCC Assembly

Notes

Assembly costs for the clock and control cards.

3.1.2.7.2.5 2 CCC Spares/Preprod

Notes

Cost to purchase completed spare clock and control cards. The cost for the first is to provide for a preproduction prototype for verification before full production proceeds. The preproduction prototype will also serve as a spare.

3.1.2.7.3 Test CCC

Notes

All the effort to test the Regional Calorimeter Trigger Clock and Control Card.

The EDIA cost is based on the experience with production testing of the Zeus Trigger Boards and checked against the full-size prototype Clock & Control Card already constructed and tested. Based on the experience with the prototype Clock and Control Card, this is a relatively straightforward task. The cost is based on the engineering design of the prototype Clock and Control Card.

WBS	Task Name

3.1.2.8 Receiver Card

Notes

All the effort to develop, produce, assemble, install and test the Regional Calorimeter Trigger Receiver Cards. The Receiver card is 9U by 400mm. The rear side of the card receives the calorimeter data from optical fibers, translates from fiber to copper, and converts from serial to parallel format. The front side of the card contains circuitry to synchronize the incoming data with the local clock, and check for data transmission errors. There are also lookup tables and adder blocks on the front. The lookup tables translate the incoming information to transverse energy on several scales. The energy summation tree begins on these cards in order to reduce the amount of data forwarded on the backplane to the Jet Summary card. Separate cable connectors and buffering are also provided for intercrate sharing.

The M&S and EDIA costs are based on the design of the prototype Receiver Card being manufactured, and the design and manufacture of the Zeus 9U x 400 mm 83 MHz trigger boards. This is a difficult task. The cost is based on modifications to an existing engineering design.

3.1.2.8.1 Design RC

Notes

All the effort to design the Regional Calorimeter Trigger Receiver Cards.

The EDIA costs are based on the design of the prototype Receiver Card being manufactured, and the design and manufacture of the Zeus 9U x 400 mm 83 MHz trigger boards. This is a difficult task. The cost is based on modifications to an existing engineering design.

3.1.2.8.2 RC Procure

Notes

All the effort to procure the Regional Calorimeter Trigger Receiver Cards.

The M&S and EDIA costs are based on the design of the prototype Receiver Card being manufactured, and the design and manufacture of the Zeus 9U x 400 mm 83 MHz trigger boards. This is a difficult task. The cost is based on modifications to an existing engineering design.

3.1.2.8.2.1 RC Procure Manage

Notes

Engineering and Techncial work to order Receiver Cards. The engineering for this task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.8.2.2 RC Parts

Notes

Parts cost for the Receiver Card.

WBS	Task Name

3.1.2.8.2.3 RC Board

Notes

Printed circuit board cost for the Receiver Card.

3.1.2.8.2.4 RC Assembly

Notes

Assembly costs for the Receiver Card.

3.1.2.8.2.5 16 RC Spares/Preprod

Notes

Cost to purchase completed spare Receiver Cards. The cost for the first is to provide for a preproduction prototype for verification before full production proceeds. The preproduction prototype will also serve as a spare.

3.1.2.8.3 Test RC

Notes

All the effort to test the Regional Calorimeter Trigger Receiver Cards.

The EDIA costs are based on experience with the engineering design of the prototype Receiver Card being prepared for manufacture, and the production testing of the Zeus 9U x 400 mm 83 MHz trigger boards. This is a difficult task.

3.1.2.9 Electron Identification Card

Notes

Al the effort to develop, produce, assemble, install and test the Regional Calorimeter Trigger Electron Identification Card. The Electron Identification Card receives data at 160 MHz in a staged fashion from the Receiver Cards and performs the electron identification algorithm described above. The Electron Isolation card is 9U x 280mm and resides in the front of the crate. The electron isolation algorithm is performed on this card and the final results sorted to identify the 4 highest rank electron candidates.

The M&S and EDIA costs are based on the conceptual design of the Electron Identification Card, analysis of the costs of the prototype CMS Regional Calorimeter Receiver and Clock & Control Cards, and the design and manufacture of the Zeus 9U x 400 mm 83 MHz trigger boards. This is card is less complex than the Receiver Card and will use some of the circuitry developed for the Receiver Card. Therefore this task is of average difficulty.

3.1.2.9.1 Design ElC

Notes

This WBS element includes all the effort to design the Regional Calorimeter Trigger Electron Identification Card.

The EDIA costs are based on the conceptual design of the Electron Identification Card, analysis of the costs of the prototype CMS Regional Calorimeter Receiver and Clock & Control Cards, and the design and manufacture of the Zeus 9U x 400 mm 83 MHz trigger

WBS Task Name

"Design EIC" continued

Notes

boards. This is card is less complex than the Receiver Card and will use some of the circuitry developed for the Receiver Card. Therefore this task is of average difficulty.

3.1.2.9.2 EIC Procure

Notes

This WBS element includes all the effort to procure the Regional Calorimeter Trigger Electron Identification Cards.

The M&S and EDIA production costs are based on the conceptual design of the Electron Identification Card, analysis of the costs of the prototype CMS Regional Calorimeter Receiver and Clock & Control Cards, and the design and manufacture of the Zeus 9U x 400 mm 83 MHz trigger boards. This is card is less complex than the Receiver Card and will use some of the circuitry developed for the Receiver Card. Therefore this task is of average difficulty.

3.1.2.9.2.1 EIC Procure Manage

Notes

Engineering and Techncial work to order Electron Identification Cards. The engineering for this task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.9.2.2 EIC Parts

Notes

Parts cost for the Electroni Identification Cards.

3.1.2.9.2.3 EIC Board

Notes

Printed circuit board cost for the Electron Identification Card.

3.1.2.9.2.4 EIC Assembly

Notes

Assembly costs for the Electron Identification Cards.

3.1.2.9.2.5 16 EIC Spares/Preprod

Notes

Cost to purchase completed spare Electron Identficiation Cards. The cost for the first is to provide for a preproduction prototype for verification before full production proceeds. The preproduction prototype will also serve as a spare.

3.1.2.9.3 Test EIC

Notes

This WBS element includes all the effort to test the Regional Calorimeter Trigger Electron Identification Cards.

WBS Task Name

"Test EIC" continued

Notes

The M&S and EDIA costs are based on the conceptual design of the Electron Identification Card, analysis of the costs of the prototype CMS Regional Calorimeter Receiver and Clock & Control Cards, and the design and manufacture of the Zeus 9U x 400 mm 83 MHz trigger boards. This is card is less complex than the Receiver Card and will use some of the circuitry developed for the Receiver Card. Therefore this task is of average difficulty.

3.1.2.10 Jet Summary Card

Notes

All the effort to develop, produce, assemble, install and test the Regional Calorimeter Trigger Jet Summary Card. The Jet Summary Card is a 9U x 280mm board the middle of the trigger data processing section of each regional trigger crate. It collects and summarizes data from both the Receiver cards and the Electron Isolation cards at 160 MHz. It produces the jet, electron, total Et, Ex, and Ey information and transmits it to the Global Calorimeter Trigger Processor.

The M&S and EDIA costs are based on the conceptual design of the Jet Summary Card, analysis of the costs of the prototype CMS Regional Calorimeter Receiver and Clock & Control Cards, and the design and manufacture of the Zeus 9U x 400 mm 83 MHz trigger boards, particularly the Zeus calorimeter trigger Adder Card that summarized information in a crate and transmitted it to the Zeus Global Calorimeter Trigger. This card is simpler than the Receiver Card and Electron Identification Cards, and it uses much of the circuitry already developed for them. Therefore, it is rated of average difficulty and the cost is based on a conceptual design.

3.1.2.10.1 Design JSC

Notes

all the effort to design the Regional Calorimeter Trigger Jet Summary Card.

The M&S costs are based on the conceptual design of the Jet Summary Card,analysis of the costs of the prototype CMS Regional Calorimeter Receiver and Clock & Control Cards, and design and manufacture of Zeus trigger cards. This card is simpler than the Receiver Card and Electron Identification Cards, and it uses much of the circuitry already developed for them. Therefore, it is rated of average difficulty.

3.1.2.10.2 JSC Procure

Notes

All the cost to procure the Regional Calorimeter Trigger Jet Summary Cards.

The M&S and EDIA costs are based on the conceptual design of the Jet Summary Card, analysis of the costs of the prototype CMS Regional Calorimeter Receiver and Clock & Control Cards, and the production of the cards built for the Zeus trigger system. This card is simpler than the Receiver Card and Electron Identification Cards, and it uses much of

WBS **Task Name**

"JSC Procure" continued

Notes

the circuitry already developed for them. Therefore, it is rated of average difficulty.

3.1.2.10.2.1 JSC Procure Manage

Notes

Engineering and Techncial work to order Jet Summary Cards. The engineering for this task is performed by Wisconsin base program engineering with no cost to the US CMS Project.

3.1.2.10.2.2 JSC Parts

Notes

Parts cost for the Jet Summary Cards.

3.1.2.10.2.3 JSC Board

Notes

Printed circuit board cost for the Jet Summary Card.

3.1.2.10.2.4 JSC Assembly

Notes

Assembly costs for the Jet Summary Card.

3.1.2.10.2.5 2 JSC Spares/Preprod

Notes

Cost to purchase completed spare Jet Summary Cards. The cost for the first is to provide for a preproduction prototype for verification before full production proceeds. The preproduction prototype will also serve as a spare.

3.1.2.10.3 Test JSC

Notes

This WBS element includes all the effort to develop, produce, assemble, install and test the Regional Calorimeter Trigger Jet Summary Card.

The M&S and EDIA costs are based on the conceptual design of the Jet Summary Card, analysis of the costs of the prototype CMS Regional Calorimeter Receiver and Clock & Control Cards,and production testing of the Zeus trigger cards. This card is simpler than the Receiver Card and Electron Identification Cards, and it uses much of the circuitry already developed for them. Therefore, it is rated of average difficulty.

3.1.2.11 Cables

Notes

This WBS element includes all the effort to procure, install and test the Regional Calorimeter Trigger Cables. Each Receiver card sends some of its data off crate at 80 MHz to up to 5 neighboring crates. The 19 crates are located in pairs in a row of 10 adjacent racks. Crate to crate communication is handled by special cables running between the Receiver cards. The maximum amount of information shared between two

WBS Task Name

"Cables" continued

Notes

Receiver cards in different crates is carried on 204 twisted pair (102 in each direction) at 80 MHz.

The amount of cable is based on the number of interchanged signals and the crate layout in the racks in the electronics barracks. The cost for the cable is based on the cost for halogen free twist and flat differential-pair signal cable that carried signals for the Zeus trigger system. This is an easy task and the cables are ordered from a catalog.

3.1.2.12 DAQ Processor

Notes

This WBS element includes all the effort to procure, install and test the Regional Calorimeter Trigger DAQ Processor. This is the readout crate controller and communication module (ROC) provided by the CMS DAQ group.

The cost, servicing, operation and maintenance of the DAQ Processor is the responsibility of the Lisbon CMS group and there is no cost for this to US CMS.

3.1.2.13 Crate Monitor Card

Notes

This WBS element includes all the effort to procure, install and test the Regional Calorimeter Trigger Crate Monitor Card. This modules serves as the crate environment monitor which may or may not be a commercial board. The decision to purchase or create a custom design will depend on the final requirements of the environmental monitoring system.

The cost, servicing, operation and maintenance of the Crate Monitor Card is the responsibility of the Lisbon CMS group and there is no cost for this to US CMS.

3.1.2.13.1 CMC Procure

Notes

This WBS element includes all cost to procure the Regional Calorimeter Trigger Crate Monitor Card.

The cost, servicing, operation and maintenance of the Crate Monitor Card is the responsibility of the Lisbon CMS group and there is no cost for this to US CMS.

3.1.2.13.2 2 CMC Spares

Notes

This WBS element includes all cost to procure 2 spare Regional Calorimeter Trigger Crate Monitor Cards.

The cost, servicing, operation and maintenance of the Crate Monitor Card is the

WBS **Task Name**

"2 CMC Spares" continued

Notes

responsibility of the Lisbon CMS group and there is no cost for this to US CMS.

3.1.2.14 Trigger Tests

Notes

This WBS element includes all the effort to perform Calorimeter Regional Trigger system tests of fully instrumented crates, ship these crates to the CMS Hall at CERN, and commission the installation site, install, test, and commission the full Calorimeter Regional Trigger system in the CMS Hall electronics barracks.

The EDIA costs for testing of the fully instrumented crates are based on the experience in production testing of the Zeus Calorimeter Trigger electronics, a system of comparable size and number of high speed large electronics boards. The M&S for the shipping costs are based on the actual costs per crate of electronics incurred in shipping the Zeus Calorimeter Trigger electronics to DESY. The EDIA cost to commission the installation site, install, test, and commission the full Calorimeter Regional Trigger system in the CMS Hall electronics barracks is based on the actual experience in doing similar activities for the Zeus Calorimeter Trigger system at DESY. A considerable amount of effort will be physicist labor paid by the DoE base program at U. Wisconsin. This effort is only used for contingency. Therefore, while this task is difficult, it has the multiplier of 1.0 for a fixed cost since additional EDIA contingency is available from the DoE base program at U. Wisconsin.

3.1.2.14.1 Trigger Subsystem Tests

Notes

This WBS element includes all the effort to perform Calorimeter Regional Trigger system tests of fully instrumented crates.

The EDIA costs for testing of the fully instrumented crates are based on the experience in production testing of the Zeus Calorimeter Trigger electronics. This task is difficult, but it has the multiplier of 1.0 for a fixed cost since additional EDIA contingency is available from the DoE base program at U. Wisconsin.

3.1.2.14.2 Trigger System Installation

Notes

All the effort and cost to ship the Calorimeter Regional Trigger crates to the CMS Hall at CERN, and commission the installation site, install, test, and commission the full Calorimeter Regional Trigger system in the CMS Hall electronics barracks.

The M&S for the shipping costs are based on the actual costs per crate of electronics incurred in shipping the Zeus Calorimeter Trigger electronics to DESY. The EDIA cost to commission the installation site, install, test, and commission the full Calorimeter Regional

WBS **Task Name**

"Trigger System Installation" continued

Notes

Trigger system in the CMS Hall electronics barracks is based on the actual experience in doing similar activities for the Zeus Calorimeter Trigger system at DESY. This task is difficult, but it has the multiplier of 1.0 for a fixed cost since additional EDIA contingency is available from the DoE base program at U. Wisconsin.

3.1.2.14.2.1 Shipping

Notes

The M&S for the shipping costs are based on the actual costs per crate of electronics incurred in shipping the Zeus Calorimeter Trigger electronics to DESY.

3.1.2.14.2.2 Remote Site Commission

Notes

The EDIA cost to commission the installation site, install, test, and commission the full Calorimeter Regional Trigger system in the CMS Hall electronics barracks is based on the actual experience in doing similar activities for the Zeus Calorimeter Trigger system at DESY. This

3.1.2.14.2.3 Installation

Notes

The EDIA cost to commission the installation site, install, test, and commission the full Calorimeter Regional Trigger system in the CMS Hall electronics barracks is based on the actual experience in doing similar activities for the Zeus Calorimeter Trigger system at DESY.

3.1.2.15 Trigger Project Management

Notes

All the effort to provide project managment of the Calorimeter Trigger project.

The effort involved is based on the Project Management of the Zeus Calorimeter System and the SDC Trigger System. The required 5% of an FTE engineer is provided by the U. Wisconsin base program and therefore there is no cost to the US CMS project

3.1.2.15.1 Tracking & Reporting

Notes

All the effort to provide tracking and reporting of the Calorimeter Trigger project.

The effort involved is based on the tracking and reporting of the Zeus Calorimeter System and the SDC Trigger System. The required 5% of an FTE engineer is provided by the U. Wisconsin base program and therefore there is no cost to the US CMS project.

3.1.3 Physicist Activity

Notes

All physicist effort required for the trigger system.

WBS	Task Name

3.1.3.1 Muon Trigger

Notes

All physicist effort needed for the muon trigger project.

3.1.3.1.1 Simulation

Notes

Physicist effort for muon trigger simulation.

3.1.3.1.2 Software Development

Notes

Physicist effort to develop software for testing the muon trigger.

3.1.3.1.3 Testing

Notes

Physicist effort to test the muon trigger hardware.

3.1.3.1.4 Commissioning

Notes

Physicist effort to commission the muon trigger.

3.1.3.1.4 Management

Notes

Physicist effort to manage the muon trigger project.

3.1.3.2 Calorimeter Trigger

Notes

All physicist effort needed for the calorimeter trigger project.

3.1.3.2.1 Simulation

Notes

Physicist effort for calorimeter trigger simulation.

3.1.3.2.2 Software Development

Notes

Physicist effort to develop software for testing the calorimeter trigger.

3.1.3.2.3 Testing

Notes

Physicist effort to test the calorimeter trigger hardware.

3.1.3.2.4 Commissioning

Notes

Physicist effort to commission the calorimeter trigger.

3.1.3.2.4 Management

Notes

Physicist effort to manage the calorimeter trigger project.