Figure 6.24  An N-channel JFET with DC bias voltages applied. The depletion region (shown cross-hatched) grows as the reverse voltage across the PN junction is increased and reduces the volume of the conducting N region. The depletion region is thicker near the drain because the ohmic voltage drop across the N material connecting drain to source makes the reverse PN junction voltage larger in this area.
Fig. 5.1 Physical structure of the enhancement-type NMOS transistor: (a) perspective view; (b) cross section. Typically $L = 1$ to 10 $\mu$m, $W = 2$ to 500 $\mu$m, and the thickness of the oxide layer is in the range 0.02 to 0.1 $\mu$m.
Fig. 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An $n$ channel is induced at the top of the substrate beneath the gate.
Fig. 5.5 Operation of the enhancement NMOS transistor as $v_{DS}$ is increased. The induced channel acquires a tapered shape and its resistance increases as $v_{DS}$ is increased. Here, $v_{GS}$ is kept constant at a value $> V_t$.

$v_{DS}$ is increased, the channel becomes more tapered and its resistance increases correspondingly. Thus the $i_D-v_{DS}$ curve does not continue as a straight line but bends as shown in Fig. 5.6. Eventually, when $v_{DS}$ is increased to the value that reduces the voltage between gate and channel at the drain end to $V_t$—that is, $v_{GS} - v_{DS} = V_t$ or $v_{DS} = v_{GS} - V_t$—the channel depth at the drain end decreases to almost zero, and the channel is said to be

Fig. 5.6 The drain current $i_D$ versus the drain-to-source voltage $v_{DS}$ for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$. 

1. Triode: $v_{DS} < v_{GS} - V_t$
2. Saturation: $v_{DS} = v_{GS} - V_t$
3. Current saturates because the channel is pinched off at the drain end, and $v_{DS}$ no longer affects the channel.
4. $v_{GS} > V_t$

Curve bends because the channel resistance increases with $v_{DS}$

Almost a straight line with slope proportional to $(v_{GS} - V_t)$