EICard Data Path Checkout List: Card Number _____

First Steps: Put the EIC in slot 2, and fill the back of the crate with 7 RC's. Plug in 3 68-pin data-sharing cables in J4 from RC 0 to 1, RC 2 to 3, and RC 4 to 5. Log in to the **cmslab** account. Boot the crate and zero all the memories with **rctCrateTest –t 1**. Start **vmedia** and execute the script **eiso_data_paths.txt**. That will program things in the order given by the grey numbers. Place a check mark over the grey number.

Direct data: check at U125 (pin 8,11,14,17) and U126 (pins 8,11,14). First hex pattern should completely show up, second should have no bits firing at all (put the scope in auto trigger for all tests). All paths checked.

Path: # of Bits	First Pattern	Okay?	Second Pattern	Okay?
DIRECT A: 8 bits $440000	7F	1	00	2
DIRECT B: 8 bits $4c0000	7F	3	00	4
DIRECT C: 8 bits $540000	7F	5	00	6
DIRECT D: 8 bits $5c0000	7F	7	00	8
DIRECT E: 8 bits $640000	7F	9	00	10
DIRECT F: 8 bits $6c0000	7F	11	00	12
DIRECT G: 8 bits $740000	7F	13	00	14
DIRECT H: 8 bits $7c0000	7F	15	00	16

Shared data: The pattern is what should occur at the U125 and U126 like above. The third is a 7F followed by a 7F and will be a is a double pulse in each location.

Path: # of bits	Patt.	Okay?	Patt.	Okay?	Pattern	Okay?
Backplane R0: 8 bits	7F	17	00	18	7F and 7F	19
Repeat	7F	20	00	21	7F and 7F	22
Cable R0: 8 bits	7F	23	00	24	7F and 7F	25
Repeat	7F	26	00	27`	7F and 7F	28
Backplane R1: 8 bits	7F	29	00	30	7F and 7F	31
Repeat	7F	32	00	33	7F and 7F	34
Cable R1: 8 bits	7F	35	00	36	7F and 7F	37
Repeat	7F	38	00	39	7F and 7F	40
WEST(Backplane): 8 bits	7F	41	00	42	7F and 7F	43
EAST(Backplane): 8 bits	7F	44	00	45	7F and 7F	46

Corner Data: These are probably best checked at the PLCC's leading into the EISO ASIC for R0: U66: 24, 28, 4, 6 then 23, 27, 3, 5 and R1: U128: 24, 28, 4, 6 then 23, 27, 3, 5

Path(route): # of bits	Pattern	Okay?
SW(Backplane): 4 bits	FF	47
NW(Cable): 4 bits	FF	48
Move the West Cable to the East Side		
SE(Backplane): 4 bits	FF	49
NE(Cable): 4 bits	FF	50