```
### Log file for this test:  /afs/hep.wisc.edu/cms/RCTlog/daffodil/RC_2004-08-26
.log  ###
################################################################
################ RC Test 4 - JTAG all ASICS ########
### Test run on  2004-08-26_17:21:32
### HOST computer is:  daffodil
### Run executable fault_library
################################################################

Device to open: /dev/btp96
Device to open: /dev/btp160
Device to open: /dev/btp64
Enter command (help for usage)>
RCT boot succeeded with 2 cards.
Enter command (help for usage)> Enter command (help for usage)> Enter command (h
elp for usage)>
Starting to check the Phase to Adder
Device to open: /dev/btp96
Device to open: /dev/btp160
Device to open: /dev/btp64
Cards inserted 0080

 Card R3 is inserted

RC has barcode: f69c
Checking Phase 0 and 2 to Adder 0
Memory address 18440000
Had Memory address 18400000
Memory address 184C0000
Had Memory address 18480000
Memory address 18540000
Had Memory address 18500000
Memory address 185C0000
Had Memory address 18580000
Memory address 18640000
Had Memory address 18600000
Memory address 186C0000
Had Memory address 18680000
Memory address 18740000
Had Memory address 18700000
Memory address 187C0000
Had Memory address 18780000
Route OP 1 pin 0 OK!
Route OP 2 pin 0 OK!
Route OP 3 pin 0 OK!
Route OP 4 pin 0 OK!
Route OP 1 pin 1 OK!
Route OP 2 pin 1 OK!
Route OP 3 pin 1 OK!
Route OP 4 pin 1 OK!
Route OP 1 pin 2 OK!
Route OP 2 pin 2 OK!
Route OP 3 pin 2 OK!
Route OP 4 pin 2 OK!
Route OP 1 pin 3 OK!
Route OP 2 pin 3 OK!
Route OP 3 pin 3 OK!
Route OP 4 pin 3 OK!
Route OP 1 pin 4 OK!
Route OP 2 pin 4 OK!
Route OP 3 pin 4 OK!
Route OP 4 pin 4 OK!
```

Location of Logfile

SBS successfully booted and talked to cards in the crate

Only the CCC and the RC to be tested should be plugged in

Compare this number with the RC barcode

```
Route OP 1 pin 5 OK!
Route OP 2 pin 5 OK!
Route OP 3 pin 5 OK!
Route OP 4 pin 5 OK!
Route OP 1 pin 6 OK!
Route OP 2 pin 6 OK!
Route OP 3 pin 6 OK!
Route OP 4 pin 6 OK!
Route OP 1 pin 7 OK!
Route OP 2 pin 7 OK!
Route OP 3 pin 7 OK!
Route OP 4 pin 7 OK!

Checking Phase 1 and 3 to Adder 0
Memory address 18440000
Had2 Memory address 18400000
Memory address 184C0000
Had2 Memory address 18480000
Memory address 18540000
Had2 Memory address 18500000
Memory address 185C0000
Had2 Memory address 18580000
Memory address 18640000
Had2 Memory address 18600000
Memory address 186C0000
Had2 Memory address 18680000
Memory address 18740000
Had2 Memory address 18700000
Memory address 187C0000
Had2 Memory address 18780000
Route OP 1 pin 0 OK!
Route OP 2 pin 0 OK!
Route OP 3 pin 0 OK!
Route OP 4 pin 0 OK!
Route OP 1 pin 1 OK!
Route OP 2 pin 1 OK!
Route OP 3 pin 1 OK!
Route OP 4 pin 1 OK!
Route OP 1 pin 2 OK!
Route OP 2 pin 2 OK!
Route OP 3 pin 2 OK!
Route OP 4 pin 2 OK!
Route OP 1 pin 3 OK!
Route OP 2 pin 3 OK!
Route OP 3 pin 3 OK!
Route OP 4 pin 3 OK!
Route OP 1 pin 4 OK!
Route OP 2 pin 4 OK!
Route OP 3 pin 4 OK!
Route OP 4 pin 4 OK!
Route OP 1 pin 5 OK!
Route OP 2 pin 5 OK!
Route OP 3 pin 5 OK!
Route OP 4 pin 5 OK!
Route OP 1 pin 6 OK!
Route OP 2 pin 6 OK!
Route OP 3 pin 6 OK!
Route OP 4 pin 6 OK!
Route OP 1 pin 7 OK!
Route OP 2 pin 7 OK!
Route OP 3 pin 7 OK!
Route OP 4 pin 7 OK!
```

```
Checking Phase 4 and 6 to Adder 1
Memory address 18440000
Had Memory address 18400000
Memory address 184C0000
Had Memory address 18480000
Memory address 18540000
Had Memory address 18500000
Memory address 185C0000
Had Memory address 18580000
Memory address 18640000
Had Memory address 18600000
Memory address 186C0000
Had Memory address 18680000
Memory address 18740000
Had Memory address 18700000
Memory address 187C0000
Had Memory address 18780000
Route OP 1 pin 0 OK!
Route OP 2 pin 0 OK!
Route OP 3 pin 0 OK!
Route OP 4 pin 0 OK!
Route OP 1 pin 1 OK!
Route OP 2 pin 1 OK!
Route OP 3 pin 1 OK!
Route OP 4 pin 1 OK!
Route OP 1 pin 2 OK!
Route OP 2 pin 2 OK!
Route OP 3 pin 2 OK!
Route OP 4 pin 2 OK!
Route OP 1 pin 3 OK!
Route OP 2 pin 3 OK!
Route OP 3 pin 3 OK!
Route OP 4 pin 3 OK!
Route OP 1 pin 4 OK!
Route OP 2 pin 4 OK!
Route OP 3 pin 4 OK!
Route OP 4 pin 4 OK!
Route OP 1 pin 5 OK!
Route OP 2 pin 5 OK!
Route OP 3 pin 5 OK!
Route OP 4 pin 5 OK!
Route OP 1 pin 6 OK!
Route OP 2 pin 6 OK!
Route OP 3 pin 6 OK!
Route OP 4 pin 6 OK!
Route OP 1 pin 7 OK!
Route OP 2 pin 7 OK!
Route OP 3 pin 7 OK!
Route OP 4 pin 7 OK!

Checking Phase 5 and 7 to Adder 1
Memory address 18440000
Had2 Memory address 18400000
Memory address 184C0000
Had2 Memory address 18480000
Memory address 18540000
Had2 Memory address 18500000
Memory address 185C0000
Had2 Memory address 18580000
Memory address 18640000
Had2 Memory address 18600000
Memory address 186C0000
Had2 Memory address 18680000
```

```
Memory address 18740000
Had2 Memory address 18700000
Memory address 187C0000
Had2 Memory address 18780000
Route OP 1 pin 0 OK!
Route OP 2 pin 0 OK!
Route OP 3 pin 0 OK!
Route OP 4 pin 0 OK!
Route OP 1 pin 1 OK!
Route OP 2 pin 1 OK!
Route OP 3 pin 1 OK!
Route OP 4 pin 1 OK!
Route OP 1 pin 2 OK!
Route OP 2 pin 2 OK!
Route OP 3 pin 2 OK!
Route OP 4 pin 2 OK!
Route OP 1 pin 3 OK!
Route OP 2 pin 3 OK!
Route OP 3 pin 3 OK!
Route OP 4 pin 3 OK!
Route OP 1 pin 4 OK!
Route OP 2 pin 4 OK!
Route OP 3 pin 4 OK!
Route OP 4 pin 4 OK!
Route OP 1 pin 5 OK!
Route OP 2 pin 5 OK!
Route OP 3 pin 5 OK!
Route OP 4 pin 5 OK!
Route OP 1 pin 6 OK!
Route OP 2 pin 6 OK!
Route OP 3 pin 6 OK!
Route OP 4 pin 6 OK!
Route OP 1 pin 7 OK!
Route OP 2 pin 7 OK!
Route OP 3 pin 7 OK!
Route OP 4 pin 7 OK!

Checking the Adder to Adder routes!
All four pins from output wire 1 okay!
All four pins from output wire 2 okay!
All four pins from output wire 3 okay!
All four pins from output wire 4 okay!
All four pins from output wire 5 okay!
All four pins from output wire 6 okay!
All four pins from output wire 7 okay!
All four pins from output wire 8 okay!
All four pins from output wire 9 okay!
All four pins from output wire 10 okay!
All four pins 11 are tied to ground
All four pins from output wire 12 okay!
All four pins from output wire 13 okay!

Starting to check the memory to BSCAN Asic
Memories Mid 1 and Edge 0 to Bscan 0 and 1 OK!
Memory 3 to Bscan 2 Edge bit 3
Memory 3 to Bscan 2 Edge bit 4
Memory 3 to Bscan 2 Edge bit 5
Memory 3 to Bscan 2 Edge bit 6
Memories Mid 2 and Edge 3 to Bscan 2 and 3 OK!
Memory 4 to Bscan 4 Edge bit 3
Memory 4 to Bscan 4 Edge bit 4
Memory 4 to Bscan 4 Edge bit 5
Memory 4 to Bscan 4 Edge bit 6
```

```
Memories Mid 5 and Edge 4 to Bscan 4 and 5 OK!
Memories Mid 6 and Edge 7 to Bscan 6 and 7 OK!

################ RC Test 4 End ###################################
```