```
### Log file for this test:  /afs/hep.wisc.edu/cms/RCTlog/daffodil/RC_2004-08-26
.log  ###
```

Location of log file

```
##############################################################
################ RC Test 7 - Pattern tests (energy sums) ########
### Test run on  2004-08-26_19:04:34
### HOST computer is:  daffodil
### Run executable output_test
Please, check bit patterns on JSC J4, J5, J6.
##############################################################

Device to open: /dev/btp96
Device to open: /dev/btp160
Device to open: /dev/btp64
Enter command (help for usage)>
RCT boot succeeded with 16 cards.
Enter command (help for usage)> Enter command (help for usage)> Enter command (h
elp for usage)>
Zero memories first.
Device to open: /dev/btp96
Device to open: /dev/btp160
Device to open: /dev/btp64
RCTCrate::initialize() : vmeReset() successful
RCTCrate::initialize() : Defined RCTClockControlCard 10000000
RCTCrate::initialize() : Defined RCTReceiverCard with address 12000000
RCTCrate::initialize() : Defined RCTReceiverCard with address 14000000
RCTCrate::initialize() : Defined RCTReceiverCard with address 16000000
RCTCrate::initialize() : Defined RCTReceiverCard with address 18000000
RCTCrate::initialize() : Defined RCTReceiverCard with address 1b000000
RCTCrate::initialize() : Defined RCTReceiverCard with address 1d000000
RCTCrate::initialize() : Defined RCTReceiverCard with address 1f000000
RCTCrate::initialize() : Defined RCTElectronIsolationCard with address 11000000
RCTCrate::initialize() : Defined RCTElectronIsolationCard with address 13000000
RCTCrate::initialize() : Defined RCTElectronIsolationCard with address 15000000
RCTCrate::initialize() : Defined RCTElectronIsolationCard with address 17000000
RCTCrate::initialize() : Defined RCTElectronIsolationCard with address 1a000000
RCTCrate::initialize() : Defined RCTElectronIsolationCard with address 1c000000
RCTCrate::initialize() : Defined RCTElectronIsolationCard with address 1e000000
RCTCrate::initialize() : Defined RCTJetSummaryCard with address 19000000
rctCrateTest: initialize() succeeded
Cards in the crate are: 7fff
RCTCrate::doZeroPatternTest() : Loading RC (f500, 12000000)
RCTCrate::doZeroPatternTest() : Verifying RC (f500, 12000000)
RCTCrate::doZeroPatternTest() : Loading RC (fa00, 14000000)
RCTCrate::doZeroPatternTest() : Verifying RC (fa00, 14000000)
RCTCrate::doZeroPatternTest() : Loading RC (0, 16000000)
RCTCrate::doZeroPatternTest() : Verifying RC (0, 16000000)
RCTCrate::doZeroPatternTest() : Loading RC (f600, 18000000)
RCTCrate::doZeroPatternTest() : Verifying RC (f600, 18000000)
RCTCrate::doZeroPatternTest() : Loading RC (f700, 1b000000)
RCTCrate::doZeroPatternTest() : Verifying RC (f700, 1b000000)
RCTCrate::doZeroPatternTest() : Loading RC (fe00, 1d000000)
RCTCrate::doZeroPatternTest() : Verifying RC (fe00, 1d000000)
RCTCrate::doZeroPatternTest() : Loading RC (f800, 1f000000)
RCTCrate::doZeroPatternTest() : Verifying RC (f800, 1f000000)
RCTCrate::doZeroPatternTest() : Loading EIC (0, 11000000)
RCTCrate::doZeroPatternTest() : Verifying EIC (0, 11000000)
RCTCrate::doZeroPatternTest() : Loading EIC (f900, 13000000)
RCTCrate::doZeroPatternTest() : Verifying EIC (f900, 13000000)
RCTCrate::doZeroPatternTest() : Loading EIC (b100, 15000000)
RCTCrate::doZeroPatternTest() : Verifying EIC (b100, 15000000)
RCTCrate::doZeroPatternTest() : Loading EIC (0, 17000000)
RCTCrate::doZeroPatternTest() : Verifying EIC (0, 17000000)
```

SBS successfully booted and talked to the cards in the crate

Crate has to be fully loaded, with RC under test in slot 3: 1 CCC, 1 JSC, 7 EICs, 6 RCs and the RC under test

Check that the verification doesn't fail. When it does, leave the script (Ctrl-D) and vmedia (exit) and redo >run_RC_test7

```
RCTCrate::doZeroPatternTest() : Loading EIC (0, 1a000000)
RCTCrate::doZeroPatternTest() : Verifying EIC (0, 1a000000)
RCTCrate::doZeroPatternTest() : Loading EIC (0, 1c000000)
RCTCrate::doZeroPatternTest() : Verifying EIC (0, 1c000000)
RCTCrate::doZeroPatternTest() : Loading EIC (f800, 1e000000)
RCTCrate::doZeroPatternTest() : Verifying EIC (f800, 1e000000)
RCTCrate::doZeroPatternTest() : Loading JSC (ff00, 19000000)
RCTCrate::doZeroPatternTest() : Verifying JSC (ff00, 19000000)
rctCrateTest: All tests successful
Now fill the appropriate patterns into the memory.
Device to open: /dev/btp96
Device to open: /dev/btp160
Device to open: /dev/btp64
Type of test:  Random - 0, Ones - 1, Zeros - 2
Receiver Card 0
Bit Sequence 0: 3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F
Bit Sequence 1: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 2: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 3: 3333333333333333333333333333333333
Bit Sequence 4: 3333333333333333333333333333333333
Bit Sequence 5: 0303030303030303030303030303030303
Bit Sequence 6: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 7: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 8: 0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F
Bit Sequence 9: C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3
Bit Sequence 10: 0303030303030303030303030303030303
Bit Sequence 11: 3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C
Receiver Card 1
Bit Sequence 0: 3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F
Bit Sequence 1: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 2: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 3: 3333333333333333333333333333333333
Bit Sequence 4: 3333333333333333333333333333333333
Bit Sequence 5: 0303030303030303030303030303030303
Bit Sequence 6: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 7: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 8: 0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F
Bit Sequence 9: C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3
Bit Sequence 10: 0303030303030303030303030303030303
Bit Sequence 11: 3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C
Receiver Card 2
Bit Sequence 0: 3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F
Bit Sequence 1: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 2: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 3: 3333333333333333333333333333333333
Bit Sequence 4: 3333333333333333333333333333333333
Bit Sequence 5: 0303030303030303030303030303030303
Bit Sequence 6: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 7: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 8: 0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F
Bit Sequence 9: C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3
Bit Sequence 10: 0303030303030303030303030303030303
Bit Sequence 11: 3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C
Receiver Card 3
Bit Sequence 0: 3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F
Bit Sequence 1: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 2: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 3: 3333333333333333333333333333333333
Bit Sequence 4: 3333333333333333333333333333333333
Bit Sequence 5: 0303030303030303030303030303030303
Bit Sequence 6: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 7: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 8: 0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F
```

When the RC to be tested is in slot 3, only these pins need to be tested.

```
Bit Sequence 9: C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3
Bit Sequence 10: 0303030303030303030303030303030303
Bit Sequence 11: 3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C
Receiver Card 4
Bit Sequence 0: 3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F
Bit Sequence 1: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 2: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 3: 3333333333333333333333333333333333
Bit Sequence 4: 3333333333333333333333333333333333
Bit Sequence 5: 0303030303030303030303030303030303
Bit Sequence 6: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 7: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 8: 0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F
Bit Sequence 9: C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3
Bit Sequence 10: 0303030303030303030303030303030303
Bit Sequence 11: 000000000000000000000000000000001
```

Use this as trigger bit with the scope.

```
Receiver Card 5
Bit Sequence 0: 3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F
Bit Sequence 1: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 2: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 3: 3333333333333333333333333333333333
Bit Sequence 4: 3333333333333333333333333333333333
Bit Sequence 5: 0303030303030303030303030303030303
Bit Sequence 6: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 7: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 8: 0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F
Bit Sequence 9: C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3
Bit Sequence 10: 0303030303030303030303030303030303
Bit Sequence 11: 3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C
Receiver Card 6
Bit Sequence 0: 3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F3F
Bit Sequence 1: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 2: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 3: 3333333333333333333333333333333333
Bit Sequence 4: 3333333333333333333333333333333333
Bit Sequence 5: 0303030303030303030303030303030303
Bit Sequence 6: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 7: CFCFCFCFCFCFCFCFCFCFCFCFCFCFCFCF
Bit Sequence 8: 0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F0F
Bit Sequence 9: C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3
Bit Sequence 10: 0303030303030303030303030303030303
Bit Sequence 11: 3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C3C
## You can now start checking the output pattern on the JSC J4, J5, J6.
################ RC Test 7 End ################################
```