STC to Receiver Card Link Tests: RC Number_____

Setup: A RCT crate with at least one Receiver Card (RC) inserted in slot 3. At least 4 Receiver Mezzanine Cards (RMC) on the RC (all 8 is preferable). A separate VME crate with a set of STC cards and 20 m cables from the transmit mezzanine cards to the first of the RMC's on the RC.

Initialization: Power up both crates. Open two terminal windows on the PC, logging in remotely to another host to operate the crate controller for either the RCT or STC. Use one window for running vmedia in the subdirectory vmediaSTC for the STC, and one window should be in the subdirectory RCTvmedia for the RC. Before starting the RCT vmedia session, type rctBoot and then "b" and then type exit to return to the shell prompt. Use the checklist at the end of this document to keep track of each check as it is done.

1. To setup the RC enter vmedia and type:
    a. RCT: `vmedia> read setup_rc3.txt`
    which is equivalent to:
    b. RCT: `vmedia> read aa3.txt`
    c. RCT: `vmedia> poke 1 18000000 4`
    d. RCT: `vmedia> poke 1 18000002 00`
    e. RCT: `vmedia> poke 1 18000002 ff`
    f. RCT: `vmedia> poke 1 18000002 00`
    g. RCT: `vmedia> poke 1 18000006 98`

2. To do the first checks run the STC with incremental data:
    a. STC: `vmedia> read four_link_test.txt`
    b. STC: `vmedia> resettall`
    c. STC: `vmedia> read inc_long_error_c1.txt`
    d. STC: `vmedia> read inc_long_error_c3.txt`
    e. STC: `vmedia> read inc_long_error_c5.txt`
    f. STC: `vmedia> read inc_long_error_c7.txt`
    g. STC: `vmedia> idletall`
    h. STC: `vmedia> readyall`

3. Send a reset to the RCT system:
    a. RCT: `vmedia> resys`

4. Start sending data:
    a. STC: `vmedia> datat0`

5. To check the Compare Phase:
    a. RCT: `vmedia> dump 1 18000002` (several times)
    b. The top 8 of 16 bits (hex) show the CMP_PHS bit for each of the 8 ASICs on the board. For example, Phase ASIC 2 will have the bit in location (hex) 0400 stay at zero if the compare phase is working okay. This only works if a link is attached and running. Please repeat the dump several times to be certain it

stays at zero, because it may change! If this bit stays zero, put a check in the Compare Phase box for that ASIC below. If it doesn't stay zero for all four ASICS attached, CMP_PHS was probably not set up correctly for this configuration. This will have to be done before RC Links can be checked. Please report this and stop testing. If only one is misbehaving, please make note of that and stop testing and report this.

4. Probe on the RC to check the patterns for all bits
   a. Trigger on the error for a given phase ASIC to see the patterns. Resistors R110 and R111 (Schematic D0738 – SELCT_ERR) will have the error bits for each of the 8 Phase ASICs. You should only see one error bit. If you see more, stop the STC and repeat parts 2g-4 again. If you cannot seem to clear errors after several repetitions of these steps, start from step 2b. The patterns are easily seen in ECL on the translators (pins 1 and 4) at the data output of the 8 Phase ASICs (Schematics D0717, D0757, D0758, D0759, D0734, D0760, D0761, D0762 – RECV…). The quality bits can be seen on translators for the EMC Phase ASICs (pin 4), on R167 & R168 for the HD data. If the data checks out okay for the Phase ASICs, check all QB. Check BX0 for the first two phase ASICs at U453 pin 4 for EM and pin 7 for HD.
   b. Check relative timing with another link if you are using more than one link (i.e. compare error bit to data coming out of another Phase ASIC).

5. Double-check the EDC and Check the Zero Data
   a. Flip the 1 switch on SW16 to change the EDC interpretation. This should send the error bits to "high" levels and zero all the data instantly. Probe at the R110 and R111 and check a few of the data bits.

Checklist:

Phase ASIC	Compare Phase	Data: 16 bits	QB: 2 bits	BX0	EDC	Zero Data	Timing
0 (EM)							
1 (HD)							
2 (EM)				N/A			
3 (HD)				N/A			
4 (EM)				N/A			
5 (HD)				N/A			
6 (EM)				N/A			
7 (HD)				N/A			

If any test fails – please stop testing and put the card aside for more careful debugging.