

University of Wisconsin
APxF Rev K3 PCB Fabrication Specification
08-June-2026

General

1. Approximate dimensions: 322mm H × 282mm W × 2.3mm T. Refer to the fabrication drawing layer in the artwork for precise dimension and tolerance specifications.
2. 16-Layer board with sequential lamination, built on EM-890K and EM-37B.
3. Board to be manufactured in accordance with IPC-6011 and IPC-6012 (class 2) except where specified.
4. All features plotted as the intended final post-etch dimensions, with exception of controlled-impedance traces (see below).
5. Overall board finish is Immersion Gold, with a strip of hard gold along one edge, as defined in the plotted layer *tophardgold.pho*.
6. Red solder mask shall be used on both sides.
7. White silkscreen ink shall be used on both sides. Silkscreen may be clipped where necessary.
8. Combination of bow and twist shall not exceed 7.5 mils/inch in any direction.
9. Controlled impedance traces to be held to ±10% of target impedance
10. Design origin is the plated hole at the lower left corner. Artwork has been plotted with an (X,Y) offset of (3000 mils, 3000 mils)
11. Design to be plotted at a 22.5 degree rotation with respect to the warp/fill axis of the laminate material. If the panel cannot accommodate this rotation, then the vendor will indicate the practical degree of rotation.
12. Vendor may add thieving features to all electrical layers as necessary, with the following exception:
 - 6 polygonal regions at approximate plotted (X,Y) locations (7920, 13400) (8700, 13400) (8080, 8500) (8870, 8500), (4570, 5750) and (12130, 6460) (in mils) have copper keepout regions on layers 1-14. No thieving should be added in these regions on any layer.
 - Thieving to be kept at least 150 mils from active design features.
13. Vendor stackup and etch-compensated artwork (including rotation) to be approved prior to start of fabrication.

Stackup and Impedance Control

This section references stackup files [APxF_Stackup_Rev_31Mar2026.pdf](#) as a reference. This stackup was used on a prior build of this design.

14. Board has 16 electrical layers with laminations as follows:
 - a. Layers 1-8, EM-890K with blind vias.
 - b. Layers 11-16, EM-890K with blind vias.
 - c. Layers 1-16, with layers 9-10 on EM-370/EM-37B core/prepreg and plated/non-plated through holes.
15. Mechanically Spread (MS) glass must be used in the EM-890K sections of the stackup.
16. Plane Layers.
 - a. Layers 2, 4, 6, 8-11, 13 and 15 are copper plane layers.
 - b. Layers 2, 4, 6, 13 and 15 are 1 oz VLP-2 copper.
 - c. Layers 8 and 11 terminate blind via phases and are plated up to 2 oz nominal final weight from base HTE foil.
 - d. Layers 9 and 10 have 4 oz final weight.
17. Surface Layers 1 and 16 are HTE foil and plated up to 1.5 oz nominal final weight.
18. Internal routing layers 3, 5, 7, 12 and 14 are 0.5 oz VLP-2 copper.
19. Controlled Impedance Track Widths. The table below shows the plotted track widths and spacings for single-ended and differential controlled impedance traces. Track widths are subject to vendor modification.

Layer(s)	Controlled Impedance ($\pm 10\%$)	Plotted Track Width (mils)	Plotted Track Edge-Edge Spacing (mils)
1, 16	50 Ohm SE	7.4	
1, 16	100 Ohm DP	5.5	9
1	95 Ohm DP	6.2	8.3
3, 5, 7, 12, 14	50 Ohm SE	3.6	
3, 5, 7, 12, 14	100 Ohm DP	3.4	6.8
3, 5, 7	95 Ohm DP	3.7	6.5

20. Other tracks are plotted at nominal post-etch dimensions.

Holes

21. Hole counts are as follows (approximate):
- Plated holes, layers 1-16: **6237**.
 - Non-plated holes, layers 1-16: **129**.
 - Plated blind vias, layers 1-8: **3852**.
 - Plated blind vias, layers 11-16: **2519**.
22. Plated hole diameters in the artwork are given as final plated inside diameter, ± 3 mils, *except as specified in section 29, **Press-fit connector holes***. See the top and bottom drill plot files *topdrill.pho* and *botdrill.pho*.
23. All plated holes use positive etch-back, per IPC Class 2.
24. Blind and thru vias: the design has blind vias and thru plotted with 6, 8, 10 and 15 mil nominal drills.
- 6 mil vias are in blind phases only and drilled at 5.9 mils.
 - 8 mil vias are in blind phases only and drilled at 7.9 mils.
 - 10 mil vias are both blind and through the board and drilled at 9.5 mils.
 - 15 mil vias are both blind and through the board and drilled at 15.6 mils
25. All blind and through-hole vias plotted at 6, 8, 10 and 15 mils must be plated over to support via-in-pad assembly. Copper wrap is permitted where necessary to achieve uniform plating.
26. All through-holes not plated over must be free of debris and non-conductive material.
27. Vendor must remove any remaining non-connected pads from plated holes on all layers, with the following exceptions:
- Unconnected pads on layers 1 and 16.
 - Unconnected pads on layers 8 and 11 that terminate blind vias.
28. Backdrilling:
- Backdrilling locations are given in the Gerber file *botbackdrill.pho* as pad flashes.
 - There are 4 out of 80 holes to be backdrilled on the 15.75 mil nominal drill size.
 - Backdrilling diameter is left to the vendor, subject to existing plane clearances in the artwork.
 - Backdrilling is to be applied at layer 16 surface, drilling towards layer 1.
 - Backdrilling depth is subject to board stackup and drill depth tolerances. Target backdrill depth is from layer 16 to between layers 8 and 9. **Backdrills must not reach layer 8 at any location.**
29. Press-fit connector holes:
- Certain plotted drill sizes represent holes for press-fit connectors with specific associated final plated hole sizes and tolerances as set by the connector manufacturer.
 - The plotted drill size, associated final plated hole diameter and tolerance are given in the table below:

Plotted Artwork Drill Size (mils)	Final Plated Diameter (mils)	Tolerance (mils)
15.75	11.82	± 2
21.65	18.12	± 2
45.28	39.4	+3.5 -2.4

68.90	63.04	+3.5 -2.4
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30. Holes are plotted in 4 separate drill files, as follows:

- a. Blind vias, layers 1-8.
- b. Blind vias, layers 11-16.
- c. Plated through holes, layers 1-16.
- d. Non-plated through-holes, layers 1-16.

Testing

31. All layers to undergo inspection prior to lamination.
32. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 Ohms or less.
33. Resistance between planes and non-connected plated-through holes and vias shall be 10 Megaohms or larger.
34. Impedance on all signal layers shall be checked with TDR. Finished impedance shall be to the nominal value $\pm 10\%$.
35. Vendor shall provide appropriate coupons for testing.
36. Testing report to be enclosed with the quality control documentation shipped with the boards.
37. Locations in IPC-D-356A file are given in English units.