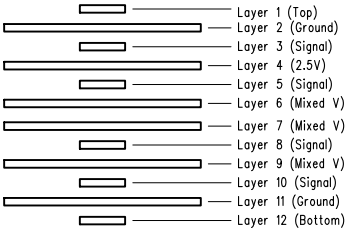
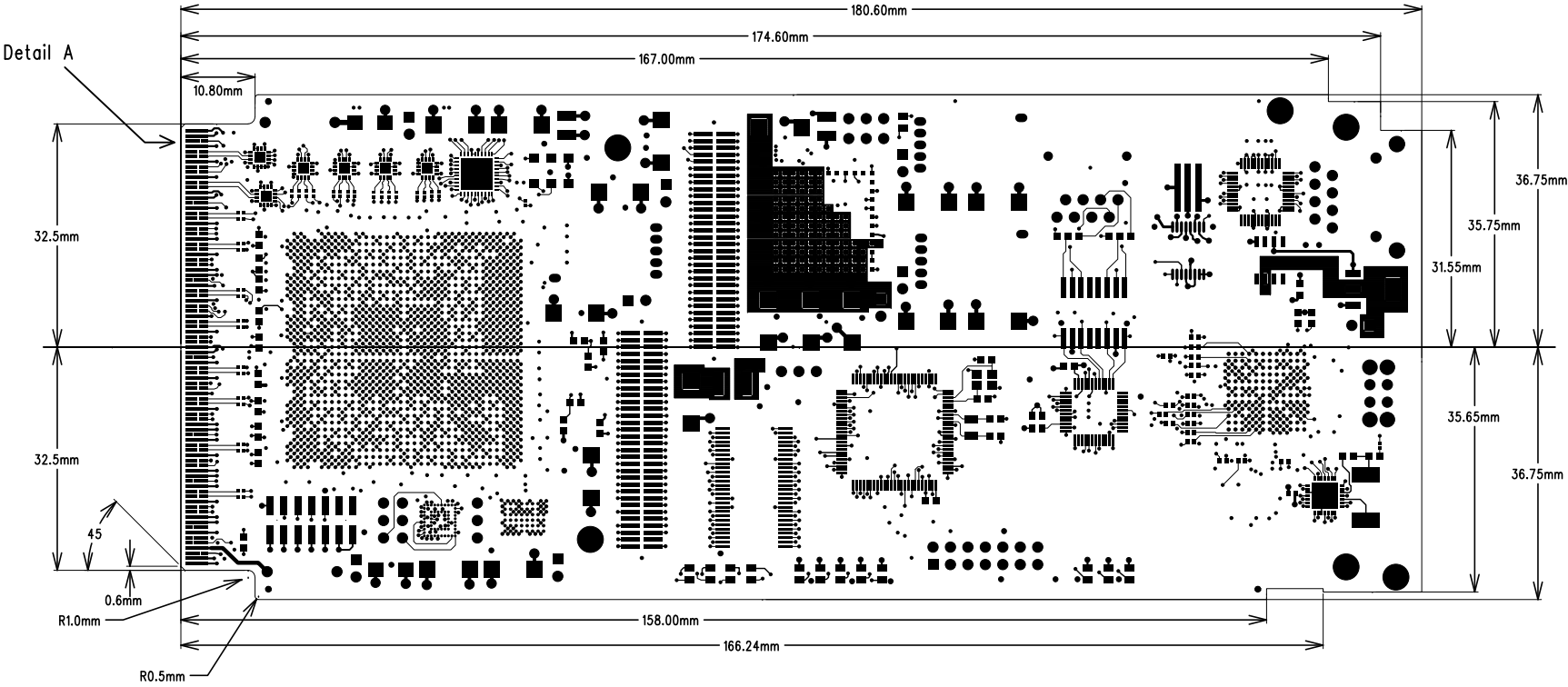


Layer Stackup



Specifications:

- Dielectric material is Nelco N4000-13 or equivalent.
- Overall thickness is 1.6 mm \pm 0.16mm as shown in Detail A.
- Controlled impedance: 50 ohms \pm 10% on 5 mil tracks on top & bottom layers and 4 mil tracks on inner layers.
- All layers use 1/2 oz. copper (before plating).
- Holes:
 - Board contains blind vias spanning layers 1-6 and layers 7-12. See top and bottom side drill drawings for size and plating requirements.
 - Hole diameters are given as after plating \pm 3 mils, except as noted.
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed.
 - Hole sizes in drill tables are given in mils.
 - Board contains 3 classes of 7.87 mil vias: Through vias spanning layers 1-12, blind vias spanning layers 1-6, and blind vias spanning layers 7-12. All other holes are through-board.
 - Drill locations are partitioned into 4 separate drill files:
 - Plated-through holes,
 - Non-Plated-through holes,
 - Layer 1-6 Blind vias,
 - Layer 7-12 Blind vias.
- Finish:
 - Module edge connector finish shall be a minimum of 0.76 microns hard gold over 2.54 microns minimum nickel.
 - Finish in component area is immersion gold.
- Minimum observed signal layer clearances are 5 mils on the outer layers and 4 mils on inner layers 3, 5, 8, and 10.
- Solder Mask (SMOBC) to be applied to both top and bottom sides. Mask shall be photoimagable, with maximum thickness of 3 mils.
- Silkscreen to applied to both top and bottom sides. Silkscreen shall be white ink.
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
- Combination of bow and twist shall not exceed 10 mils/inch along any direction.
- Design origin is at the midline of the edge connector. All layers are plotted with an (X,Y) offset (2000 mils, 4000 mils).
- Vendor may remove pads from unplated holes and plated holes without electrical connection.
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination.
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 Ohms or less.
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger.
 - Impedance of all signal layers shall be checked with TDR. Finished impedance shall be 50 Ohms \pm 10%. Vendor provides appropriate coupons for testing. Reports for each board should be included in the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units.



APPROVALS		DATE	University of Wisconsin High Energy Physics
DRAWN	TAG	02JAN08	
CHECKED			GCT MUON AUX I/O CARD REVA
APPROVED			Fabrication Instructions
SIZE	B	SCALE	DRAWING NO.
		1:1	