

Contents of GCT Muon Aux IO Module Schematics by Page Number

1. Rear AMC Connector J15 (card edge type), Front TTC pin diode/optical receiver circuit J3, Front TTS connector J17 with LVDS buffer U25, and S-Link-64 connectors J1 and J2.
2. Virtex-5 FPGA (U8) Banks 1-5. Banks 3 & 4 contain various clocks available to the device. Bank 1 contains the QPLL interface, bank 2 contains the clock switch interface, and bank 3 contains the microcontroller interface.
3. FPGA Banks 6, 11, 12, 13 and 15. Banks 6/12 and 7 contain the S-Link interface. Bank 7 also has TTS driver control signals. Bank 13 has auxiliary RS232 I/O signals. Bank 15 has the TTCRx interface.
4. FPGA Banks 17-21. Bank 17 contains LVDS TTS output signals, other banks are spare, biased at 2.5V for I/O.
5. FPGA Banks 22, 23 and 25. Spare banks biased at 2.5V for I/O.
6. FPGA GMT Banks 112-118. Connected to uTCA backplane X/R pairs 0-7.
7. FPGA GMT Banks 120/126. Connected to uTCA backplane X/R pairs 8-15.
8. FPGA Ground Connections.
9. FPGA VCC Connections plus the auxiliary RS232 I/O transceiver/connector.
10. TTC Interface. Contains TTCRx chip U15 and QPLL chip U13, plus 160.32 MHz crystal X1.
11. Clock distribution page. Contains 4x4 switch U6 plus 1:2 repeaters U17-U20 for distributing clocks to the GMT banks. Available GMT clock selections are an on-board 125.0 MHz crystal, or backplane clocks 1/3. Also contains repeaters for the QPLL 40MHz (U22, to FPGA/backplane), and the backplane clocks (U27, U28, to switch/FPGA fabric).
12. Power supplies. Contains linear 5V, 2A supply (U14 ckt) for the TTC diode. For digital logic it contains a 1.8V, 12A supply (U23), a 3.3V, 10A supply (U11), and a 2.5V, 10A supply (U10). All are driven from the main +12V source. The low-voltage supplies use super-low-ESR caps for filtering. Also has filtering and fuse/transorb circuits for the incoming +12V and pilot +3.3V
13. Secondary regulators for +1.2V (U26/Q1) and 1.0V “analog” voltage to the GMT blocks (U1), along with the 1.0V, 10A converter (U12) for the FPGA fabric.
14. FPGA configuration sheet. Copied from Matrix Card. Contains the JTAG-steering FPGA (U24), the FPGA Flash (U4), and FPGA Bank 0.
15. Microcontroller interface. Copied from Matrix Card.
16. Ethernet Interface. Copied from Matrix Card.